AN214937

Bluetooth Audio Over I^{2}S

Associated Part Family: CYW4330

This application note describes how to configure host hardware and software to transmit/receive Bluetooth audio data with the CYW4330 in I2S format. More specifically, it describes how to configure and use PCM2 intellectual property (IP) on the CYW4330 for Bluetooth audio transmissions over the I2S interface at various sample rates.

1 About This Document

1.1 Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM4330	CYW4330

1.2 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary.

2 About the I^{2}S Interface

The CYW4330 has two independent digital I^{2}S audio ports for supporting Bluetooth and high-fidelity FM audio signals. The first port, which supports Bluetooth audio and is shared with PCM IP, is commonly referred to as the I^{2}S/PCM interface.

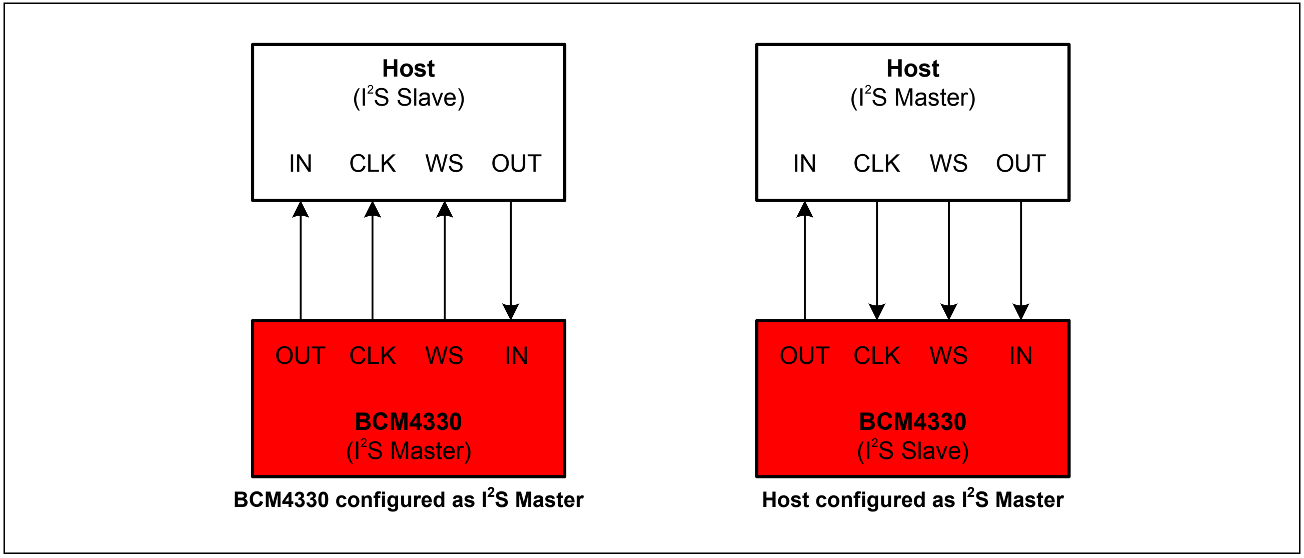
The I^{2}S/PCM interface is driven by PCM1 IP and PCM2 IP. PCM1 IP is the default for Bluetooth audio. Though PCM1 IP can be used for 8 kHz sampled Bluetooth audio transmissions, higher sampled Bluetooth audio, such as a 48 kHz sample rate, must use PCM2 IP.

Note: The Bluetooth configuration file has to be modified to use PCM2 IP to drive the I^{2}S/PCM interface on the CYW4330.

2.1 I^{2}S Interface Connections

Figure 1 shows two typical ways for making the I^{2}S interface connections between the host device and the CYW4330. The connection method selected depends on which device (master) provides the PCM clock and SYNC signals.

Figure 1. Typical I^{2}S Interface Connections



2.2 Supporting High Sample Rates

In most cases, the I^{2}S/PCM interface is configured to support an 8 kHz sample rate, which is the default sample rate for Bluetooth audio. However, the PCM2 IP can support audio transmissions at higher I^{2}S sample rates.

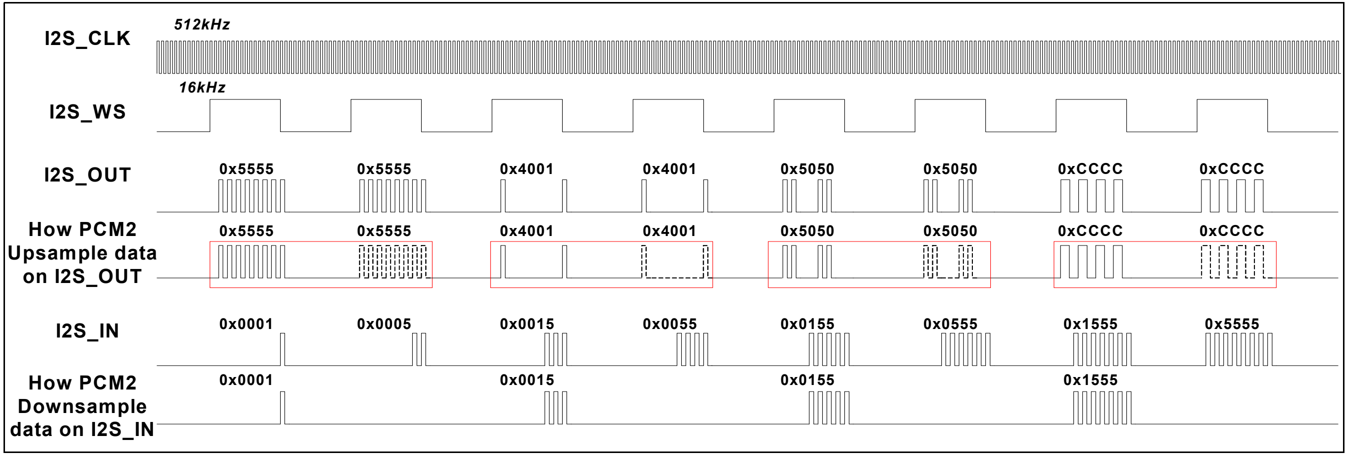
This section describes how the CYW4330 handles transmissions at high I^{2}S sample rates and the changes on the host stack required to support the higher sample rates.

2.2.1 Signal Information

Figure 2 provides a representative snapshot of the I2S_CLK, I2S_WS, and I2S_OUT signals when a sample rate (I2S_WS) of 16 kHz is used. Figure 2 shows internal signals for upsampled PCM2 data on I2S_OUT and downsampled data on I2S_IN.

Note: The CYW4330 supports a maximum I^{2}S sample rate of 128 kHz.

Figure 2. I2S_CLK, I2S_WS, and I2S_OUT Signals



Because the sample rate is twice the Bluetooth audio sample rate of 8 kHz, PCM2 IP needs upsample data on I2S_OUT and downsample data on I2S_IN. To explain how the data upsampling and downsampling works, Figure 2 also includes plots of the internal PCM2 IP signals.

An examination of the signals represented in Figure 2 reveals the following:

- I2S_CLK frequency is 32 times the I2S_WS frequency.

- I^2S data is mono audio data, with each data point having 16 bits.
- Data on I2S_OUT and I2S_IN is only valid when the I2S_WS is in logic high.
- Bluetooth audio that the CYW4330 transmits/receives is 8 kHz sampled audio data.

PCM2 IP can upsample Bluetooth audio data to a higher sample rate (I2S_WS). However, the higher I^2S sample rate must be N-1 times greater than 8 kHz. When the I2S_WS sample rate is upsampled, the CYW4330 essentially copies I^2S data N-1 times, continuously sending it out I2S_OUT at an N times upsampled I2S_WS rate. For example, when I2S_WS is upsampled at 16 kHz (2 times 8 kHz), the data on I2S_OUT is copied twice, and then transmitted in two consecutive I2S_WS periods. Figure 2 on page 2 shows pairs of duplicate I^2S data enclosed in red rectangles.

Conversely, PCM2 IP only processes input data on I2S_IN at an 8 kHz sample rate. Hence, due to downsampling, some data on I2S_IN is lost when a higher I^2S sample rate is used. This situation is reflected in Figure 2, which shows that when the input data on I2S_IN is 0x0001, 0x0005, 0x0015, 0x0055, 0x0155, 0x0555, 0x1555, and 0x5555, only 0x0001, 0x0015, 0x0155, and 0x1555 are processed by PCM2 IP.

2.2.2 Host Stack Changes

To use a higher I^2S sample rate, the host must modify the parameter values set using the PCM2_Setup command (see PCM2_Setup on page 5). The changes made only apply to the PCM_Clock_Freq and Ch_0_Period signals. The host must ensure that the two parameter values match. Supported PCM_Clock_Freq and Ch_0_Period settings are listed in Table 2, “Supported Sample Rates,” on page 6.

3 I^2S Interface Initialization

Once the host PCM hardware is configured, the host stack can issue the HCI commands required to initialize the CYW4330 to enable Bluetooth audio support over the I^2S/PCM interface using the PCM2 IP. These HCI commands must be run in the following order:

1. Write_Voice_Setting
2. Write_SCO_PCM_Int_Param
3. PCM2_Setup

Note: The Write_Voice_Setting command is a standard Bluetooth command, as is defined in the Bluetooth Core Specification. The Write_SCO_PCM_Int_Param and PCM2_Setup commands are Cypress vendor-specific commands. See 3.1 Standard and Vendor-Specific Bluetooth Command Definitions for details.

3.1 Standard and Vendor-Specific Bluetooth Command Definitions

The following assumptions are made regarding the Bluetooth commands defined in this section:

- I2S_WS signal frequency is 16 kHz.
- I^2S clock rate is 512 kHz.
- CYW4330 is configured as the I^2S/PCM master.

3.1.1 Write_Voice_Setting

This command writes the values for the Voice_Setting parameter that controls the various settings for the voice connections.

Note: This command is defined in the Bluetooth Core Specification.

Prototype:

Write_Voice_Setting Input_Coding: Linear

[26 0C 02]: 60 00

opcode=	0xC26 (3110, “Write_Voice_Setting”)
Input_Coding=	0x0 (0, “Linear”)
Input_Data_Format=	0x1 (1, “2’s complement”)
Sample_Size=	0x1 (1, “16 bit”)
Linear_PCM_Bit_Pos=	0x0 (0)
Air_Coding_Format=	0x0 (0, “CVSD”)

3.1.2 Write_SCO_PCM_Int_Param

OFC 0x01C

This command writes SCO and PCM parameter values.

Prototype:

Note: Code elements in the prototype that are important for setting up Bluetooth audio over I^{2}S/PCM are in bold type.

Write_SCO_PCM_Int_Param SCO_Routing: PCM

[1C FC 05]: 00 02 00 01 01

opcode=	0xFC1C (64540, “Write_SCO_PCM_Int_Param”)
SCO_Routing [a]=	0x0 (0, “PCM”)
PCM_Interface_Rate =	0x2 (2, “512 KBps”)
Frame_Type=	0x0 (0, “Short”)
Sync_Mode=	0x1 (1, “Master”)
Clock_Mode=	0x1 (1, “Master”)

[a] See SCO_Routing for details.

3.1.2.1 Additional Parameter Information

SCO_Routing

SCO_Routing		Size: 1 byte
Specifies whether the SCO path is through the I^{2}S/PCM interface or transport.		
Type: uint8		
Value [a]	**Description**	
0x0	PCM	
0x1	Transport	
0x2	Codec	
0x3	I^{2}S	

[a] Cannot be combined bitwise.

3.1.3 PCM2_Setup

OFC 0x0AE

This command is used to configure the PCM2 IP.

Prototype:

Note: Code elements in the prototype that are important for setting up Bluetooth audio over the I^2S/PCM interface are in bold type.

PCM2_Setup	Action: Write
[AE FC 1A]: 00 00 01 0D 00 D0 07 00 01 0F 01 00 00 00 00 00 00 00 00 01 02 03 04 01 00 00	
opcode=	0xFCAE (64686, "PCM2_Setup")
Action=	0x0 (0, "Write")
Test_Options=	0x0 (0, "")
Op_Mode=	0x1 (1, "I2S")
Sync_and_Clock_Options [a]=	0xD (13, "Sync Signal | Sync Output Enable | Generate PCM_CLK")
PCM_Clock_Freq [b]=	0x7D000 (512000)
Sync_Signal_Width=	0x1 (1)
Slot_Width=	0xF (15)
NumberOfSlots=	0x1 (1)
Bank_0_Fill_Mode=	0x0 (0, "0s")
Bank_0_Number_of_Fill_Bits=	0x0 (0)
Bank_0_Programmable_Fill_Data=	0x0 (0)
Bank_1_Fill_Mode=	0x0 (0, "0s")
Bank_1_Number_of_Fill_Bits=	0x0 (0)
Bank_1_Programmable_Fill_Data=	0x0 (0)
Data_Justify_And_Bit_Order_Options=	0x0 (0, "")
Ch_0_Slot_Number=	0x0 (0)
Ch_1_Slot_Number=	0x1 (1)
Ch_2_Slot_Number	0x2 (2)
Ch_3_Slot_Number=	0x3 (3)
Ch_4_Slot_Number=	0x4 (4)
Ch_0_Period [c]=	0x1 (1)
Ch_1_Period=	0x0 (0)
Ch_2_Period=	0x0 (0)

[a] See Sync_and_Clock_Options on page 6 for details.

[b] See PCM_Clock_Freq on page 7 for details.

[c] See Ch_0_Period on page 7 for details.

3.1.3.1 Slave Configuration

To configure the I^2S/PCM interface as the slave, the host stack must change the values of the following parameter:

Sync_and_Clock_Options = 0x0 (0, "")

For detailed information on the Sync_and_Clock_Options parameter, see Additional Parameter Information on page 6.

3.1.3.2 Sample Rate Configuration

When configuring the I^2S/PCM interface to support a particular sample rate, make sure to choose the appropriate sample rate for PCM_Clock_Freq and Ch_0_Period pair.

Table 2 lists samle rates for supported PCM_Clock_Freq and Ch_0_Period pairs.

Table 2. Supported Sample Rates

Sample Rate (I2S_WS)	Ch_0_Period	PCM_Clock_Freq
8 kHz	0x0	0x3E800 (256000)
16 kHz	0x1	0x7D000 (512000)
24 kHz	0x2	0xBB800 (768000)
32 kHz	0x3	0xFA000 (1024000)
40 kHz	0x4	0x138800 (1280000)
48 kHz	0x5	0x177000 (1536000)
56 kHz	0x6	0x1B5800 (1792000)
64 kHz	0x7	0x1F4000 (2048000)
72 kHz	0x8	0x232800 (2304000)
80 kHz	0x9	0x271000 (2560000)
88 kHz	0xa	0x2AF800 (2816000)
96 kHz	0xb	0x2EE000 (3072000)
104 kHz	0xc	0x32C800 (3328000)
112 kHz	0xd	0x36B000 (3584000)
120 kHz	0xe	0x3A9800 (3840000)
128 kHz	0xf	0x36B000 (4096000)

3.1.3.3 Additional Parameter Information

Sync_and_Clock_Options

Sync_and_Clock_Options		Size: 1 byte
Configures various Sync (WS) and clock options.		
Type: uint8		
		Values:
Bit	**Option**	**Description**
0	Sync Signal	Turns on the internal sync generator. The sync is generated as one of the following: Toggle = I^{2}S mode is selected. Pulse = PCM mode is selected (pulse width = sync_width). To enable output of the generated sync, firmware must set sync_oe (bit 21 of pcm2_config_adr).
1	Sync Aligned	Determines how sync_event is decoded. sync_gen = 1The sync event happens in the same cycle as the first bit of data in the slot. sync_gen = 0The sync event happens in the cycle before the first bit of data.
2	Sync Output Enable	Enables output of the generated sync signal. The sync_gen and sync_oe signals must be set to generate the sync signal.
3	Generate PCM_CLK	0 = CYW4330 operates as the slave device and PCM_CLK is an input. 1 = CYW4330 operates as the master device and drives PCM_CLK.
4	TriState when Idle	0 = PCM_IP drives 0 on unused slots that it transmits. 1 = PCM_IP tristates its driver when not transmitting.
5	Clock Inversion	1 = Data is driven on the falling edge of pcm_clk and sampled on the rising edge (opposite of Normal mode). 0 = Data is driven on the rising edge of pcm_clk and sampled on the falling edge.
6	N/A	–
7	N/A	–

PCM_Clock_Freq

PCM_Clock_Freq	Size: 4 bytes
Sets the I^{2}S/PCM clock rate (I2S_CLK). The I^{2}S sample rate (I2S_WS) is calculated by dividing I2S_CLK by 32.	
Type: uint32 (little endian)	

Ch_0_Period

Ch_0_Period	Size: 1 byte
Specifies the number of copies of duplicate data. 0 = No duplicate data (sample rate = 8 kHz). 1 = Duplicate data one time (sample rate = 16 kHz).	
Type: uint8	

Document History Page

Document Title: AN214937 - Bluetooth Audio Over I^{2}S Document Number: 002-14937				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	08/15/2011	4330-AN700-R Initial release
*A	5473381	UTSV	10/13/2016	Updated in Cypress template Added Cypress part numbering scheme
*B	5789060	AESATMP8	06/28/2017	Updated logo and Copyright.

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