AN214931

CYW4330 WLCSP and WLBGA Daisy Chain Package

Associated Part Family: CYW4330

This application note describes the collaborative coexistence schemes available for use with the CYW4330 Bluetooth chip.

Contents

1 Introduction

This Application Note describes the daisy chain package version of the CYW4330. Daisy chain packages can be used to assess the surface mount process and board-level reliability.

1.1 Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM4330	CYW4330

1.2 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined upon first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary.

2 IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

3 Overview

The daisy chain package comprises various pin-to-pin connections that, when attached to a compatible daisy chain board, module, or substrate, form a continuously connected loop through all critical package and/or package-to-board interconnects. This loop can be electrically tested or monitored to verify the integrity of the interconnects after the component mounting process and under Board-Level Reliability (BLR) testing.

Figure 1. High-Level Overall Daisy Chain Package and PCB Connectivity

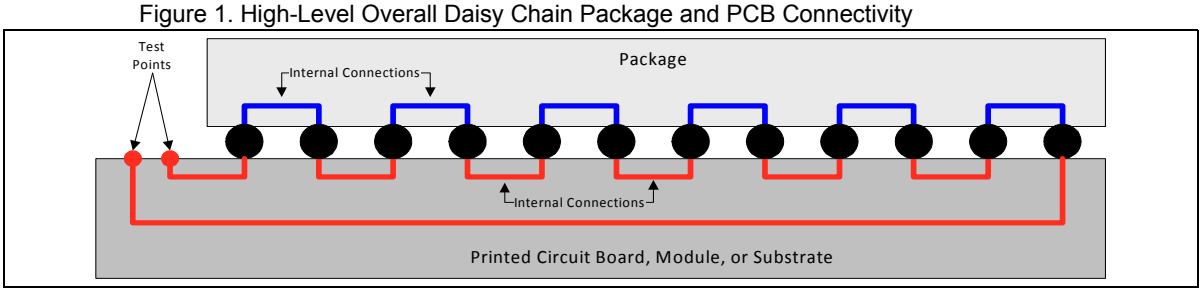
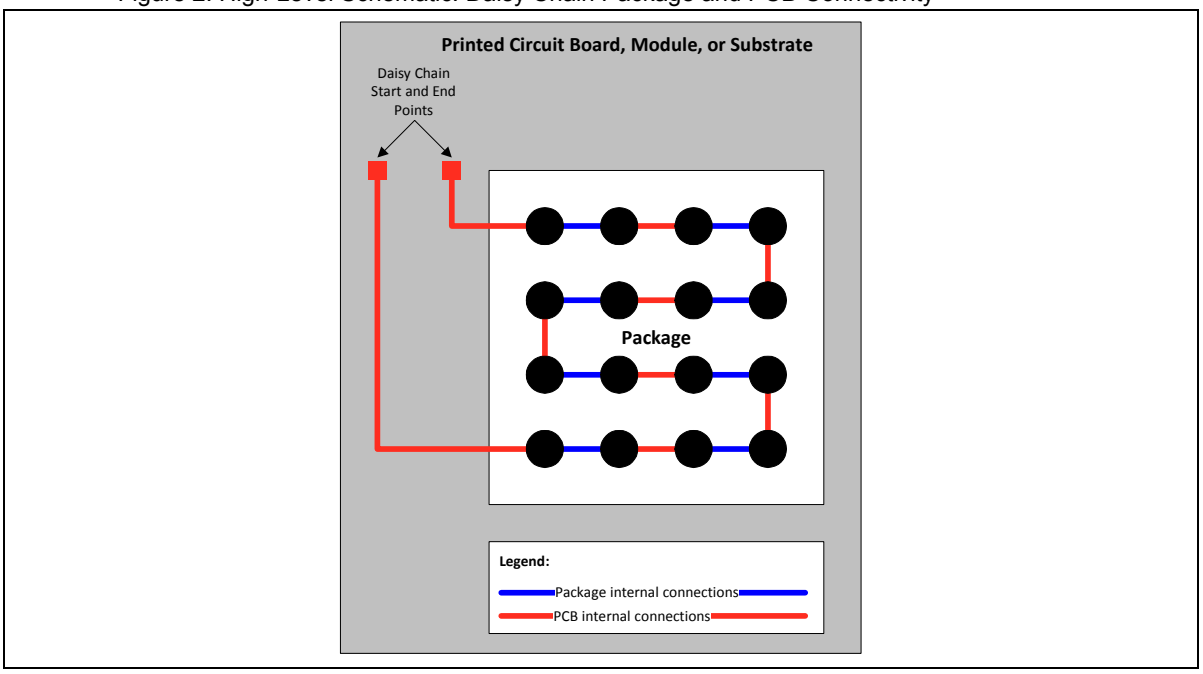


Figure 2. High-Level Schematic: Daisy Chain Package and PCB Connectivity



4 Daisy Chain Construction

The daisy chain package is designed to match the form and fit of the corresponding product; the same manufacturing processes, materials, and dimensions are used for the associated product. Where minor exceptions occur, they are described in this document.

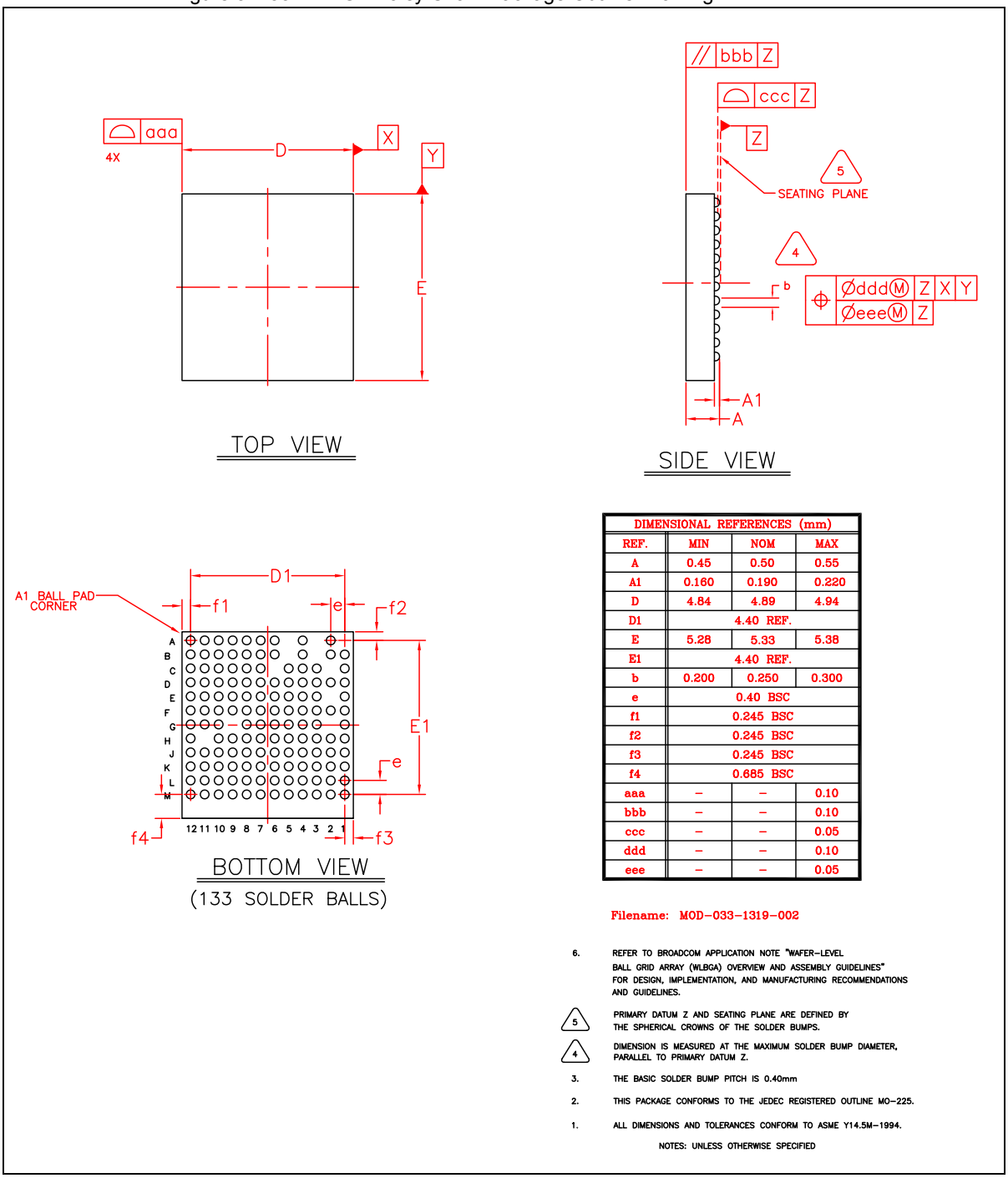
5 Package Overview

Table 2. Daisy Chain Package Overview

Package Type	WLBGA	WLCSP
Package body size	4.89 × 5.33 mm	4.89 × 5.33 mm
Package pin count	133	225
Package pin pitch	0.4 mm	0.2 mm
Package thickness	0.55 mm maximum	0.41 mm maximum

6 Package Drawings

Figure 3. 133-WLBGA Daisy Chain Package Outline Drawing



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.160	0.190	0.220
D	4.84	4.89	4.94
D1		4.40 REF.	
E	5.28	5.33	5.38
E1		4.40 REF.	
b	0.200	0.250	0.300
e		0.40 BSC	
f1		0.245 BSC	
f2		0.245 BSC	
f3		0.245 BSC	
f4		0.685 BSC	
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.05
ddd	–	–	0.10
eee	–	–	0.05

Filename: MOD-033-1319-002

6. REFER TO BROADCOM APPLICATION NOTE "WAFER-LEVEL BALL GRID ARRAY (WLBGA) OVERVIEW AND ASSEMBLY GUIDELINES" FOR DESIGN, IMPLEMENTATION, AND MANUFACTURING RECOMMENDATIONS AND GUIDELINES.

5 PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BUMPS.

4 DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM Z.

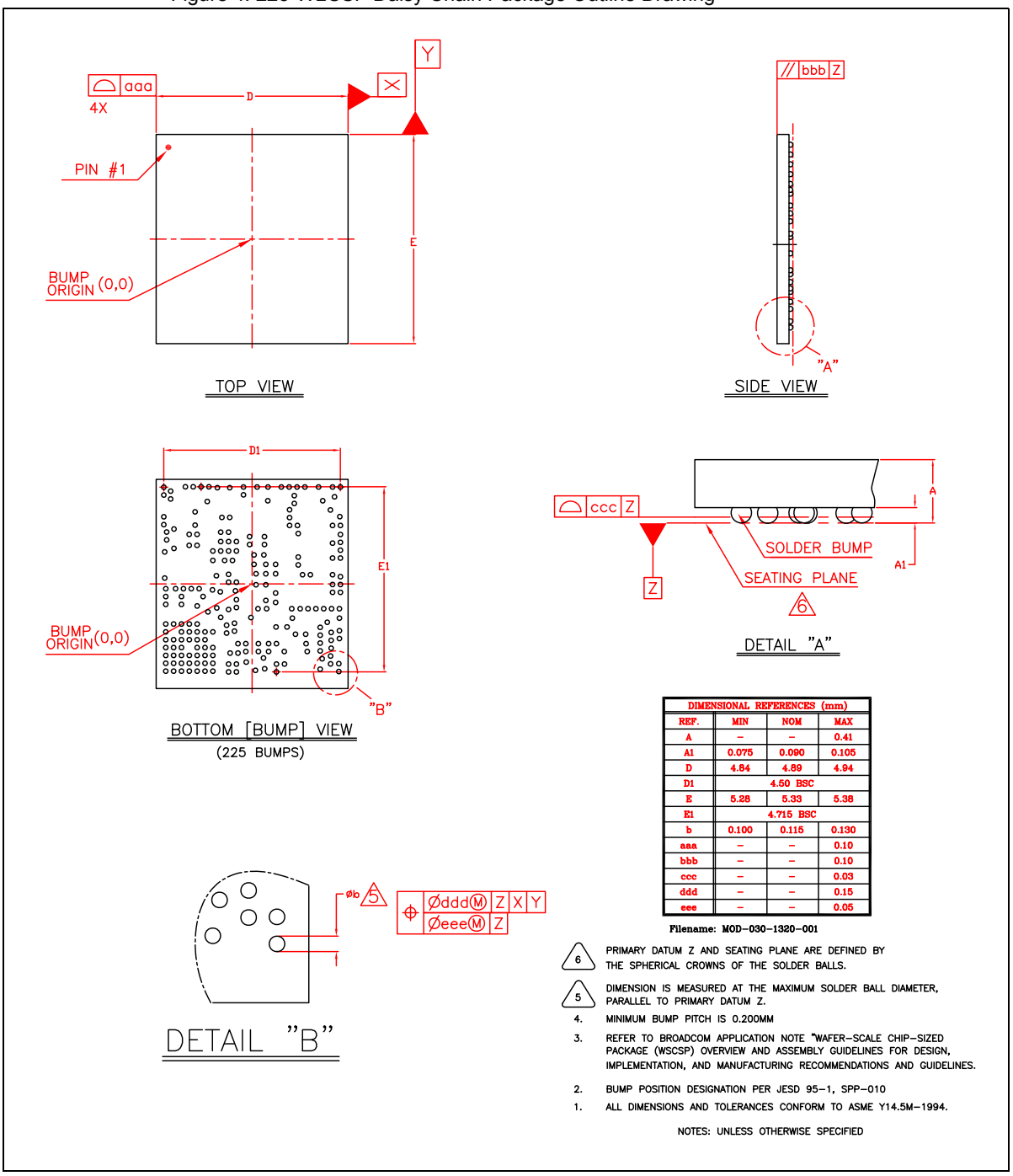
3. THE BASIC SOLDER BUMP PITCH IS 0.40mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO-225.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M-1994.

NOTES: UNLESS OTHERWISE SPECIFIED

Figure 4. 225-WLCSP Daisy Chain Package Outline Drawing



7 Package Differences

There are no construction, geometry, processes, or material differences between the CYW4330 daisy chain package and the CYW4330 product.

8 Daisy Chain Netlist, PCB Netlist, and No Connects (133-WLBGA)

Table 3 lists the daisy chain packages netlist and connectivity for the 133-WLBGA. The ball origin [0,0] is in the component center. X and Y pin coordinates are in microns.

Table 4 lists the recommended printed circuit board netlists for 133-WLBGA. When combined with the package netlist, the connections result in a continuous daisy chain.

Table 5 lists the ball not connected in the daisy chain for the 133-WLBGA.

A different PCB netlist can be implemented to achieve the same overall continuous loop; however, subsequent changes to the component daisy chain netlist will be based on the PCB netlist in Table 4. If this PCB netlist is not followed, then these component daisy chain changes may result in compatibility problems with a differently designed PCB.

Table 3. 133-WLBGA Daisy Chain Netlist and Connectivity

Ball #	Ball Name	Ball X	Ball Y		Ball #	Ball Name	Ball X	Ball Y
L12	SR_VDDBAT1	-2200	-1580	>>	M12	SR_VLX	-2200	-1980
J12	VOUT_3P3	-2200	-780	>>	K12	SR_VDDBAT1	-2200	-1180
G12	CLK_REQ_OUT	-2200	20	>>	H12	BT_GPIO_4	-2200	-380
E12	FM_RFVDD1p2	-2200	820	>>	F12	FM_VDD2p5	-2200	420
C12	FM_TX	-2200	1620	>>	D12	FM_RXN	-2200	1220
A12	FM_AOUT1	-2200	2420	>>	B12	FM_AOUT2	-2200	2020
A11	BT_VCOVDD1p2	-1800	2420	>>	B11	BT_PLLVDD1p2	-1800	2020
C11	FM_VSSAUDIO	-1800	1620	>>	D11	FM_RXP	-1800	1220
E11	FM_RFVSS	-1800	820	>>	F11	FM_VSSVCO	-1800	420
G11	TM0(NC for A0)	-1800	20	>>	J11	VOUT_3P1	-1800	-780
K11	SR_VDDBAT2	-1800	-1180	>>	L11	PMU_AVSS	-1800	-1580
M10	VDD_LDO	-1400	-1980	>>	M11	SR_PVSS	-1800	-1980
K10	BT_REG_ON	-1400	-1180	>>	L10	VOUT_LNLDO1	-1400	-1580
H10	BT_GPIO_2	-1400	-380	>>	J10	EXT_PWM_REQ	-1400	-780
F10	FM_PLLVSS	-1400	420	>>	G10	BT_RST_N	-1400	20
D10	FM_AUDIOVDD	-1400	1220	>>	E10	FM_PLLVDD	-1400	820
B10	BT_RFVSS	-1400	2020	>>	C10	BT_PLLVSS	-1400	1620
A10	BT_FEVSS	-1400	2420	>>	A9	BT_RF	-1000	2420
B9	BT_RFVDD1p2	-1000	2020	>>	C9	BT_VSS	-1000	1620
D9	BT_GPIO_1	-1000	1220	>>	E9	NC (CLK_REQ_MODE)	-1000	820
F9	BT_GPIO_0	-1000	420	>>	H9	BT_GPIO_3	-1000	-380
J9	BT_GPIO_5	-1000	-780	>>	K9	EXT_SMPS_REQ	-1000	-1180
L9	WL_REG_ON	-1000	-1580	>>	M9	VOUT_CLDO	-1000	-1980
L8	SDIO_DATA3	-600	-1580	>>	M8	SDIO_DATA1	-600	-1980
J8	WL_GPIO_4	-600	-780	>>	K8	BT_VDDC_0	-600	-1180
G8	BT_GPIO_7	-600	20	>>	H8	BT_GPIO_6	-600	-380
E8	BT_VDDC_2	-600	820	>>	F8	BT_VSSC_1	-600	420
C8	BT_IFVSS	-600	1620	>>	D8	WL_GPIO_6	-600	1220
A8	BT_PAVDD3p3	-600	2420	>>	B8	BT_IFVDD1p2	-600	2020
A7	WRF_rfin	-200	2420	>>	B7	WRF_lna2g_VDD1p2	-200	2020
C7	WRF_lna2g_GND	-200	1620	>>	D7	NC (CLK_REQ_IN)	-200	1220
E7	WL_VDDC_2	-200	820	>>	F7	BT_VDDO_0	-200	420
G7	I2S_DI	-200	20	>>	H7	I2S_DO	-200	-380
J7	LPO	-200	-780	>>	K7	WL_VDDC_1	-200	-1180
L7	SDIO_CMD	-200	-1580	>>	M7	SDIO_CLK	-200	-1980
L6	WL_GPIO_5	200	-1580	>>	M6	SDIO_DATA_0	200	-1980

Table 3. 133-WLBGA Daisy Chain Netlist and Connectivity (Continued.)

Ball #	Ball Name	Ball X	Ball Y		Ball #	Ball Name	Ball X	Ball Y
J6	PCM_IN	200	-780	>>	K6	PCM_SYNC	200	-1180
G6	UART_CTS_N	200	20	>>	H6	PCM_CLK	200	-380
D6	UART_TXD	200	1220	>>	E6	UART_RXD	200	820
A6	WRF_rfout	200	2420	>>	B6	WRF_pa_GND	200	2020
C5	WRF_GND	600	1620	>>	D5	WL_GPIO_3	600	1220
E5	WL_VSS_2	600	820	>>	F5	JTAG_SEL	600	420
G5	WL_GPIO_1	600	20	>>	H5	WL_GPIO_2	600	-380
J5	PCM_OUT	600	-780	>>	K5	rf_sw_ctrl_0	600	-1180
L5	WL_VSS_1	600	-1580	>>	M5	SDIO_DATA_2	600	-1980
L4	rf_sw_ctrl_2	1000	-1580	>>	M4	rf_sw_ctrl_3	1000	-1980
J4	rf_sw_ctrl_5	1000	-780	>>	K4	rf_sw_ctrl_7	1000	-1180
G4	WRF_afe_VDD1p2	1000	20	>>	H4	WL_GPIO_0	1000	-380
E4	WRF_gpio_out	1000	820	>>	F4	WRF_afe_GND	1000	420
C4	WRF_padrv_GND	1000	1620	>>	D4	WRF_A_TSSI_IN	1000	1220
A4	WRF_pa_VDD5p0	1000	2420	>>	B4	WRF_pa_GND	1000	2020
C3	WRF_padrv_VDD5p0	1400	1620	>>	D3	WRF_LOGEN_A_GND	1400	1220
E3	WRF_res_ext	1400	820	>>	F3	WRF_TCXO_VDD3p3	1400	420
G3	WRF_TCXO_in	1400	20	>>	H3	WRF_xtal_VDD1p2	1400	-380
J3	rf_sw_ctrl_6	1400	-780	>>	K3	rf_sw_ctrl_4	1400	-1180
L3	VDDIO_RF_0	1400	-1580	>>	M3	WL_VDDO_0	1400	-1980
L2	HSIC_DATA	1800	-1580	>>	M2	HSIC_STROBE	1800	-1980
J2	rf_sw_ctrl_1	1800	-780	>>	K2	WL_VSS_0	1800	-1180
F2	WRF_VCO_LDO_OUT_VDD1P2	1800	420	>>	H2	WRF_xtal_GND	1800	-380
B2	WRF_pa_GND	1800	2020	>>	D2	WRF_LOGEN_A_VDD1P2	1800	1220
A2	WRF_rfout_5G	1800	2420	>>	B1	WRF_rfin_5G	2200	2020
C1	WRF_ana_GND	2200	1620	>>	D1	WRF_ana_VDD1p2	2200	1220
E1	WRF_vco_ldo_in_VDD1p8	2200	820	>>	F1	WRF_vco_GND	2200	420
G1	WRF_xtal_OP	2200	20	>>	H1	WRF_xtal_ON	2200	-380
J1	HSIC_RREF	2200	-780	>>	K1	WL_VDDC_0	2200	-1180
L1	HSIC_AVDD12	2200	-1580	>>	M1	HSIC_AVSS	2200	-1980

Note: All coordinates are looking down on the package balls (dead bug).

Table 4. 133-WLBGA Recommended PCB Netlist

Ball #	Ball Name	Ball X	Ball Y		Ball #	Ball Name	Ball X	Ball Y
M1	HSIC_AVSS	2200	-1980	Connected To	External Daisy Chain START			
M12	SR_VLX	-2200	-1980	Connected To	External Daisy Chain END			
K12	SR_VDDBAT1	-2200	-1180	Connected To	L12	SR_VDDBAT1	-2200	-1580
H12	BT_GPIO_4	-2200	-380	Connected To	J12	VOUT_3P3	-2200	-780
F12	FM_VDD2p5	-2200	420	Connected To	G12	CLK_REQ_OUT	-2200	20
D12	FM_RXN	-2200	1220	Connected To	E12	FM_RFVDD1p2	-2200	820
B12	FM_AOUT2	-2200	2020	Connected To	C12	FM_TX	-2200	1620
A11	BT_VCOVDD1p2	-1800	2420	Connected To	A12	FM_AOUT1	-2200	2420
B11	BT_PLLVDD1p2	-1800	2020	Connected To	C11	FM_VSSAUDIO	-1800	1620
D11	FM_RXP	-1800	1220	Connected To	E11	FM_RFVSS	-1800	820
F11	FM_VSSVCO	-1800	420	Connected To	G11	TM0(NC for A0)	-1800	20
J11	VOUT_3P1	-1800	-780	Connected To	K11	SR_VDDBAT2	-1800	-1180
L11	PMU_AVSS	-1800	-1580	Connected To	M11	SR_PVSS	-1800	-1980
L10	VOUT_LNLDO1	-1400	-1580	Connected To	M10	VDD_LDO	-1400	-1980
J10	EXT_PWM_REQ	-1400	-780	Connected To	K10	BT_REG_ON	-1400	-1180
G10	BT_RST_N	-1400	20	Connected To	H10	BT_GPIO_2	-1400	-380
E10	FM_PLLVDD	-1400	820	Connected To	F10	FM_PLLVSS	-1400	420
C10	BT_PLLVSS	-1400	1620	Connected To	D10	FM_AUDIOVDD	-1400	1220
A10	BT_FEVSS	-1400	2420	Connected To	B10	BT_RFVSS	-1400	2020
A9	BT_RF	-1000	2420	Connected To	B9	BT_RFVDD1p2	-1000	2020
C9	BT_VSS	-1000	1620	Connected To	D9	BT_GPIO_1	-1000	1220
E9	NC (CLK_REQ_MODE)	-1000	820	Connected To	F9	BT_GPIO_0	-1000	420
H9	BT_GPIO_3	-1000	-380	Connected To	J9	BT_GPIO_5	-1000	-780
K9	EXT_SMPS_REQ	-1000	-1180	Connected To	L9	WL_REG_ON	-1000	-1580
M8	SDIO_DATA1	-600	-1980	Connected To	M9	VOUT_CLDO	-1000	-1980
K8	BT_VDDC_0	-600	-1180	Connected To	L8	SDIO_DATA3	-600	-1580
H8	BT_GPIO_6	-600	-380	Connected To	J8	WL_GPIO_4	-600	-780
F8	BT_VSSC_1	-600	420	Connected To	G8	BT_GPIO_7	-600	20
D8	WL_GPIO_6	-600	1220	Connected To	E8	BT_VDDC_2	-600	820
B8	BT_IFVDD1p2	-600	2020	Connected To	C8	BT_IFVSS	-600	1620
A7	WRF_rfin	-200	2420	Connected To	A8	BT_PAVDD3p3	-600	2420
B7	WRF_lna2g_VDD1p2	-200	2020	Connected To	C7	WRF_lna2g_GND	-200	1620
D7	NC (CLK_REQ_IN)	-200	1220	Connected To	E7	WL_VDDC_2	-200	820
F7	BT_VDDO_0	-200	420	Connected To	G7	I2S_DI	-200	20
H7	I2S_DO	-200	-380	Connected To	J7	LPO	-200	-780
K7	WL_VDDC_1	-200	-1180	Connected To	L7	SDIO_CMD	-200	-1580
M6	SDIO_DATA_0	200	-1980	Connected To	M7	SDIO_CLK	-200	-1980
K6	PCM_SYNC	200	-1180	Connected To	L6	WL_GPIO_5	200	-1580
H6	PCM_CLK	200	-380	Connected To	J6	PCM_IN	200	-780
E6	UART_RXD	200	820	Connected To	G6	UART_CTS_N	200	20
B6	WRF_pa_GND	200	2020	Connected To	D6	UART_TXD	200	1220

Table 4. 133-WLBGA Recommended PCB Netlist (Continued.)

Ball #	Ball Name	Ball X	Ball Y		Ball #	Ball Name	Ball X	Ball Y
A6	WRF_rfout	200	2420	Connected To	C5	WRF_GND	600	1620
D5	WL_GPIO_3	600	1220	Connected To	E5	WL_VSS_2	600	820
F5	JTAG_SEL	600	420	Connected To	G5	WL_GPIO_1	600	20
H5	WL_GPIO_2	600	-380	Connected To	J5	PCM_OUT	600	-780
K5	rf_sw_ctrl_0	600	-1180	Connected To	L5	WL_VSS_1	600	-1580
M4	rf_sw_ctrl_3	1000	-1980	Connected To	M5	SDIO_DATA_2	600	-1980
K4	rf_sw_ctrl_7	1000	-1180	Connected To	L4	rf_sw_ctrl_2	1000	-1580
H4	WL_GPIO_0	1000	-380	Connected To	J4	rf_sw_ctrl_5	1000	-780
F4	WRF_afe_GND	1000	420	Connected To	G4	WRF_afe_VDD1p2	1000	20
D4	WRF_A_TSSI_IN	1000	1220	Connected To	E4	WRF_gpio_out	1000	820
B4	WRF_pa_GND	1000	2020	Connected To	C4	WRF_padrv_GND	1000	1620
A4	WRF_pa_VDD5p0	1000	2420	Connected To	C3	WRF_padrv_VDD5p0	1400	1620
D3	WRF_LOGEN_A_GND	1400	1220	Connected To	E3	WRF_res_ext	1400	820
F3	WRF_TCXO_VDD3p3	1400	420	Connected To	G3	WRF_TCXO_in	1400	20
H3	WRF_xtal_VDD1p2	1400	-380	Connected To	J3	rf_sw_ctrl_6	1400	-780
K3	rf_sw_ctrl_4	1400	-1180	Connected To	L3	VDDIO_RF_0	1400	-1580
M2	HSIC_STROBE	1800	-1980	Connected To	M3	WL_VDDO_0	1400	-1980
K2	WL_VSS_0	1800	-1180	Connected To	L2	HSIC_DATA	1800	-1580
H2	WRF_xtal_GND	1800	-380	Connected To	J2	rf_sw_ctrl_1	1800	-780
D2	WRF_LOGEN_A_VDD1P2	1800	1220	Connected To	F2	WRF_VCO_LDO_OUT_VDD1P2	1800	420
A2	WRF_rfout_5G	1800	2420	Connected To	B2	WRF_pa_GND	1800	2020
B1	WRF_rfin_5G	2200	2020	Connected To	C1	WRF_ana_GND	2200	1620
D1	WRF_ana_VDD1p2	2200	1220	Connected To	E1	WRF_vco_ldo_in_VDD1p8	2200	820
F1	WRF_vco_GND	2200	420	Connected To	G1	WRF_xtal_OP	2200	20
H1	WRF_xtal_ON	2200	-380	Connected To	J1	HSIC_RREF	2200	-780
K1	WL_VDDC_0	2200	-1180	Connected To	L1	HSIC_AVDD12	2200	-1580

Note: The balls listed in Table 5 are not connected in the daisy chain. These balls should be NC on the PCB.

Table 5. 133-WLBGA Balls Not Connected in Daisy Chain

Ball #	Ball Name	Ball X	Ball Y
F6	UART_RTS_N	200	420

9 Daisy Chain Netlist, PCB Netlist, and No Connects (225-WLCSP)

Table 6 lists the daisy chain packages netlist and connectivity for the 225-WLCSP. The bump origin [0,0] is in the component center. X and Y pin coordinates are in microns.

Table 7 lists the recommended printed circuit board netlists for 225-WLCSP. When combined with the package netlist, the connections result in a continuous daisy chain.

Table 8 lists the bump not connected in the daisy chain for the 225-WLCSP.

A different PCB netlist can be implemented to achieve the same overall continuous loop; however, subsequent changes to the component daisy chain netlist are based on the PCB netlist in Table 7. If this PCB netlist is not followed, then these component daisy chain changes may result in compatibility problems with a differently designed PCB.

Table 6. 225-WLCSP Daisy Chain Netlist and Connectivity

Bump #	Bump Name	Bump X	Bump Y		Bump #	Bump Name	Bump X	Bump Y
86	SR_VLX	-2200	-2220	>>	87	SR_VLX	-2200	-2020
76	SR_VDDBAT1	-2200	-1620	>>	89	SR_VLX	-2200	-1820
79	SR_VDDBAT1	-2200	-1420	>>	98	VOUT_3P3	-2200	-1220
99	VOUT_3P3	-2200	-1020	>>	120	BT_GPIO_3	-2200	-520
115	BT_GPIO_1	-2200	-320	>>	118	BT_CLK_REQ_OUT	-2200	-120
42	FM_VDD2P5	-2227	151	>>	49	FM_VSSVCO	-2227	817
47	FM_RXP	-2177	1123	>>	48	FM_RXN	-2177	1323
43	FM_TX	-2250	1711	>>	46	FM_RXVDD1P2	-2250	1511
51	FM_AOUT1	-2250	2465	>>	52	FM_AOUT2	-2250	2265
50	FM_VDDAUDIO	-2076	2165	>>	53	FM_VSSAUDIO	-2076	2365
44	FM_RXVSS	-1991	1400	>>	45	FM_RXVSS	-1991	906
132	BT_TM1	-1750	-120	>>	133	BT_TM0	-1950	-120
119	BT_GPIO_2	-1800	-320	>>	121	BT_GPIO_4	-1800	-520
80	SR_VDDBAT1	-2000	-1420	>>	96	VOUT_3P1	-2000	-1020
77	SR_VDDBAT1	-2000	-1620	>>	90	SR_VLX	-2000	-1820
71	SR_PVSS	-2000	-2220	>>	88	SR_VLX	-2000	-2020
72	SR_PVSS	-1800	-2220	>>	74	SR_PVSS	-1800	-2020
69	PMU_AVSS	-1800	-1820	>>	78	SR_VDDBAT1	-1800	-1620
81	SR_VDDBAT2	-1800	-1420	>>	83	SR_VDDBAT2	-1800	-1220
85	SR_VDDBAT2	-1600	-1020	>>	97	VOUT_3P1	-1800	-1020
82	SR_VDDBAT2	-1600	-1420	>>	84	SR_VDDBAT2	-1600	-1220
70	PMU_AVSS	-1600	-1820	>>	75	SR_PVSS	-1600	-2020
73	SR_PVSS	-1600	-2220	>>	103	VOUT_LNLDO1	-1400	-2220
104	VOUT_LNLDO1	-1400	-2020	>>	105	VOUT_LNLDO1	-1400	-1820
95	VDD_LDO	-1400	-1620	>>	107	BT_REG_ON	-1400	-1420
109	EXT_PWM_REQ	-1400	-1220	>>	110	EXT_PWM_REQ	-1400	-1020
117	BT_GPIO_0	-1250	-320	>>	122	BT_GPIO_5	-1400	-560
124	BT_I2S_DI	-1350	-120	>>	131	BT_RST_N	-1550	-120
54	FM_VDDPLL1P2	-1603	983	>>	55	FM_VSSPLL	-1403	983
56	FM_IFVSS	-1403	1263	>>	57	FM_IFVDD1P2	-1603	1263
60	BT_PLLVSS	-1452	1499	>>	61	BT_PLLVDD1P2	-1452	1837
63	BT_VCOVSS	-1500	2475	>>	64	BT_VCOVDD1P2	-1700	2475

Table 6. 225-WLCSP Daisy Chain Netlist and Connectivity

Bump #	Bump Name	Bump X	Bump Y		Bump #	Bump Name	Bump X	Bump Y
65	BT_FEVSS	-1100	2475	>>	67	BT_LNAVDD1P2	-1300	2475
59	BT_IFVDD1P2	-770	1695	>>	62	BT_LNAVSS	-1143	2101
114	BT_CLK_REQ_MODE	-800	1080	>>	116	BT_CLK_REQ_POL	-800	1320
138	BT_VDDC	-800	840	>>	139	BT_VDDC	-1000	840
123	BT_I2S_CLK	-910	210	>>	148	BT_VDDC	-1000	600
125	BT_I2S_DO	-1010	-150	>>	126	BT_I2S_WS	-810	-200
140	BT_VDDC	-1125	-710	>>	143	BT_VDDC	-900	-610
108	BT_REG_ON	-1200	-1420	>>	111	EXT_SMPS_REQ	-1200	-1220
93	VDD_LDO	-1200	-1820	>>	94	VDD_LDO	-1200	-1620
91	VDD_LDO	-1200	-2220	>>	92	VDD_LDO	-1200	-2020
101	VOUT_CLDO	-1000	-2020	>>	102	VOUT_CLDO	-1000	-2220
100	VOUT_CLDO	-1000	-1820	>>	106	WL_REG_ON	-1000	-1620
112	EXT_SMPS_REQ	-1000	-1220	>>	141	BT_VDDC	-800	-850
144	BT_VDDC	-650	-1050	>>	145	BT_VDDC	-650	-1250
179	SDIO_DATA_2	-600	-2040	>>	214	WL_VSS	-560	-1760
176	SDIO_CMD	-400	-2240	>>	180	SDIO_DATA_3	-600	-2240
177	SDIO_DATA_0	-150	-1990	>>	178	SDIO_DATA_1	-400	-2040
175	SDIO_CLK	-360	-1760	>>	207	WL_VDDIO	-160	-1720
209	PACKAGEOPTION_0	-360	-1520	>>	210	PACKAGEOPTION_1	-160	-1520
146	BT_VDDC	-450	-1000	>>	147	BT_VDDC	-450	-1200
151	BT_VSSC	-600	-650	>>	166	LPO	-400	-600
154	BT_VSSC	-425	-175	>>	159	BT_VSSC	-400	-400
150	BT_VDDO_0	-600	245	>>	153	BT_VSSC	-600	45
149	BT_VDDO_0	-700	600	>>	157	BT_VSSC	-500	600
142	BT_VDDC	-600	840	>>	156	BT_VSSC	-400	840
152	BT_VSSC	-600	1080	>>	155	BT_VSSC	-400	1080
58	BT_IFVSS	-570	1695	>>	113	BT_CLK_REQ_IN	-600	1320
66	BT_RF	-885	2452	>>	68	BT_PAVDD3P3	-570	2452
6	WRF_GNDLNA_1P2_2G	-220	2270	>>	27	WRF_VDDLNA_1P2_2G	-220	2470
134	BT_UART_CTS_N	-65	1205	>>	137	BT_UART_TXD	-65	1005
203	WL_VDDC	50	500	>>	204	WL_VDDC	50	740
220	WL_VSS	100	-20	>>	221	WL_VSS	100	260
198	WL_VDDC	-30	-855	>>	199	WL_VDDC	150	-630
211	PACKAGEOPTION_2	160	-1520	>>	212	PACKAGEOPTION_3	160	-1720
192	WL_VDDC	85	-2200	>>	215	WL_VSS	290	-1885
165	JTAG_SEL	620	-2240	>>	194	WL_VDDC	320	-2160
206	WL_VDDIO	825	-2040	>>	208	WL_VDDIO	620	-2040
205	WL_VDDIO	820	-1720	>>	225	WL_VSS	420	-1720
216	WL_VSS	420	-1520	>>	223	WL_VSS	620	-1520
181	VDD_ISLAND	610	-1095	>>	197	WL_VDDC	370	-630
200	WL_VDDC	600	-470	>>	201	WL_VDDC	350	-420

Table 6. 225-WLCSP Daisy Chain Netlist and Connectivity

Bump #	Bump Name	Bump X	Bump Y		Bump #	Bump Name	Bump X	Bump Y
218	WL_VSS	600	-230	>>	219	WL_VSS	350	-20
128	BT_PCM_IN	350	260	>>	129	BT_PCM_OUT	600	260
127	BT_PCM_CLK	350	500	>>	130	BT_PCM_SYNC	600	500
136	BT_UART_RXD	315	1005	>>	202	WL_VDDC	300	740
10	WRF_GNDPA_3P3_2G	400	2120	>>	135	BT_UART_RTS_N	315	1205
18	WRF_RFIN_2G	128	2470	>>	20	WRF_RFOUT_2G	404	2470
31	WRF_VDDPA_3P3_2G	745	2470	>>	32	WRF_VDDPA_3P3_2G	945	2470
33	WRF_VDDPA_3P3_5G	1145	2470	>>	34	WRF_VDDPA_3P3_5G	1345	2470
11	WRF_GNDPA_3P3_2G	1075	2050	>>	12	WRF_GNDPA_3P3_5G	1075	2250
9	WRF_GNDPAD_3P3	955	1890	>>	30	WRF_VDDPAD_3P3	955	1690
2	WRF_GNDANA_1P2	955	1490	>>	25	WRF_VDDANA_1P2	1155	1490
16	WRF_G_TSSI_IN	1175	1285	>>	23	WRF_VDDAFE_1P2	1175	685
4	WRF_GNDAFE_1P2	1175	485	>>	24	WRF_VDDAFE_1P2	1285	235
5	WRF_GNDAFE_1P2	1485	235	>>	188	WL_GPIO_3	1625	-630
189	WL_GPIO_4	1425	-630	>>	191	WL_GPIO_6	1225	-630
190	WL_GPIO_5	1010	-630	>>	224	WL_VSS	1025	-870
170	RF_SW_CTRL_3	1105	-1280	>>	222	WL_VSS	890	-1095
171	RF_SW_CTRL_4	1365	-1280	>>	173	RF_SW_CTRL_6	1375	-1520
172	RF_SW_CTRL_5	1735	-2170	>>	174	RF_SW_CTRL_7	1405	-1720
168	RF_SW_CTRL_1	1735	-1705	>>	169	RF_SW_CTRL_2	1785	-1905
167	RF_SW_CTRL_0	1735	-1505	>>	182	VDDIO_RF	1735	-1305
183	VDDIO_RF	1735	-1105	>>	184	VDDIO_RF	1915	-975
186	WL_GPIO_1	2025	-630	>>	187	WL_GPIO_2	1825	-630
38	WRF_XTAL_CAB_VDDXO	2050	-14	>>	39	WRF_XTAL_CAB_VSSXO	2050	-214
22	WRF_VCOLDO_OUT_1P2	2050	660	>>	37	WRF_XTAL_CAB_VDD3V	2050	235
3	WRF_GNDANA_1P2	2050	1490	>>	15	WRF_GPIO_OUT	2050	1040
8	WRF_GNDLO_1P2_5G	1995	1885	>>	13	WRF_GNDPA_3P3_5G	1800	2120
7	WRF_GNDLNA_1P2_5G	2050	2470	>>	21	WRF_RFOUT_5G	1693	2470
19	WRF_RFIN_5G	2250	2470	>>	28	WRF_VDDLNA_1P2_5G	2100	2220
1	WRF_A_TSSI_IN	2250	1490	>>	29	WRF_VDDLO_1P2_5G	2235	1715
17	WRF_RES_EXT	2250	1060	>>	26	WRF_VDDANA_1P2	2250	1260
14	WRF_GNDVCO_1P2	2250	660	>>	35	WRF_VDD_VCOLDO_IN_1P8	2250	860
36	WRF_XTAL_CAB_CKIN3V	2250	186	>>	41	WRF_XTAL_CAB_XOP	2250	-14
40	WRF_XTAL_CAB_XON	2250	-214	>>	185	WL_GPIO_0	2225	-630
195	WL_VDDC	2225	-1190	>>	196	WL_VDDC	2225	-870
193	WL_VDDC	2015	-1235	>>	213	WL_VSS	2225	-1390
161	HSIC_AVSS	2015	-1635	>>	217	WL_VSS	2015	-1435
160	HSIC_AVDD12	2000	-1835	>>	163	HSIC_RREF	2000	-2035
162	HSIC_DATA	2210	-2230	>>	164	HSIC_STROBE	2210	-2030

Table 7. 225-WLCSP Recommended PCB Netlist

Bump #	Bump Name	Bump X	Bump Y		Bump #	Bump Name	Bump X	Bump Y
86	SR_VLX	-2200	-2220	Connected to	External Daisy Chain END			
162	HSIC_DATA	2210	-2230	Connected to	External Daisy Chain START			
87	SR_VLX	-2200	-2020	Connected to	89	SR_VLX	-2200	-1820
76	SR_VDDBAT1	-2200	-1620	Connected to	79	SR_VDDBAT1	-2200	-1420
98	VOUT_3P3	-2200	-1220	Connected to	99	VOUT_3P3	-2200	-1020
115	BT_GPIO_1	-2200	-320	Connected to	120	BT_GPIO_3	-2200	-520
42	FM_VDD2P5	-2227	151	Connected to	118	BT_CLK_REQ_OUT	-2200	-120
47	FM_RXP	-2177	1123	Connected to	49	FM_VSSVCO	-2227	817
46	FM_RXVDD1P2	-2250	1511	Connected to	48	FM_RXN	-2177	1323
43	FM_TX	-2250	1711	Connected to	52	FM_AOUT2	-2250	2265
51	FM_AOUT1	-2250	2465	Connected to	53	FM_VSSAUDIO	-2076	2365
44	FM_RXVSS	-1991	1400	Connected to	50	FM_VDDAUDIO	-2076	2165
45	FM_RXVSS	-1991	906	Connected to	133	BT_TM0	-1950	-120
119	BT_GPIO_2	-1800	-320	Connected to	132	BT_TM1	-1750	-120
96	VOUT_3P1	-2000	-1020	Connected to	121	BT_GPIO_4	-1800	-520
77	SR_VDDBAT1	-2000	-1620	Connected to	80	SR_VDDBAT1	-2000	-1420
88	SR_VLX	-2000	-2020	Connected to	90	SR_VLX	-2000	-1820
71	SR_PVSS	-2000	-2220	Connected to	72	SR_PVSS	-1800	-2220
69	PMU_AVSS	-1800	-1820	Connected to	74	SR_PVSS	-1800	-2020
78	SR_VDDBAT1	-1800	-1620	Connected to	81	SR_VDDBAT2	-1800	-1420
83	SR_VDDBAT2	-1800	-1220	Connected to	97	VOUT_3P1	-1800	-1020
84	SR_VDDBAT2	-1600	-1220	Connected to	85	SR_VDDBAT2	-1600	-1020
70	PMU_AVSS	-1600	-1820	Connected to	82	SR_VDDBAT2	-1600	-1420
73	SR_PVSS	-1600	-2220	Connected to	75	SR_PVSS	-1600	-2020
103	VOUT_LNLDO1	-1400	-2220	Connected to	104	VOUT_LNLDO1	-1400	-2020
95	VDD_LDO	-1400	-1620	Connected to	105	VOUT_LNLDO1	-1400	-1820
107	BT_REG_ON	-1400	-1420	Connected to	109	EXT_PWM_REQ	-1400	-1220
110	EXT_PWM_REQ	-1400	-1020	Connected to	122	BT_GPIO_5	-1400	-560
117	BT_GPIO_0	-1250	-320	Connected to	124	BT_I2S_DI	-1350	-120
54	FM_VDDPLL1P2	-1603	983	Connected to	131	BT_RST_N	-1550	-120
55	FM_VSSPLL	-1403	983	Connected to	56	FM_IFVSS	-1403	1263
57	FM_IFVDD1P2	-1603	1263	Connected to	60	BT_PLLVSS	-1452	1499
61	BT_PLLVDD1P2	-1452	1837	Connected to	64	BT_VCOVDD1P2	-1700	2475
63	BT_VCOVSS	-1500	2475	Connected to	67	BT_LNAVDD1P2	-1300	2475
62	BT_LNAVSS	-1143	2101	Connected to	65	BT_FEVSS	-1100	2475
59	BT_IFVDD1P2	-770	1695	Connected to	116	BT_CLK_REQ_POL	-800	1320
114	BT_CLK_REQ_MODE	-800	1080	Connected to	138	BT_VDDC	-800	840
139	BT_VDDC	-1000	840	Connected to	148	BT_VDDC	-1000	600
123	BT_I2S_CLK	-910	210	Connected to	125	BT_I2S_DO	-1010	-150
126	BT_I2S_WS	-810	-200	Connected to	143	BT_VDDC	-900	-610

Table 7. 225-WLCSP Recommended PCB Netlist (Continued.)

Bump #	Bump Name	Bump X	Bump Y		Bump #	Bump Name	Bump X	Bump Y
111	EXT_SMPS_REQ	-1200	-1220	Connected to	140	BT_VDDC	-1125	-710
94	VDD_LDO	-1200	-1620	Connected to	108	BT_REG_ON	-1200	-1420
92	VDD_LDO	-1200	-2020	Connected to	93	VDD_LDO	-1200	-1820
91	VDD_LDO	-1200	-2220	Connected to	102	VOUT_CLDO	-1000	-2220
100	VOUT_CLDO	-1000	-1820	Connected to	101	VOUT_CLDO	-1000	-2020
106	WL_REG_ON	-1000	-1620	Connected to	112	EXT_SMPS_REQ	-1000	-1220
141	BT_VDDC	-800	-850	Connected to	144	BT_VDDC	-650	-1050
145	BT_VDDC	-650	-1250	Connected to	214	WL_VSS	-560	-1760
179	SDIO_DATA_2	-600	-2040	Connected to	180	SDIO_DATA_3	-600	-2240
176	SDIO_CMD	-400	-2240	Connected to	178	SDIO_DATA_1	-400	-2040
177	SDIO_DATA_0	-150	-1990	Connected to	207	WL_VDDIO	-160	-1720
175	SDIO_CLK	-360	-1760	Connected to	209	PACKAGEOPTION_0	-360	-1520
147	BT_VDDC	-450	-1200	Connected to	210	PACKAGEOPTION_1	-160	-1520
146	BT_VDDC	-450	-1000	Connected to	151	BT_VSSC	-600	-650
159	BT_VSSC	-400	-400	Connected to	166	LPO	-400	-600
153	BT_VSSC	-600	45	Connected to	154	BT_VSSC	-425	-175
149	BT_VDDO_0	-700	600	Connected to	150	BT_VDDO_0	-600	245
142	BT_VDDC	-600	840	Connected to	157	BT_VSSC	-500	600
155	BT_VSSC	-400	1080	Connected to	156	BT_VSSC	-400	840
113	BT_CLK_REQ_IN	-600	1320	Connected to	152	BT_VSSC	-600	1080
58	BT_IFVSS	-570	1695	Connected to	66	BT_RF	-885	2452
27	WRF_VDDLNA_1P2_2G	-220	2470	Connected to	68	BT_PAVDD3P3	-570	2452
6	WRF_GNDLNA_1P2_2G	-220	2270	Connected to	134	BT_UART_CTS_N	-65	1205
137	BT_UART_TXD	-65	1005	Connected to	204	WL_VDDC	50	740
203	WL_VDDC	50	500	Connected to	221	WL_VSS	100	260
199	WL_VDDC	150	-630	Connected to	220	WL_VSS	100	-20
198	WL_VDDC	-30	-855	Connected to	211	PACKAGEOPTION_2	160	-1520
212	PACKAGEOPTION_3	160	-1720	Connected to	215	WL_VSS	290	-1885
192	WL_VDDC	85	-2200	Connected to	194	WL_VDDC	320	-2160
165	JTAG_SEL	620	-2240	Connected to	208	WL_VDDIO	620	-2040
205	WL_VDDIO	820	-1720	Connected to	206	WL_VDDIO	825	-2040
216	WL_VSS	420	-1520	Connected to	225	WL_VSS	420	-1720
181	VDD_ISLAND	610	-1095	Connected to	223	WL_VSS	620	-1520
197	WL_VDDC	370	-630	Connected to	201	WL_VDDC	350	-420
200	WL_VDDC	600	-470	Connected to	218	WL_VSS	600	-230
128	BT_PCM_IN	350	260	Connected to	219	WL_VSS	350	-20
129	BT_PCM_OUT	600	260	Connected to	130	BT_PCM_SYNC	600	500
127	BT_PCM_CLK	350	500	Connected to	202	WL_VDDC	300	740
135	BT_UART_RTS_N	315	1205	Connected to	136	BT_UART_RXD	315	1005
10	WRF_GNDPA_3P3_2G	400	2120	Connected to	18	WRF_RFIN_2G	128	2470

Table 7. 225-WLCSP Recommended PCB Netlist (Continued.)

Bump #	Bump Name	Bump X	Bump Y		Bump #	Bump Name	Bump X	Bump Y
20	WRF_RFOUT_2G	404	2470	Connected to	31	WRF_VDDPA_3P3_2G	745	2470
32	WRF_VDDPA_3P3_2G	945	2470	Connected to	33	WRF_VDDPA_3P3_5G	1145	2470
12	WRF_GNDPA_3P3_5G	1075	2250	Connected to	34	WRF_VDDPA_3P3_5G	1345	2470
9	WRF_GNDPAD_3P3	955	1890	Connected to	11	WRF_GNDPA_3P3_2G	1075	2050
2	WRF_GNDANA_1P2	955	1490	Connected to	30	WRF_VDDPAD_3P3	955	1690
16	WRF_G_TSSI_IN	1175	1285	Connected to	25	WRF_VDDANA_1P2	1155	1490
4	WRF_GNDAFE_1P2	1175	485	Connected to	23	WRF_VDDAFE_1P2	1175	685
5	WRF_GNDAFE_1P2	1485	235	Connected to	24	WRF_VDDAFE_1P2	1285	235
188	WL_GPIO_3	1625	-630	Connected to	189	WL_GPIO_4	1425	-630
190	WL_GPIO_5	1010	-630	Connected to	191	WL_GPIO_6	1225	-630
222	WL_VSS	890	-1095	Connected to	224	WL_VSS	1025	-870
170	RF_SW_CTRL_3	1105	-1280	Connected to	171	RF_SW_CTRL_4	1365	-1280
173	RF_SW_CTRL_6	1375	-1520	Connected to	174	RF_SW_CTRL_7	1405	-1720
169	RF_SW_CTRL_2	1785	-1905	Connected to	172	RF_SW_CTRL_5	1735	-2170
167	RF_SW_CTRL_0	1735	-1505	Connected to	168	RF_SW_CTRL_1	1735	-1705
182	VDDIO_RF	1735	-1305	Connected to	183	VDDIO_RF	1735	-1105
184	VDDIO_RF	1915	-975	Connected to	187	WL_GPIO_2	1825	-630
39	WRF_XTAL_CAB_VSSXO	2050	-214	Connected to	186	WL_GPIO_1	2025	-630
37	WRF_XTAL_CAB_VDD3V	2050	235	Connected to	38	WRF_XTAL_CAB_VDDXO	2050	-14
15	WRF_GPIO_OUT	2050	1040	Connected to	22	WRF_VCOLDO_OUT_1P2	2050	660
3	WRF_GNDANA_1P2	2050	1490	Connected to	8	WRF_GNDLO_1P2_5G	1995	1885
13	WRF_GNDPA_3P3_5G	1800	2120	Connected to	21	WRF_RFOUT_5G	1693	2470
7	WRF_GNDLNA_1P2_5G	2050	2470	Connected to	19	WRF_RFIN_5G	2250	2470
28	WRF_VDDLNA_1P2_5G	2100	2220	Connected to	29	WRF_VDDLO_1P2_5G	2235	1715
1	WRF_A_TSSI_IN	2250	1490	Connected to	26	WRF_VDDANA_1P2	2250	1260
17	WRF_RES_EXT	2250	1060	Connected to	35	WRF_VDD_VCOLDO_IN_1P8	2250	860
14	WRF_GNDVCO_1P2	2250	660	Connected to	36	WRF_XTAL_CAB_CKIN3V	2250	186
40	WRF_XTAL_CAB_XON	2250	-214	Connected to	41	WRF_XTAL_CAB_XOP	2250	-14
185	WL_GPIO_0	2225	-630	Connected to	196	WL_VDDC	2225	-870
193	WL_VDDC	2015	-1235	Connected to	195	WL_VDDC	2225	-1190
213	WL_VSS	2225	-1390	Connected to	217	WL_VSS	2015	-1435
160	HSIC_AVDD12	2000	-1835	Connected to	161	HSIC_AVSS	2015	-1635
163	HSIC_RREF	2000	-2035	Connected to	164	HSIC_STROBE	2210	-2030

Note: The bumps listed in Table 8 are not connected in the daisy chain. These bumps should be NC on the PCB.

Table 8. 225-WLCSP Bumps Not Connected in Daisy Chain

Bump #	Bump Name	Bump X	Bump Y
158	BT_VSSC	-400	45

10 Schematic Views

Figure 5. 133-WLBGA Daisy Chain Schematic View

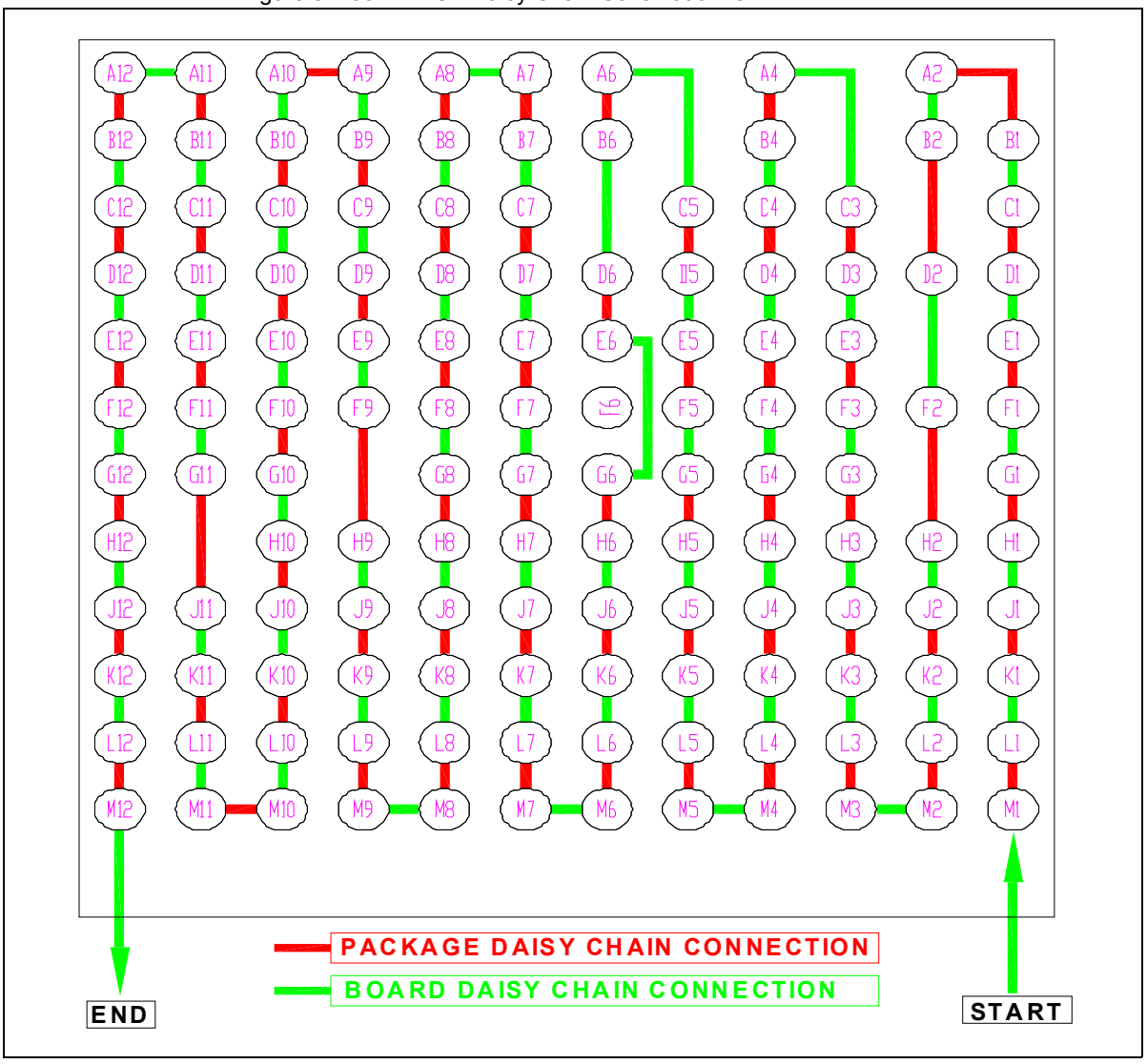
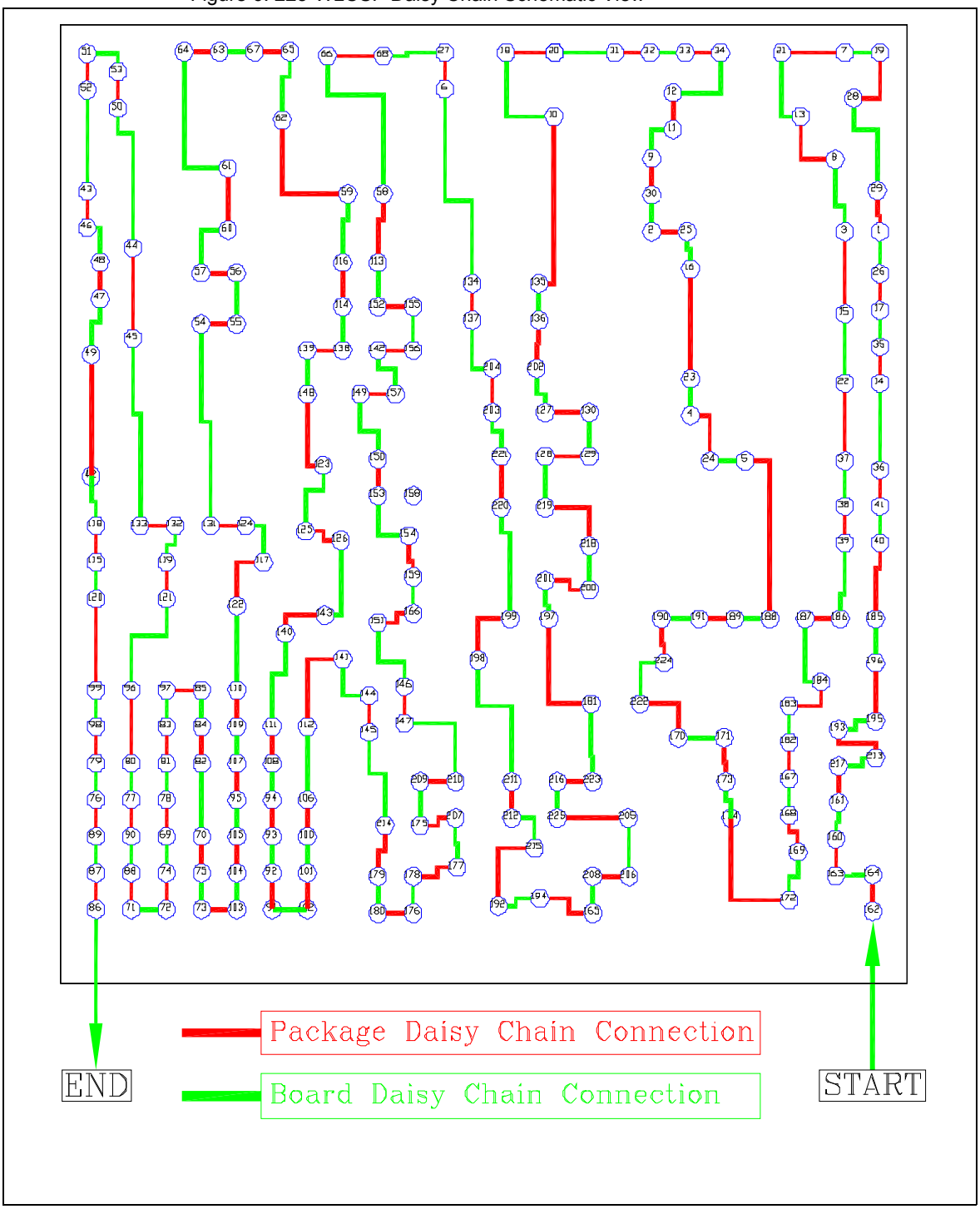


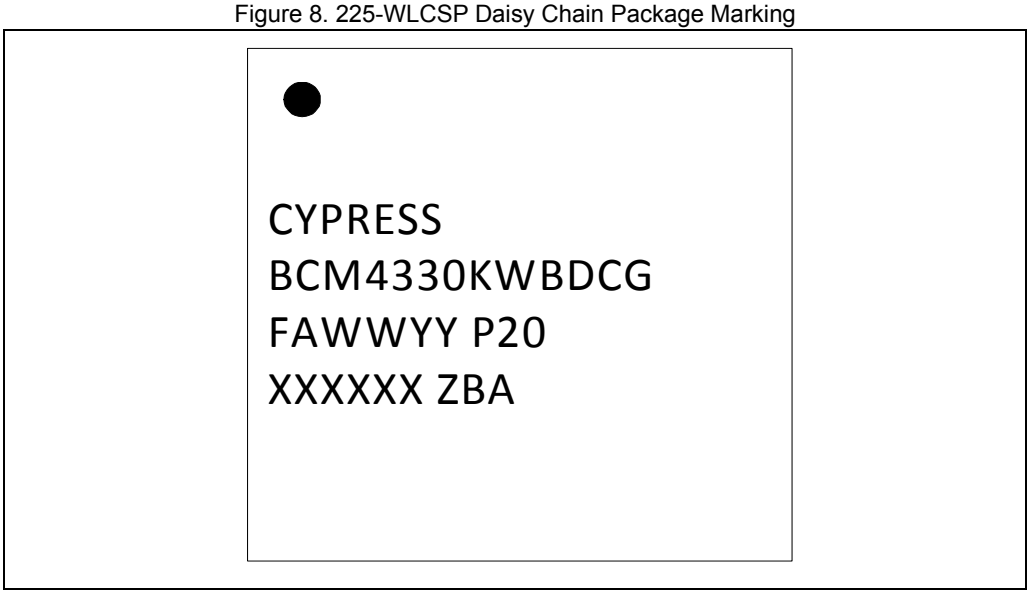
Figure 6. 225-WLCSP Daisy Chain Schematic View



11 Daisy Chain Package Marking

Figure 7. 133-WLBGA Daisy Chain Package Marking

Figure 8. 225-WLCSP Daisy Chain Package Marking



11.1 Package Marking Field Description

Multiple suppliers are listed in Table 9, but all suppliers listed may not be used for this part.

Table 9. Package and Supplier Codes

Field	Field Meaning	Supplier	Supplier Code
F	Wafer foundry	TSMC	T
		CHRT	C
		SMIC	H
		UMC	U
		N/A	Z[a]
A	T/R supplier	UTAC	D
		STATS	T
		ASE	E
		SPIL	N
YYWW	Date code	N/A	YY = Year: WW = Work Week
P20	Internal code	N/A	N/A
B	Bumping supplier	TSMC	T
		SPIL	N
		ASE	E
		Nepes	F
		SMIC	H
		STATS	S
		Amkor	A
Z	Internal code	N/A	N/A

a. In many daisy chain components, there is no fab-dependent content. If the fab code = Z, then the daisy chain component is fully manufactured by the assembly/bumping supplier.

11.2 Daisy Chain Part Variations

Table 10. Daisy Chain Part Variations

Part Number	Package	Notes
BCM4330KUBDCG	133 ball WLBGA (4.89 x 5.33 mm, 0.4 mm pitch)	Solder = SACX
BCM4330KWBDCG	225 ball WLCSP (4.89 x 5.33 mm, 0.2 mm pitch)	Solder = 98.2Sn/1.8Ag

12 Application Notes

Various package types have application notes associated with them; the appropriate application note should be reviewed prior to design and manufacturing. Application notes are available on DocSAFE or from the Broadcom sales, marketing, and field application engineers departments.

When retrieving documents from docSAFE, replace the “vv” in the document number with the largest number available in the repository to ensure access to the most current version of the document.

Table 11. Package-Specific Application Notes

Package Type	*Document Number*	*Description*
WLCSP	PACKAGING-AN3vv-R	Wafer-Scale Chip-Sized Package (WSCSP) overview and assembly guidelines
WLBGA	PACKAGING-AN6vv-R	Wafer-Level Ball Grid Array (WLBGA) overview and assembly guidelines
FBGA, PBGA, and other laminate-based BGA variants	PACKAGING-AN1vv-R	Reflow process guidelines for surface mount assemblies. Printed circuit board land pattern recommendations for ball grid array
	PACKAGING-AN5vv-R	

Document History Page

Document Title: AN214931 - CYW4330 WLCSP and WLBGA Daisy Chain Package Document Number: 002-14931				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	-	06/07/2010	4330-AN100-R Initial Release.
*A	5457425	UTSV	09/01/2016	Updated in Cypress template
*B	5879601	AESATMP8	09/11/2017	Updated logo and Copyright.

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