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AN214930

Printed Circuit Board Layout Guidelines and Component Selection for Optimized PMU Performance

Associated Part Family: CYW4330/CYW4336

This Application Note covers theCYW4330/CYW4336 PMU section (i.e., CBUCK, LDO3P3/3P1, CLDO, LNLDO) .The PMU pins are arranged in a compact way, so that when components are placed close to their respective regulator pins, the board routing can be done easily without causing interference to other parts of the chip.

Contents

1 Introduction

This Application Note covers the CYW4330/CYW4336 PMU section (i.e., CBUCK, LDO3P3/3P1, CLDO, LNLDO) and makes the following recommendations:

- Correct placement of components to facilitate optimal board routing and chip performance.
- Proper routing of traces to PMU components to account for noise coupling/EMI, current-flow capability, and PMU performance.
- Understanding the trade-offs in PMU component selection (e.g., different footprints/ratings) and the implications for overall PMU functionality and performance.

1.1 Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM4330	CYW4330
BCM4336	CYW4336

1.2 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined upon first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary.

2 IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

3 Correct PMU Component Placement

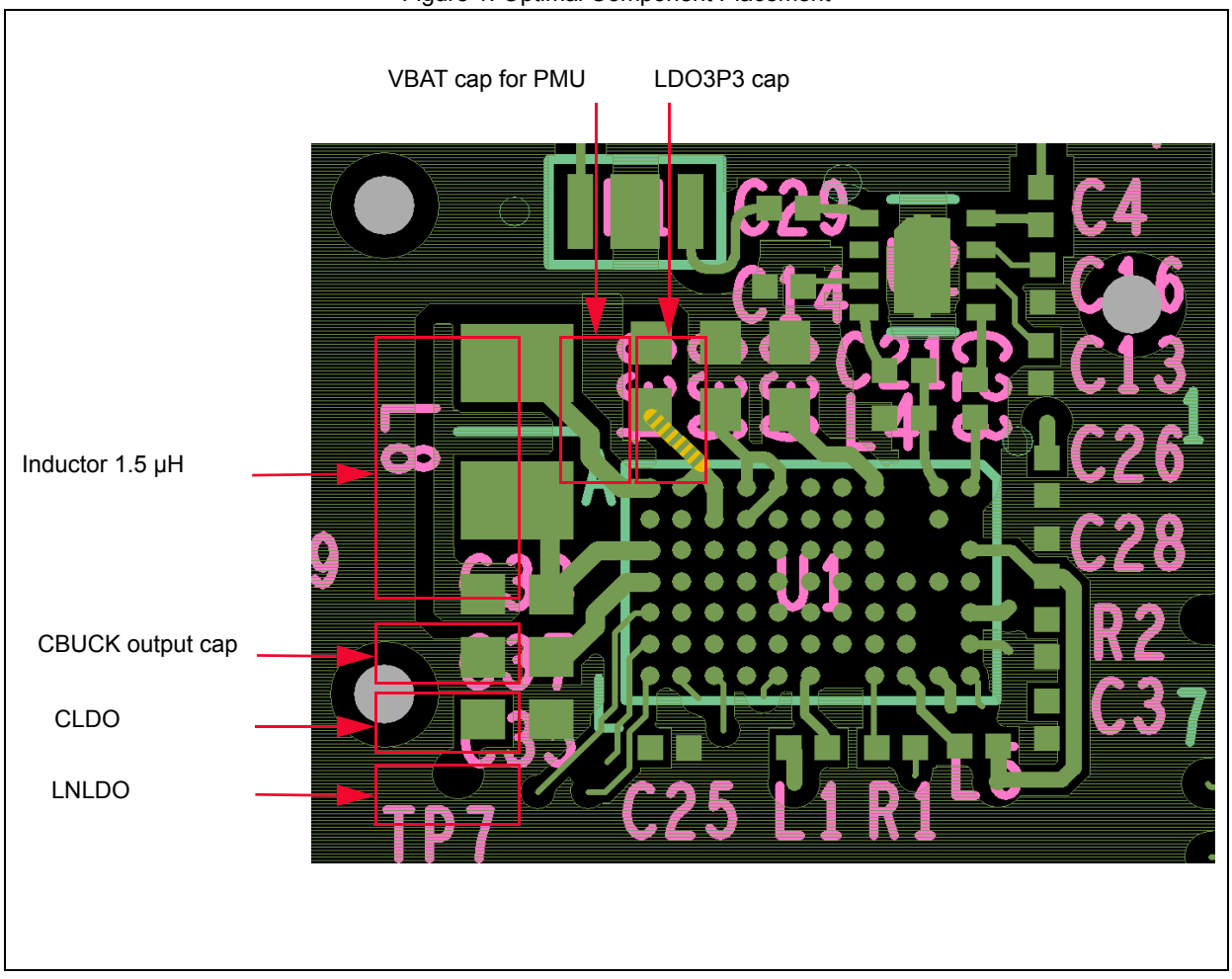
The PMU pins are arranged in a compact way, so that when components are placed close to their respective regulator pins, the board routing can be done easily without causing interference to other parts of the chip.

Figure 4 shows an example of optimal placement for the critical PMU components in close proximity to their respective regulator pins. Based on the CYW94336SDG Cypress reference board, the yellow box outlines all the critical PMU-related components. By placing these components close to their connecting pins, routing can be achieved with minimal length, as shown in Figure 4.

The highlighted components are:

- L8 = 0806 size SR_VLX pin LQM2MPN1R5NG0 Murata®
- C34 = 0402 size VBAT shared cap for SR_VDDBAT1 & 2 pins, 6.3V 4.7 µF ±20% X5R, Murata
- C38 = 0402 size CBUCK output cap, 6.3V 4.7 µF ±20% X5R, Murata
- C37 = 0402 size VOUT_CLDO cap, 6.3V 2.2 µF ±20% X5R, Murata
- C35 = 0402 size VOUT_LNLDO cap, 6.3V 2.2 µF ±20% X5R, Murata
- C36 = 0402 size VOUT_3P3 cap, 10V, 1 µF ±10% X5R, Murata

Figure 1. Optimal Component Placement



4 PMU Board Routing Considerations

Figure 2 shows the routing using the top layer (i.e., the same layer as the footprints for components and CYW4336 WLBGA chip placement). Use of vias and routing layers other than the top layer is strongly discouraged for the following reasons:

- Microvias have lower current carrying capability.
  - The VLX signal and inductor must carry up to 500 mA DC with a ripple of 800 mA pk-pk.
  - The VBAT supply line must carry up to 600 mA of combined average current for CBUCK and LDO3P3.
  - LDO3P3 sources a maximum of 80 mA, CLDO max 150 mA, LNLDO1 max 150 mA (300 mA for the CYW4330).
- Microvias have high parasitic resistance and inductance. Any extra parasitic will add to power losses and higher switching noise spikes, causing interference.
- Using microvias and lower layers increases the CBUCK switching current loop area, which is directly proportional to the radiated EMI (see Figure 3).

In Figure 2, all routings are the shortest and widest possible to minimize parasitic resistance and inductance. Regulators are sensitive to routing parasitics, which can cause instability, power efficiency losses, and in extreme cases may cause the regulator to lose voltage regulation. Extreme parasitics caused by long skinny traces can also lead to large switching voltage spikes ,which can lead to long-term chip reliability problems.

Figure 2. Mandatory PMU Component Routing – Length/Width Rules

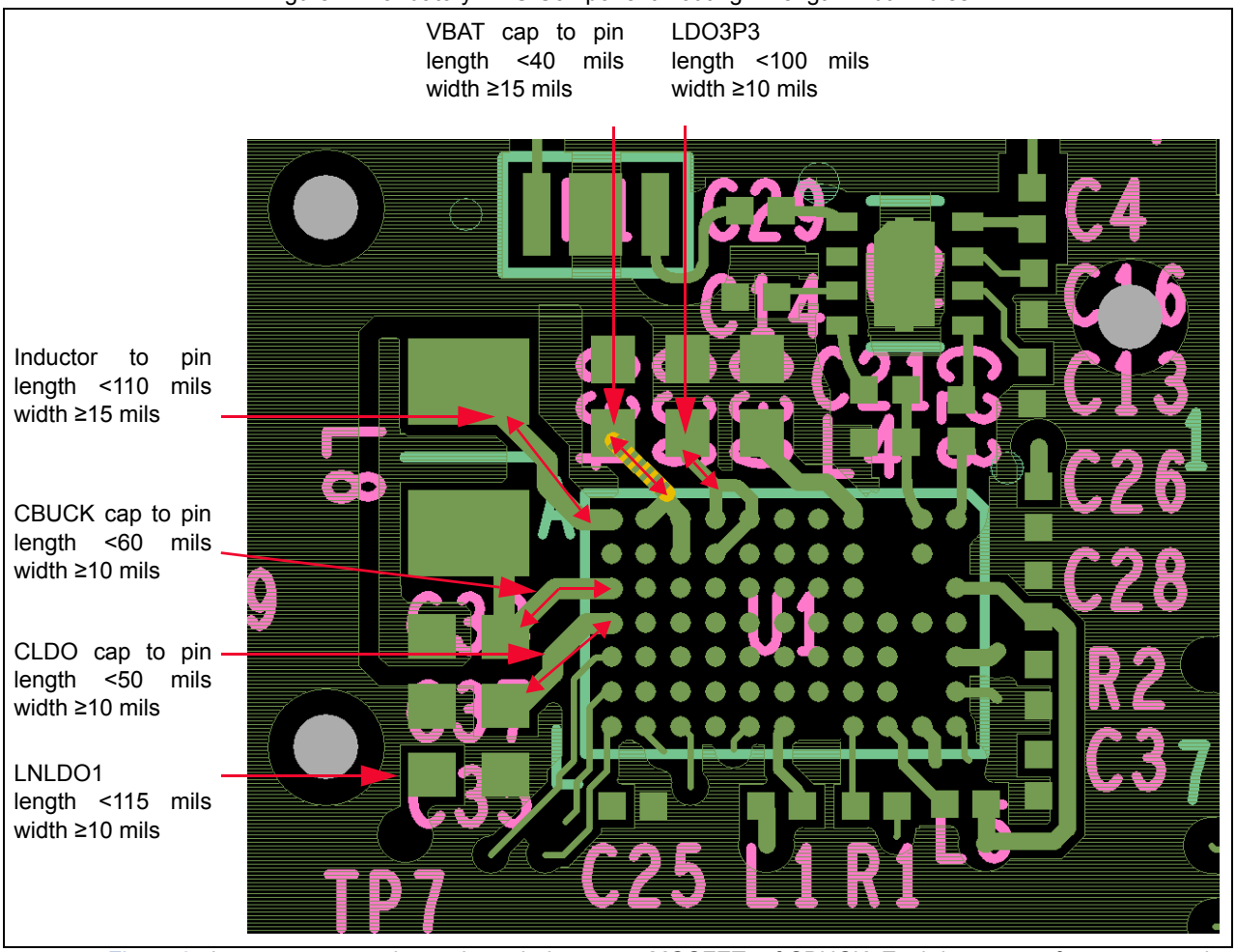


Figure 3 shows two current loops through the power MOSFETs of CBUCK. Each loop starts from a cap and ends at its ground terminal. The radiated EMI is proportional to the area within each loop. Routing of sensitive signals through the areas bounded by these two loops should be strictly avoided.

Figure 3. EMI Loops in Buck Switching Regulator

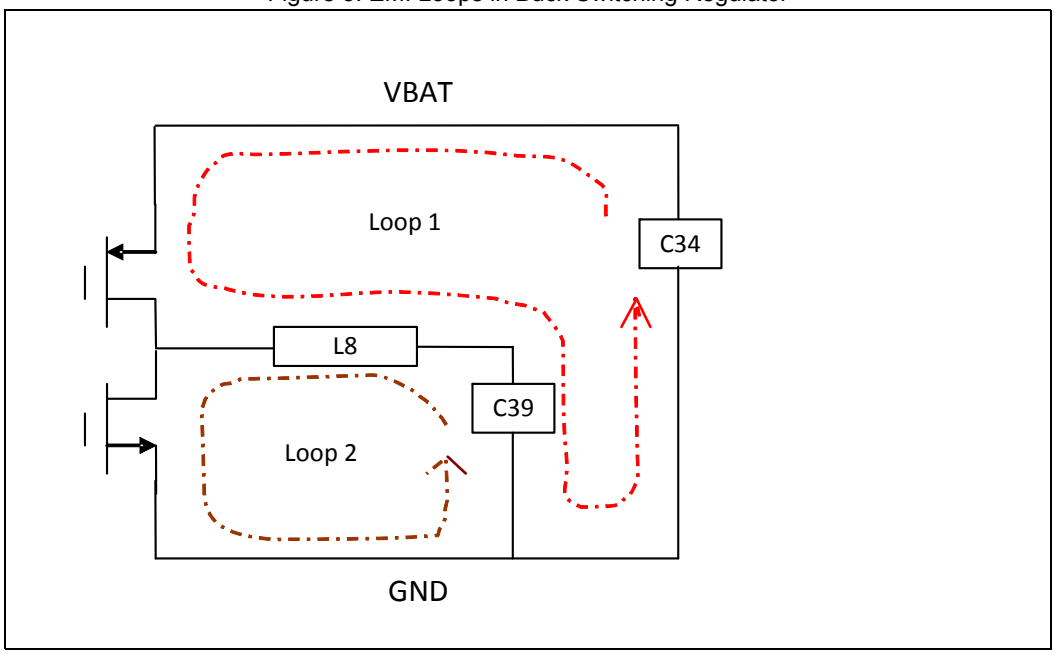


Figure 4 shows how the four top layers are used around the PMU. Loop 1 from Figure 3 is shown as a red loop. Loop 2 from Figure 3 is shown as a yellow loop.

There is a separate ground island on layer 2 under L8 (top-right in Figure 4). This is also connected to the SR_PVSS (CBUCK power ground pin). This ground island helps contain the noise in the area within loop 1. The SR_VLX trace from pin SR_VLX to L8 runs on top of this layer 2 ground island to mirror the ground return path in loop 2.

The ground island under L8 on layer 2 is densely populated with vias (see Figure 5) that connect to another ground island on layer 3, then to the main ground plane on layer 4. These vias can carry up to 500 mA of current; therefore, many vias must be used to reduce inductance and avoid ringing on the SR_PVSS pin during CBUCK switching.

Figure 4. Top Layers

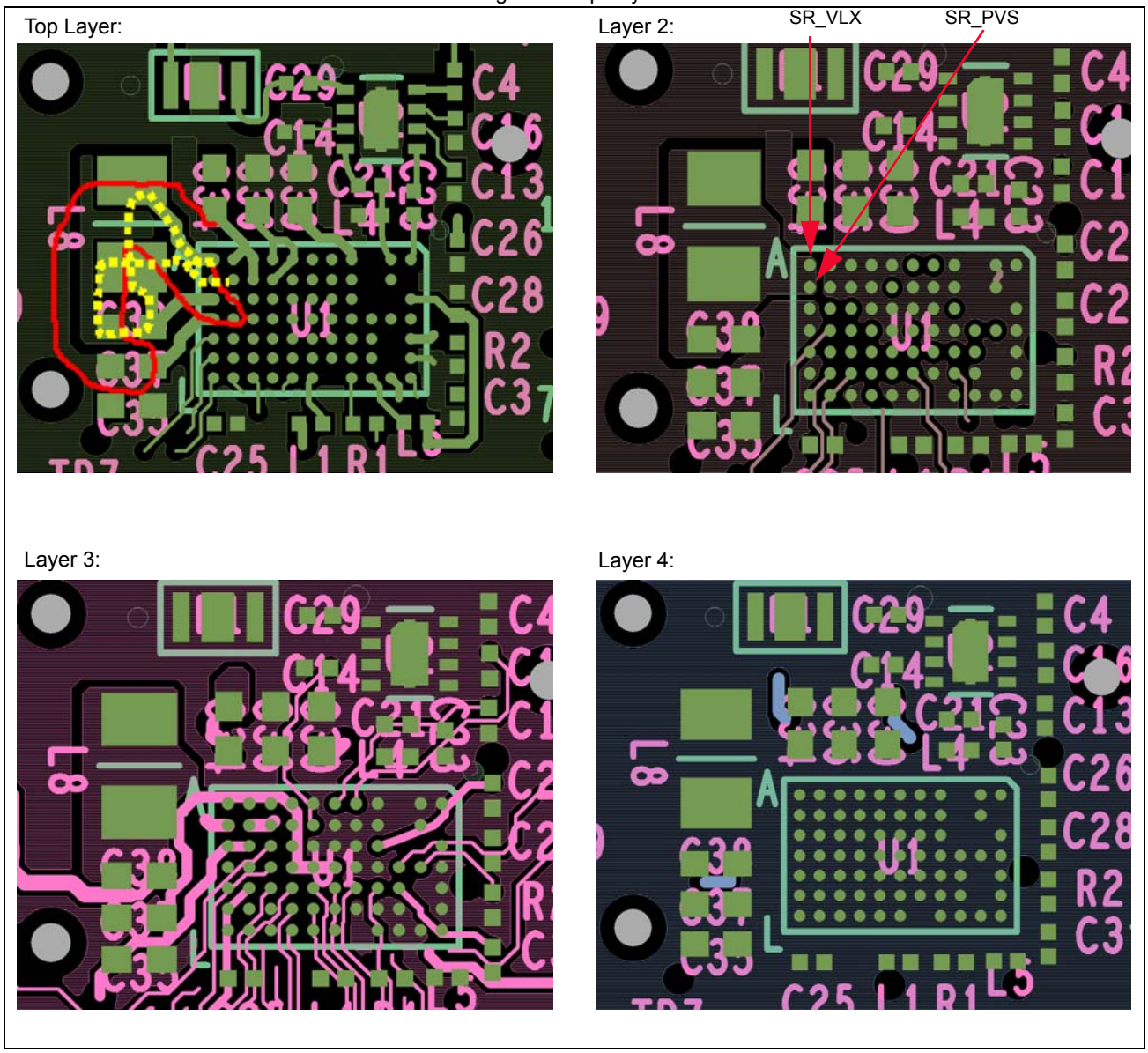


Figure 5 shows grounding on the top layer, covering the L8 inductor footprint and the regulator caps. This allows maximum coverage of ground for the PMU and allows more vias for the top layer ground plane to the underlying main ground plane.

Figure 5. Top Layer Grounding and Use of Ground Vias

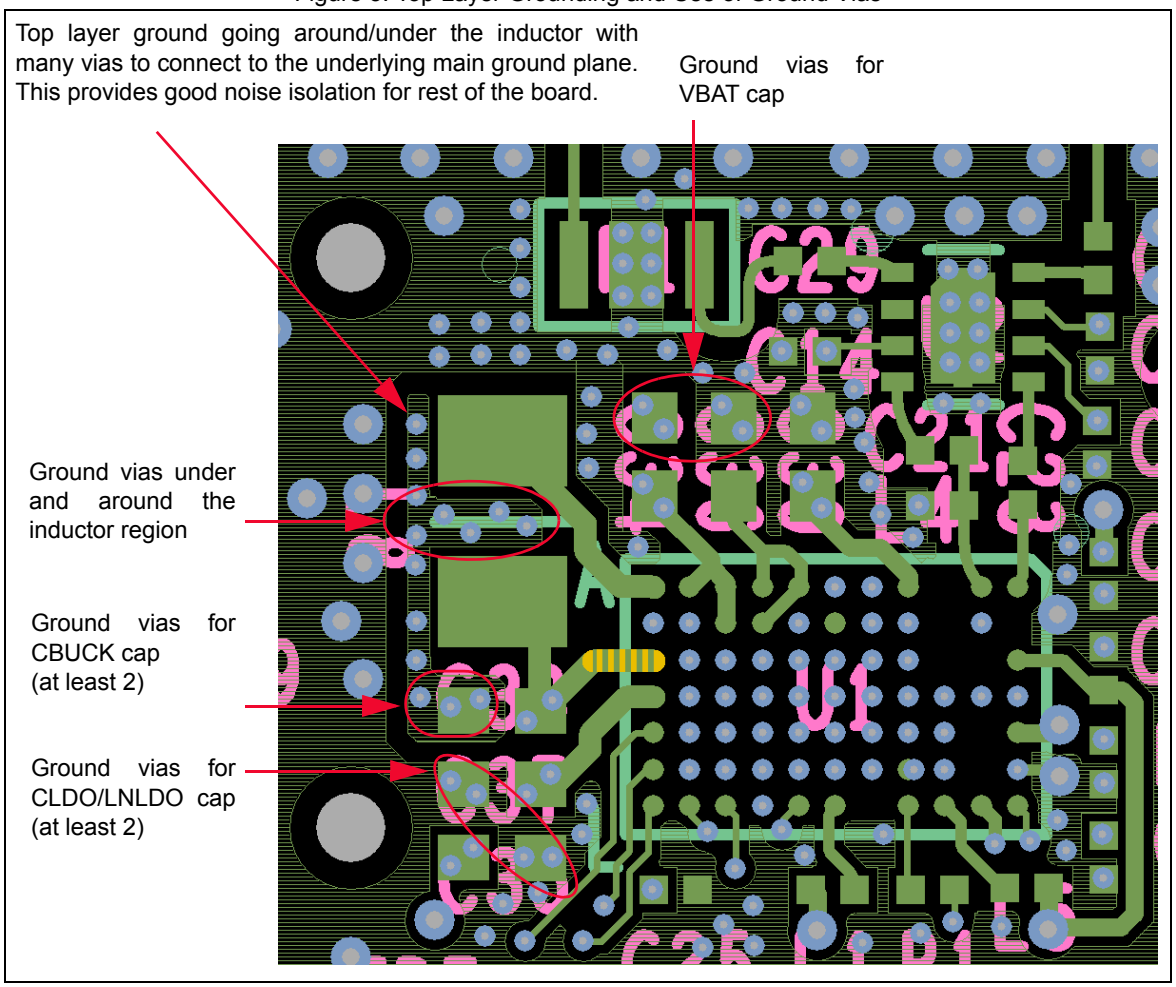
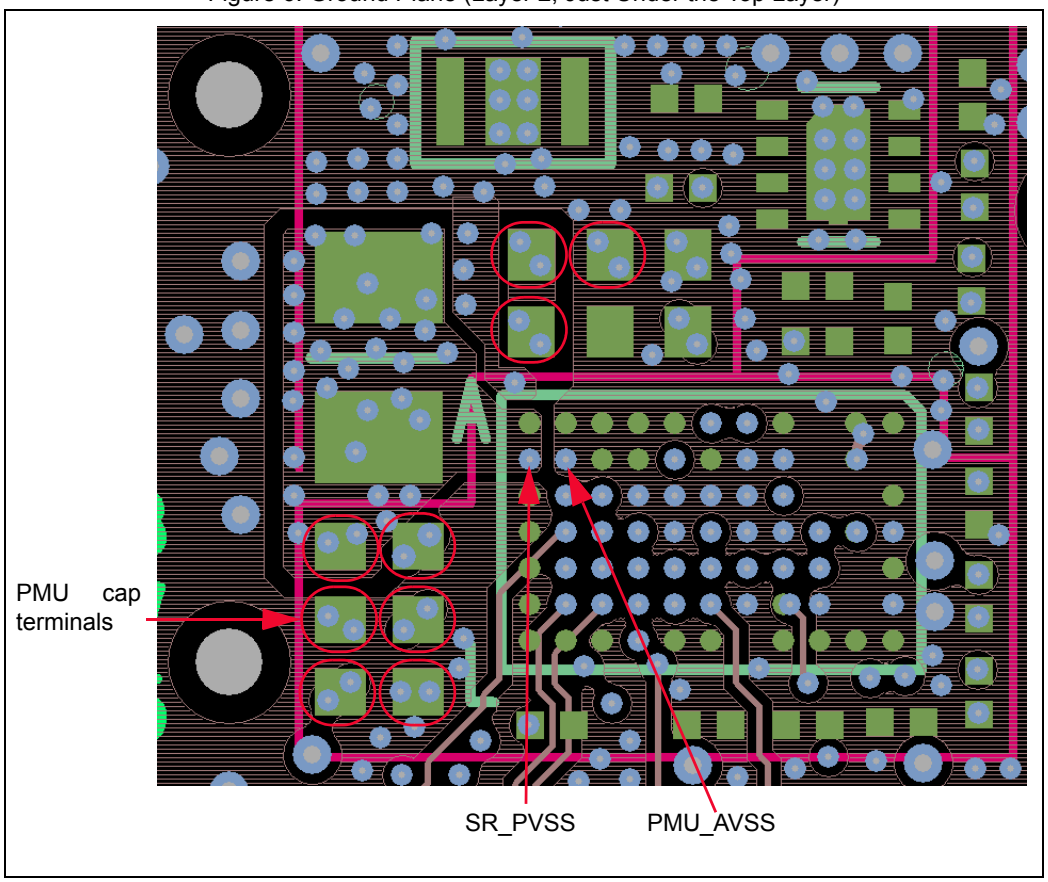


Figure 6 shows layer 2 with microvias added. The ground island under inductor L8 is populated by several vias for a good, low-parasitic connection to the ground plane at lower layers. Also, all PMU cap terminals are connected by at least two vias per terminal for low-parasitic connections to the main ground plane.

The main ground of CBUCK (SR_PVSS) and the quiet analog ground (PMU_AVSS) are connected by separate ground planes on layer 2, then they are ultimately joined in the main ground plane on layer 4. The separation of ground planes prevents the quiet ground from being contaminated by the large ground switching currents of SR_PVSS.

Figure 6. Ground Plane (Layer 2, Just Under the Top Layer)



5 Component Selection

This section explains how component characteristics are assessed and discusses the implications of selecting components that have inferior qualities.

Components that seem to have the same rating may not behave in the same manner due to different transient characteristics that cannot be fully described by their component ratings.

Board and module designers are strongly advised to use **only the recommended PMU components**, since these components have been thoroughly validated in system characterization, including extensive system tests run over the full operating temperature range.

5.1 Capacitors

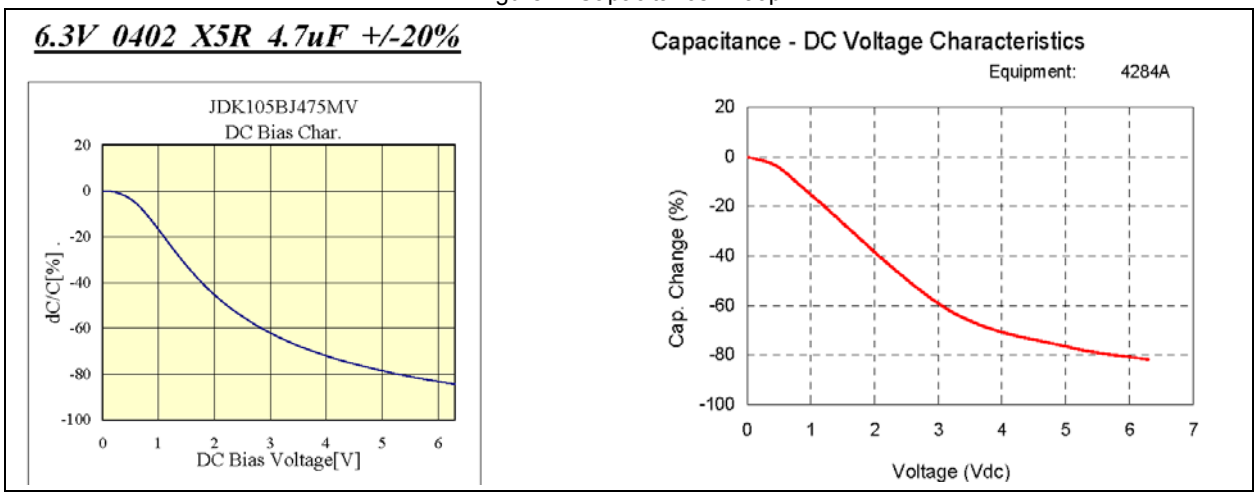
MLCC capacitors suffer from the following effects:

- Part-to-part tolerance
- Capacitance droop under DC-voltage bias
- Capacitance variation under temperature change (X5R)
- Aging effects

5.1.1 Capacitance Droop under DC Voltage Bias

Capacitors with the same description may not necessarily show the same behavior. This is especially true for cap sizes smaller than 0603 (e.g., 0402 or 0201). The plots in Figure 7 show two 0402 size caps from two different manufacturers with significantly different performance. Both are 0402, X5R, 4.7 µF, ±20%, 6.3V ceramic caps.

Figure 7. Capacitance Droop



The cap in the left plot drops by 46% at 2V bias, compared to the cap shown in the right plot, which drops by only 38%.

5.1.2 ESR, ESL, and Self-Resonant Frequency

0603-size capacitors tend to have smaller ESR/ESL and higher Self-Resonant Frequency (SRF) compared to smaller profile 0402 size capacitors. Therefore, 0603-size capacitors tend to have better performance than 0402-size capacitors.

Users are advised to follow the following recommended list of capacitors for CBUCK, CLDO, LNLDO, and LDO3P3/3P1. No substitutes should be used without consulting Cypress's WLAN applications team.

CBUCK output cap:

- Capacitance should not drop more than 26.4% under 1.5V bias (i.e., CBUCK output voltage) or drop more than 38.2% under 2V bias.
- After accounting for all the above effects, residual capacitance needed for CBUCK stability is 1.90 µF ≤ 4.7 µF ≤ 5.64 µF.
- Recommended caps (not in order of preference):
  - GRM188R60J475ME84D (0603 X5R 4.7 µF 20% 6.3V Murata)
  - GRM188R60J475ME19D (0603 X5R 4.7 µF 20% 6.3V Murata)
  - GRM188R61A475KE15 (0603 X5R 4.7 µF 20% 10V Murata)
  - GRM155R60J475M (0402 X5R 4.7 µF 20% 6.3V Murata)

SR_VDDBAT1,SR_VDDBAT2,SR_VDDBAT3 cap:

- Capacitance should not drop more than 80% at extreme 5.5V VBAT level. It should not drop more than 73% at 4.3V VBAT level.
- After accounting for all the above effects, the residual capacitance needed for good VBAT noise suppression is 1.2 µF for Vbat = 4.3V.
- Strongly recommended caps (not in order of preference):
  - GRM188R60J106ME84D (0603 X5R 10 µF 20% 6.3V Murata)
  - GRM188R60J106ME47D (0603 X5R 10 µF 20% 6.3V Murata)
  - GRM188R60J475ME84D (0603 X5R 4.7 µF 20% 6.3V Murata)
  - GRM188R60J475ME19D (0603 X5R 4.7 µF 20% 6.3V Murata)
  - GRM155R60J475M (0402 X5R 4.7 µF 20% 6.3V Murata)

CLDO output cap:

- Capacitance should not drop more than 20% under 1.25V bias (i.e., CLDO output).
- After accounting for all the above effects, the residual capacitance needed for CLDO stability is 3 µF ≤ 4.7 µF ≤ 5.64 µF (for CYW4330), 1.43 µF ≤ 2.2 µF ≤ 2.97 µF (for CYW4336).
- Recommended caps for CYW4330 (not in order of preference):
  - GRM188R60J475ME84D (0603 X5R 4.7 µF 20% 6.3V Murata)
  - GRM188R60J475ME19D (0603 X5R 4.7 µF 20% 6.3V Murata)
  - GRM188R61A475KE15 (0603 X5R 4.7 µF 20% 10V Murata)
  - GRM155R60J475M (0402 X5R 4.7 µF 20% 6.3V Murata)
- Recommended cap for CYW4336:
  - GRM155R60J225M (0402 X5R 2.2 µF 20% 6.3V Murata)

LNLDO1 Output Cap:

- Capacitance should not drop more than 20% under 1.25V bias (i.e., LNLDO1 output).
- After accounting for all the above effects, the residual capacitance needed for LNLDO1 stability is 3 µF ≤ 4.7 µF ≤ 5.64 µF (for CYW4330), 1.43 µF ≤ 2.2 µF ≤ 2.97 µF (for CYW4336).
- Recommended caps for CYW4330 (not in order of preference):
  - GRM188R60J475ME84D (0603 X5R 4.7 µF 20% 6.3V Murata)
  - GRM188R60J475ME19D (0603 X5R 4.7 µF 20% 6.3V Murata)
  - GRM188R61A475KE15 (0603 X5R 4.7 µF 20% 10V Murata)
  - GRM155R60J475M (0402 X5R 4.7 µF 20% 6.3V Murata)
- Recommended cap for CYW4336:
  - GRM155R60J225M (0402 X5R 2.2 µF 20% 6.3V Murata)

LDO3P3/LDO3P1 Output Cap:

- Capacitance should not drop more than 20% under 2.5V bias.

- After accounting for all the above effects, the residual capacitance needed for 2.5V stability is 0.6 µF ≤ 1 µF ≤ 1.4 µF.
- Recommended cap:
  - GRM155R61A105K (0402 X5R 1 µF 10% 10V Murata)

5.2 Inductors

The following are the recommended default inductors:

- Murata LQM2MPN1R5NG0 (for CYW4336 CBUCK)
- Murata LQM2MPN2R2NG0 (for CYW4330 CBUCK)

These are multi-layered inductors that exhibit more dynamic characteristics compared to wire-wound inductors and have been assessed by Cypress based on the following parameters:

- Inductor part-to-part tolerance: preferably not greater than ±20%
- DCR:
  - DCR vs. temperature
- ACR:
  - ACR vs. frequency under no-load, mid-load, max-load conditions
  - ACR vs. frequency under minimum, typical, max operating temperatures, at max-load
  - ACR vs. 3.2 MHz ripple current amplitude for no-load and max-load conditions
- Isat1: saturation current based on nominal inductance –30%
- Isat2: saturation current based on +40°C self-heating temperature rise
- Inductance under Isat2 vs. operating temperature range (i.e., –40°C to +125°C)
- Shielding

All the above characteristics must be known before an inductor can be assessed for its suitability for CBUCK.

5.2.1 DCR

DCR contributes to the conduction power losses of the CBUCK. DCR should be kept below 200 mΩ maximum for the following reasons:

- Ensure voltage regulation under high-duty cycle scenario (e.g., VBAT = 2.3V, Vout = 1.833V, Max 500 mA load).
- DCR exceeding 200 mΩ can lead to as much as 5% power loss.

DCR over-operating temperature range should be <200 mΩ maximum for the reasons described above.

5.2.2 ACR

ACR contributes to switching power losses in the CBUCK.

- ACR vs frequency under no-load, mid-load, max-load conditions
- ACR should be <1Ω under no-load conditions to ensure lower switching losses at low-loads.
- ACR vs Frequency under minimum, typical, max operating temperatures, at max-load
- ACR at 3.2 MHz over –40°C to +125°C at 500 mA load should be <2Ω.
- ACR vs 3.2 MHz ripple current amplitude for no-load and max-load conditions.

  In actual switching regulator operation, there is a DC load current sourced from the switcher through the inductor to the load. Within the inductor, there is an AC current component switching at 3.2 MHz (PWM mode) called the inductor ripple current. This inductor current sinks into the CBUCK output cap and is not seen by the load.

  ACR at no-DC load +400 mA pk-pk AC at 3.2 MHz should be <14Ω.

  ACR at max 500 mA DC +400 mA pk-pk AC at 3.2 MHz should be <2Ω.

  As shown in the limits above, ACR at the no-load condition is usually higher due to the inductor core hysteresis behavior.

5.2.3 Saturation Currents

5.2.3.1 Isat1

Multi-layered inductor data sheets usually do not display Isat1 explicitly due to lower current level. Isat1 is defined as the load current that causes the inductance to drop by 30% from the nominal value.

For CYW4336 CBUCK with a nominal value of 1.5 µH, the inductance must not drop below 0.8 µH nominal at 500 mA load.

For CYW4330 CBUCK with a nominal value of 2.2 µH, the inductance must not drop below 1.5 µH nominal at 500 mA load.

5.2.3.2 Isat2

Isat2 is usually shown on multi-layered data sheets and is usually higher than Isat1. Isat2 is defined as the saturation current causes the inductor to self-heat by +40°C.

Isat2 should be much higher than 500 mA; preferably >700 mA.

Inductance under Isat2 vs operating temperature range (i.e., –40°C to +125°C)

Inductance should be characterized with Isat2 across the full operating temperature range of the inductor.

The recommended operating temperature range is –40°C to +125°C inclusive of the inductor self-rise temperature (i.e., +40°C).

The inductor operating temp up to +125°C (including inductor self-heating +40°C) corresponds to the product temperature maximum of 85°C.

Inductance should not vary more than ±4% over the operating temperature range (–40°C to +125°C) under Isat2.

Shielding

Magnetic shielding, ferrite drum shielding, or magnetic-resin coated shielding is highly recommended to prevent EMI issues.

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