AN214926

CYW4329 WLBGA Daisy Chain Package

Associated Part Family: CYW4329

This application note describes the daisy chain package version of the CYW4329. Daisy chain packages can be used to assess the surface-mount process and board-level reliability.

Contents

1 Introduction

This application note describes the daisy chain package version of the CYW4329. Daisy chain packages can be used to assess the surface-mount process and board-level reliability.

1.1 Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM4329	CYW4329
BCM4329KUBDCG	CYW4329KUBDCG

1.2 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined upon first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary.

2 IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

3 Overview

The daisy chain package consists of various pin-to-pin connections that, when attached to a compatible daisy chain board, module, or substrate, form a continuously connected loop through all critical package and/or package-to-board interconnects. This loop can be electrically tested or monitored to verify the integrity of the interconnects after the component-mounting process and under board-level reliability (BLR) testing.

Figure 1. High-Level Overall Daisy Chain Package and PCB Connectivity

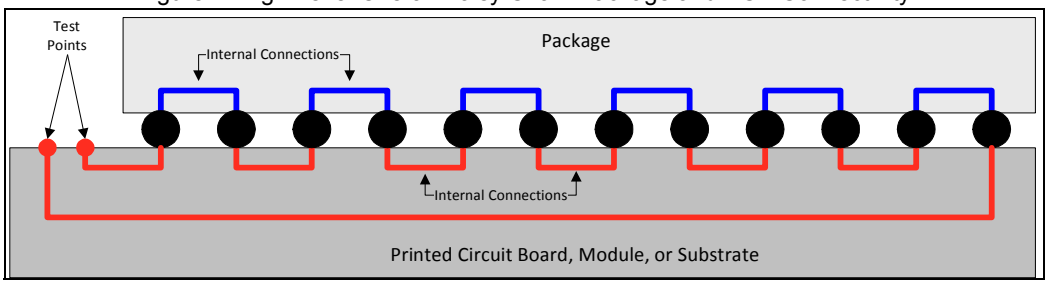
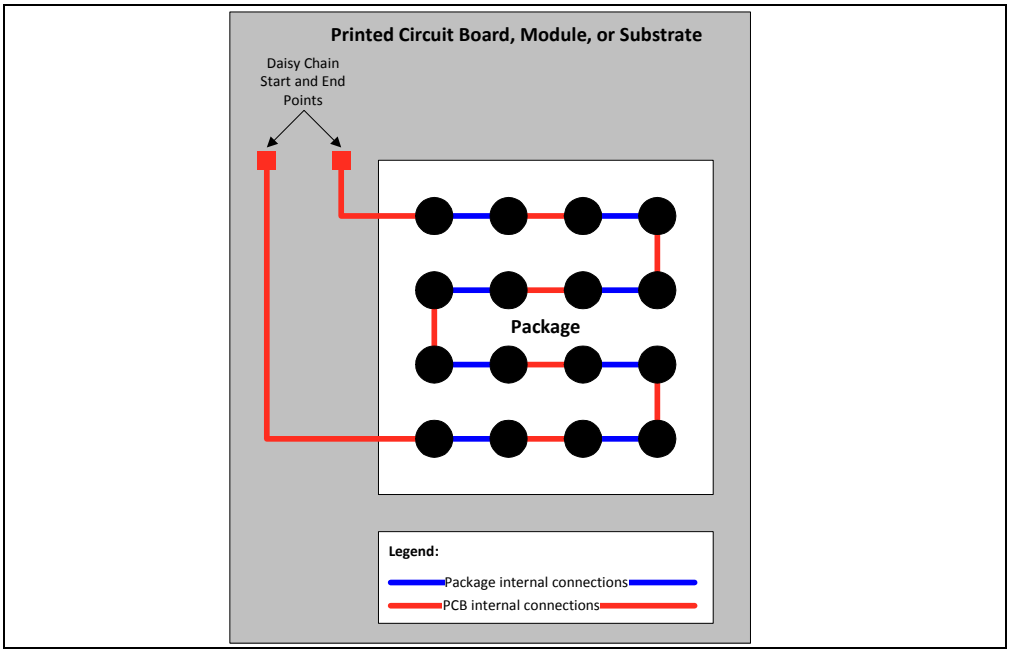


Figure 2. High-Level Schematic Daisy Chain Package and PCB Connectivity



4 Daisy Chain Construction

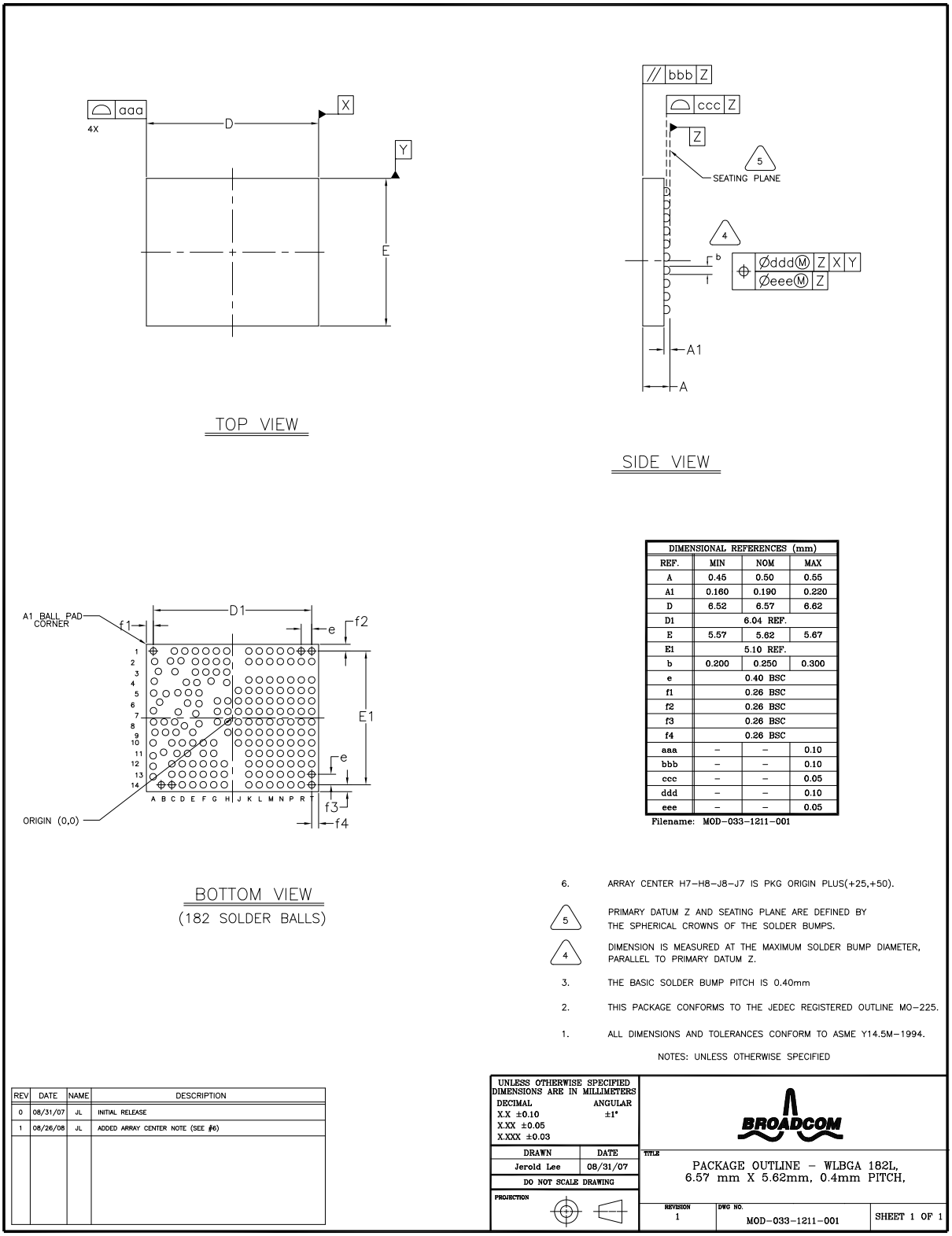
The daisy chain package is designed to match the form and fit of the corresponding product; the same manufacturing processes, materials, and dimensions are used for the associated product. Where minor exceptions occur, they are described in this document.

5 Package Overview

Table 2: Daisy Chain Package Overview

Package Type	WLBGA
Package body size	6.57 × 5.62 mm
Package ball count	182
Package ball pitch	0.4 mm
Package thickness	0.55 mm maximum

Figure 3. Daisy Chain Package Outline Drawing for CYW4329



DIMENSIONAL REFERENCES (mm)			
REF.	MIN	NOM	MAX
A	0.45	0.50	0.55
A1	0.160	0.190	0.220
D	6.52	6.57	6.62
D1		6.04 REF.	
E	5.57	5.62	5.67
E1		5.10 REF.	
b	0.200	0.250	0.300
e		0.40 BSC	
f1		0.26 BSC	
f2		0.26 BSC	
f3		0.26 BSC	
f4		0.26 BSC	
aaa	–	–	0.10
bbb	–	–	0.10
ccc	–	–	0.05
ddd	–	–	0.10
eee	–	–	0.05

Filename: MOD-033-1211-001

6. ARRAY CENTER H7–H8–J8–J7 IS PKG ORIGIN PLUS(+25,+50).

5. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BUMPS.

4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BUMP DIAMETER, PARALLEL TO PRIMARY DATUM Z.

3. THE BASIC SOLDER BUMP PITCH IS 0.40mm

2. THIS PACKAGE CONFORMS TO THE JEDEC REGISTERED OUTLINE MO–225.

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.

NOTES: UNLESS OTHERWISE SPECIFIED

REV	DATE	NAME	DESCRIPTION
0	08/31/07	JL	INITIAL RELEASE
1	08/26/08	JL	ADDED ARRAY CENTER NOTE (SEE #6)

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS	
DECIMAL	ANGULAR
X.X ±0.10	±1°
X.XX ±0.05	
X.XXX ±0.03	
DRAWN	DATE
Jerold Lee	08/31/07
DO NOT SCALE DRAWING	
PROJECTION	

BROADCOM

TITLE: PACKAGE OUTLINE – WLBGA 182L, 6.57 mm X 5.62mm, 0.4mm PITCH,

REVISION	DWG NO.	SHEET
1	MOD-033-1211-001	SHEET 1 OF 1

6 Package Differences

There are no construction, geometry, processes, or material differences between the CYW4329 daisy chain package and the CYW4329 product.

7 Daisy Chain Netlist

Table 3 shows the package netlist and daisy chain connectivity. The ball origin [0,0] is in the component center. X and Y ball coordinates are in microns.

Table 4 on page 6 shows the recommended printed circuit board (PCB) netlist. When combined with the package netlist, the connections result in a continuous daisy chain.

A different PCB netlist can be implemented to achieve the same overall continuous loop; however, subsequent changes to the component daisy chain netlist will be based on the PCB netlist in Table 4, and if this PCB netlist is not followed, then these component daisy chain changes may result in compatibility problems with a differently designed PCB.

Table 3: Daisy Chain Netlist and Connectivity

Ball #	Ball Name	X[a]	Y[a]		Ball #	Ball Name	X[a]	Y[a]
A1	WRF_VDDPAA_3P3	-3014.8	2549.9	>>	A2	WRF_GNDPAA_3P3	-2966.755	2152.48
A11	BT_RFOP	-3025	-1444	>>	A12	BT_VDDTF	-3025	-1844
A13	BT_VDDVCO	-3025	-2244	>>	B14	FM_VDDRX	-2713	-2550
A3	WRF_VDDTX_1P2	-2826.025	1774.125	>>	A4	WRF_RFINP_A1	-2981.95	1400.535
A5	WRF_RFINN_A1_XFMR	-3004.96	946.685	>>	B6	WRF_GNDRX_1P2	-2774.355	601.71
A7	WRF_RFINP_G1	-3010.84	276.485	>>	A8	WRF_RFINN_G1_XFMR	-3007.73	-153.575
A9	WRF_GNDCAB_1P2	-2953.695	-550	>>	A10	BT_VSSRF	-3025	-950
B11	BT_RFON	-2625	-1307	>>	C13	FM_TXN	-2313	-2150
B8	WRF_GNDD_1P2	-2605.665	-152.685	>>	B9	WRF_RES_EXT	-2550.98	-550
C1	WRF_RFOUTP_A	-2214.8	2549.9	>>	C2	WRF_GNDPAA_3P3	-2364.065	2170.495
C10	BT_VDDRF	-2313	-950	>>	C12	BT_VSSVCO	-2313	-1750
C11	BT_VDDIF	-2113	-1350	>>	D10	BT_VSSIF	-1913	-950
C14	FM_RXN	-2313	-2550	>>	D14	FM_RXP	-1913	-2550
C3	WRF_GNDTX_1P2	-2191.66	1761.185	>>	B5	WRF_VDDRX_1P2	-2530.785	925.875
C5	WRF_VDDLO_1P2	-2082.43	961.065	>>	C7	WRF_VDDA_1P2	-2066.785	227.09
C8	WRF_VDDD_1P2	-2203.525	-152.825	>>	C9	WRF_VDDPFDCP_1P2	-2149.895	-550.005
D1	WRF_VDDPAG_3P3	-1814.8	2549.9	>>	E1	WRF_RFOUTP_G	-1414.8	2549.9
D11	BT_VSSIFP	-1713	-1350	>>	F11	VSS_XTAL	-1113	-1350
D12	FM_VSSRX	-1913	-1750	>>	E12	FM_VSSVCO	-1513	-1750
D13	FM_TXP	-1913	-2150	>>	E13	FM_VDDVCO	-1513	-2150
D2	WRF_GNDPAG_3P3	-1963.8	2178.495	>>	D4	WRF_EXTCOUPLE_AIN	-1760.47	1357.67
D5	WRF_GNDLO_1P2	-1677.115	965.365	>>	E4	WRF_GPIO_OUT1	-1355.995	1349.9
D6	WRF_VDDVCO_1P2	-1713.505	565.275	>>	D8	WRF_GNDA_1P2	-1832.585	-303.85
D9	WRF_GNDPFDCP_1P2	-1512.295	-550	>>	E8	WRF_EXTREFIN	-1275.045	-222.135
E10	FM_VDDPLL	-1513	-950	>>	F10	FM_VSSPLL	-1113	-950
E14	FM_CVAR	-1513	-2550	>>	F14	OSCIN	-1113	-2550
E2	WRF_GNDPAG_3P3	-1414.8	2149.9	>>	F2	WRF_AFE_test_In	-1014.8	2149.9
E3	WRF_AFE_TSSI_G	-1414.8	1749.9	>>	F3	WRF_AFE_iqadc_VREF	-1014.8	1749.9
E5	WRF_GPIO_OUT2	-1275.045	952.96	>>	F4	WRF_BBPLL_VDD_1P2	-814.48	1402.28
E6	WRF_GNDVCO_1P2	-1275.045	546.615	>>	E7	WRF_VDDCAB_1P2	-1395.265	162.16
F1	WRF_AFE_test_Ip	-1014.8	2549.9	>>	G1	WRF_AFE_AVSS_RXADC	-614.8	2549.9
F12	VDD_XTAL	-1113	-1750	>>	G12	FM_ADOUT2	-713	-1750

Table 3: Daisy Chain Netlist and Connectivity (Continued.)

Ball #	Ball Name	X[a]	Y[a]		Ball #	Ball Name	X[a]	Y[a]
F13	OSCOUT	-1113	-2150	>>	G13	FM_ANAVSS	-713	-2150
G10	FM_BGNDLF	-713	-950	>>	J10	BT_COEX_OUT0	225	-950
G11	FM_TXADCVCM	-713	-1350	>>	K11	BT_GPIO_7	625	-1350
G14	FM_TXADCIN2	-713	-2550	>>	H14	FM_TXADCIN1	-313	-2550
G2	WRF_AFE_AVDD_RX ADC	-614.8	2149.9	>>	H2	WRF_AFE_test_on	-214.8	2149.9
G3	WRF_AFE_AVDD_AU X	-614.8	1749.9	>>	H3	WRF_AFE_TSSI_A	-214.8	1749.9
G6	BT_TM3	-575	650	>>	H6	RF_SW_CTRL_N_0	-175	650
G7	BT_GPIO_0	-575	250	>>	G8	VDD	-575	-150
H1	WRF_AFE_test_op	-214.8	2549.9	>>	K1	AMODE_TX_PU	625	2550
H12	FM_ADOUT1	-313	-1750	>>	K12	BT_COEX_OUT1	625	-1750
H13	FM_ANAVDD	-313	-2150	>>	K13	BT_GPIO_5	625	-2150
H4	WRF_BBPLL_GND_1 P2	-214.8	1349.9	>>	J5	RF_SW_CTRL_P_0	225	1050
H9	BT_RST_N	-175	-550	>>	J9	BT_TM0	225	-550
J6	BT_VDDO	225	650	>>	H7	BT_VDDO	-175	250
J8	BT_GPIO_2	225	-150	>>	K8	BT_TM1	625	-150
K10	BT_VSSC	625	-950	>>	L10	BT_PCM_SYNC	1025	-950
K14	BT_GPIO_6	625	-2550	>>	L14	BT_PCM_CLK	1025	-2550
K2	RF_SW_CTRL_N_3	625	2150	>>	L2	TMS	1025	2150
K4	GMODE_TX_PU	625	1450	>>	L4	TCK	1025	1450
K5	RF_SW_CTRL_P_1	625	1050	>>	L5	JTAG_TRST_L	1025	1050
K7	VDDIO_RF	625	250	>>	L7	VDDIO_RF	1025	250
K9	BT_GPIO_4	625	-550	>>	L9	BT_GPIO_3	1025	-550
L1	VDD	1025	2550	>>	M1	ERCX_STATUS	1425	2550
L11	BT_PCM_IN	1025	-1350	>>	M11	BT_UART_CTS_N	1425	-1350
L12	BT_VDDC	1025	-1750	>>	M12	BT_UART_RTS_N	1425	-1750
L13	BT_VSSC	1025	-2150	>>	M13	BT_UART_TXD	1425	-2150
L6	RF_SW_CTRL_P_3	1025	650	>>	M6	TDO	1425	650
M10	BT_VDDC	1425	-950	>>	M9	BT_PCM_OUT	1425	-550
M2	ERCX_RF_ACTIVE	1425	2150	>>	N2	WL_GPIO_2	1825	2150
M4	VSS	1425	1450	>>	N4	WL_GPIO_1	1825	1450
M5	WL_RST_N	1425	1050	>>	N5	WL_GPIO_0	1825	1050
M7	BT_SDA	1425	250	>>	M8	BT_SCL	1425	-150
N1	WL_GPIO_3	1825	2550	>>	P1	WL_GPIO_8	2225	2550
N10	VDD_LNLDO2	1825	-950	>>	N11	VOUT_LDO2	1825	-1350
N12	SR_TESTSWG	1825	-1750	>>	P12	SR_AVSS	2225	-1750
N13	SR_VDDBAT1	1825	-2150	>>	N14	SR_VDDBAT1	1825	-2550
N6	TDI	1825	650	>>	N7	TAP_SEL_0	1825	250
N8	BT_REG_ON	1825	-150	>>	N9	WL_REG_ON	1825	-550
P13	SR_PVSS	2225	-2150	>>	R13	SR_PVSS	2625	-2150
P14	SR_VLX1	2225	-2550	>>	R14	SR_VLX1	2625	-2550
P2	VDDIO	2225	2150	>>	R2	UART_TX_0	2625	2150
P4	OTP_VDD25	2225	1450	>>	P5	VSS	2225	1050
P6	sdio_cmd	2225	650	>>	P7	TAP_SEL_1	2225	250
P8	AVSS_LDO	2225	-150	>>	P9	VREF_LDO	2225	-550
R1	XTAL_PU	2625	2550	>>	T1	sdio_data_0	3025	2550
R10	SR_PALDO	2625	-950	>>	T10	SR_PALDO	3025	-950
R11	SR_VDDBAT3	2625	-1350	>>	T11	SR_VDDBAT3	3025	-1350

Table 3: Daisy Chain Netlist and Connectivity (Continued.)

Ball #	Ball Name	X[a]	Y[a]		Ball #	Ball Name	X[a]	Y[a]
R12	SR_VDDBAT2	2625	-1750	>>	T12	SR_AVDD2P5	3025	-1750
R4	UART_RX_0	2625	1450	>>	R5	VDDIO	2625	1050
R6	sdio_data_2	2625	650	>>	R7	sdio_data_3	2625	250
R8[b]	VDD_CLDO	2625	-150	>>	R9	VDD_LNLDO1	2625	-550
R8[b]	VDD_CLDO	2625	-150	>>	P11	SR_PAVSS	2225	-1350
T13	SR_VDDNLDO	3025	-2150	>>	T14	SR_VSSPLDO	3025	-2550
T2	sdio_clk	3025	2150	>>	T4	VDD	3025	1450
T5	VDDIO_SD	3025	1050	>>	T6	VDDIO_SD	3025	650
T7	sdio_data_1	3025	250	>>	T8	VOUT_CLDO	3025	-150

a. Ball coordinate, in microns

b. Ball R8 is shown connected to both P11 and R9. This is intentional.

Note: All coordinates are looking down on the package balls (dead bug).

Table 4 shows the recommended PCB netlist.

Table 4: Recommended PCB Netlist

Ball #	Ball Name		Ball #	Ball Name
A1	WRF_VDDPAA_3P3	>>	External daisy chain start	
M8	BT_SCL	>>	External daisy chain end	
A10	BT_VSSRF	>>	A11	BT_RFOP
A12	BT_VDDTF	>>	A13	BT_VDDVCO
A2	WRF_GNDPAA_3P3	>>	A3	WRF_VDDTX_1P2
A4	WRF_RFINP_A1	>>	A5	WRF_RFINN_A1_XFMR
A8	WRF_RFINN_G1_XFMR	>>	A9	WRF_GNDCAB_1P2
B14	FM_VDDRX	>>	C14	FM_RXN
B5	WRF_VDDRX_1P2	>>	B8	WRF_GNDD_1P2
B6	WRF_GNDRX_1P2	>>	A7	WRF_RFINP_G1
B9	WRF_RES_EXT	>>	B11	BT_RFON
C1	WRF_RFOUTP_A	>>	D1	WRF_VDDPAG_3P3
C11	BT_VDDIF	>>	D11	BT_VSSIFP
C12	BT_VSSVCO	>>	D12	FM_VSSRX
C13	FM_TXN	>>	D13	FM_TXP
C2	WRF_GNDPAA_3P3	>>	C3	WRF_GNDTX_1P2
C7	WRF_VDDA_1P2	>>	C8	WRF_VDDD_1P2
C9	WRF_VDDPFDCP_1P2	>>	C10	BT_VDDRF
D10	BT_VSSIF	>>	D8	WRF_GNDA_1P2
D14	FM_RXP	>>	E14	FM_CVAR
D4	WRF_EXTCOUPLE_AIN	>>	C5	WRF_VDDLO_1P2
D5	WRF_GNDLO_1P2	>>	D6	WRF_VDDVCO_1P2
D9	WRF_GNDPFDCP_1P2	>>	E10	FM_VDDPLL
E1	WRF_RFOUTP_G	>>	F1	WRF_AFE_test_lp
E12	FM_VSSVCO	>>	F12	VDD_XTAL
E13	FM_VDDVCO	>>	F13	OSCOUT
E2	WRF_GNDPAG_3P3	>>	D2	WRF_GNDPAG_3P3
E4	WRF_GPIO_OUT1	>>	E3	WRF_AFE_TSSI_G
E5	WRF_GPIO_OUT2	>>	E6	WRF_GNDVCO_1P2
E7	WRF_VDDCAB_1P2	>>	E8	WRF_EXTREFIN
F10	FM_VSSPLL	>>	G10	FM_BGNDLF

Table 4: Recommended PCB Netlist (Continued.)

Ball #	Ball Name		Ball #	Ball Name
F11	VSS_XTAL	>>	G11	FM_TXADCVCM
F14	OSCIN	>>	G14	FM_TXADCIN2
F2	WRF_AFE_test_In	>>	G2	WRF_AFE_AVDD_RXADC
F3	WRF_AFE_iqadc_VREF	>>	G3	WRF_AFE_AVDD_AUX
F4	WRF_BBPLL_VDD_1P2	>>	H4	WRF_BBPLL_GND_1P2
G1	WRF_AFE_AVSS_RXADC	>>	H1	WRF_AFE_test_op
G12	FM_ADOUT2	>>	H12	FM_ADOUT1
G13	FM_ANAVSS	>>	H13	FM_ANAVDD
G6	BT_TM3	>>	G7	BT_GPIO_0
G8	VDD	>>	H9	BT_RST_N
H14	FM_TXADCIN1	>>	K14	BT_GPIO_6
H2	WRF_AFE_test_on	>>	K2	RF_SW_CTRL_N_3
H3	WRF_AFE_TSSI_A	>>	K4	GMODE_TX_PU
H6	RF_SW_CTRL_N_0	>>	J6	BT_VDDO
H7	BT_VDDO	>>	J8	BT_GPIO_2
K8	BT_TM1	>>	K7	VDDIO_RF
L7	VDDIO_RF	>>	L6	RF_SW_CTRL_P_3
J10	BT_COEX_OUT0	>>	K10	BT_VSSC
J5	RF_SW_CTRL_P_0	>>	K5	RF_SW_CTRL_P_1
J9	BT_TM0	>>	K9	BT_GPIO_4
K1	AMODE_TX_PU	>>	L1	VDD
K11	BT_GPIO_7	>>	L11	BT_PCM_IN
K12	BT_COEX_OUT1	>>	L12	BT_VDDC
K13	BT_GPIO_5	>>	L13	BT_VSSC
L9	BT_GPIO_3	>>	L10	BT_PCM_SYNC
M9	BT_PCM_OUT	>>	N9	WL_REG_ON
M11	BT_UART_CTS_N	>>	M10	BT_VDDC
N10	VDD_LNLDO2	>>	P9	VREF_LDO
M12	BT_UART_RTS_N	>>	N11	VOUT_LDO2
M13	BT_UART_TXD	>>	N12	SR_TESTSWG
L14	BT_PCM_CLK	>>	N14	SR_VDDBAT1
P12[a]	SR_AVSS	>>	P11	SR_PAVSS
P12[a]	SR_AVSS	>>	R9	VDD_LNLDO1
R10	SR_PALDO	>>	R11	SR_VDDBAT3
N13	SR_VDDBAT1	>>	P14	SR_VLX1
T8	VOUT_CLDO	>>	T10	SR_PALDO
T11	SR_VDDBAT3	>>	T12	SR_AVDD2P5
P13	SR_PVSS	>>	R12	SR_VDDBAT2
R13	SR_PVSS	>>	T13	SR_VDDNLDO
R14	SR_VLX1	>>	T14	SR_VSSPLDO
L2	TMS	>>	M2	ERCX_RF_ACTIVE
L4	TCK	>>	M4	VSS
L5	JTAG_TRST_L	>>	M5	WL_RST_N
M1	ERCX_STATUS	>>	N1	WL_GPIO_3
M6	TDO	>>	M7	BT_SDA
N2	WL_GPIO_2	>>	P2	VDDIO
N4	WL_GPIO_1	>>	P4	OTP_VDD25
N5	WL_GPIO_0	>>	N6	TDI
N7	TAP_SEL_0	>>	N8	BT_REG_ON

Table 4: Recommended PCB Netlist (Continued.)

Ball #	Ball Name		Ball #	Ball Name
P1	WL_GPIO_8	>>	R1	XTAL_PU
P5	VSS	>>	P6	sdio_cmd
P7	TAP_SEL_1	>>	P8	AVSS_LDO
R2	UART_TX_0	>>	R4	UART_RX_0
R5	VDDIO	>>	R6	sdio_data_2
R7	sdio_data_3	>>	R8	VDD_CLDO
T1	sdio_data_0	>>	T2	sdio_clk
T4	VDD	>>	T5	VDDIO_SD
T6	VDDIO_SD	>>	T7	sdio_data_1

a. Ball P12 is shown connected to both P11 and R9. This is intentional.

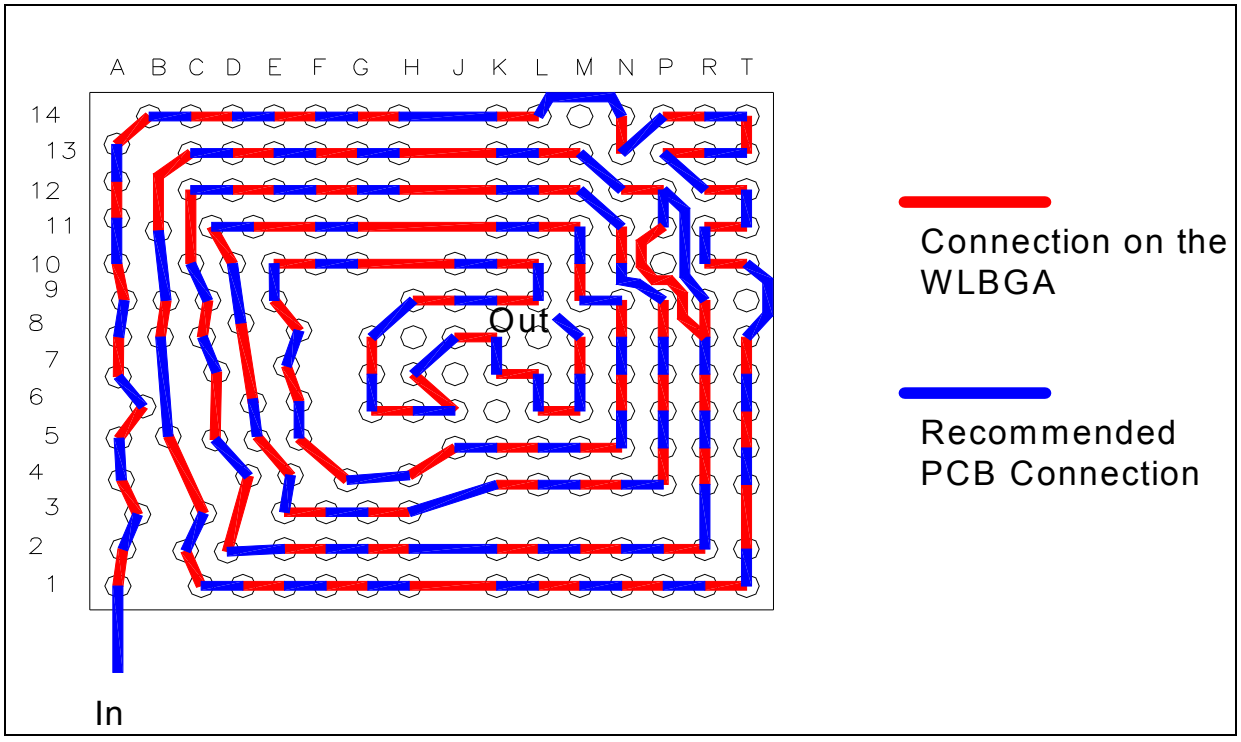
The balls listed in Table 5 are not connected in the daisy chain. These balls should be NC on the PCB.

Table 5: Balls Not Connected in Daisy Chain

Ball #	Ball Name
K6	RF_SW_CTRL_N_1
J7	VSS
L8	BT_TM6
H8	BT_GPIO_1
M14	BT_UART_RXD
T9	VOUT_LNLDO1
P10	SR_PNPO

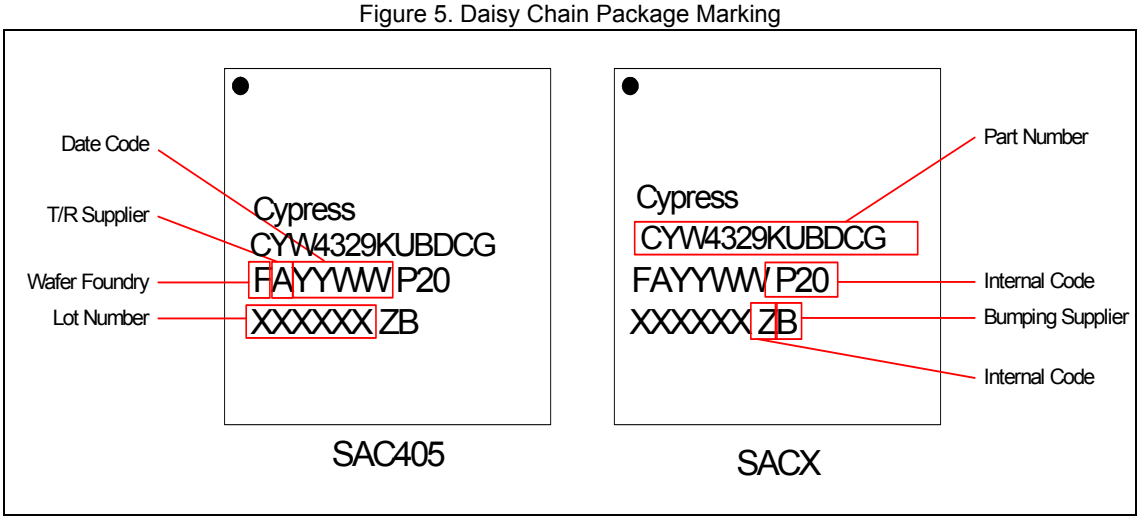
Figure 8 shows a schematic view of the CYW4329 daisy chain.

Figure 4. Schematic View of the CYW4329 Daisy Chain (PCB View)



8 Daisy Chain Package Marking

Figure 5. Daisy Chain Package Marking



8.1 Package Marking Field Description

Multiple suppliers are listed in Table 6, but all suppliers listed may not be used for this part.

Table 6: Package and Supplier Codes

Field	Field Meaning	Supplier	Supplier Code
F	Wafer foundry	TSMC	T
		CHRT	C
		SMIC	H
		UMC	U
		N/A	Z[a]
A	T/R supplier	UTAC	D
		STATS	T
		ASE	E
		SPIL	N
YYWW	Date code	N/A	YY = Year: WW = Work Week
P20	Internal code	N/A	N/A
B	Bumping supplier	TSMC	T
		SPIL	N
		ASE	E
		Nepes	F
		SMIC	H
		STATS	S
		Amkor	A
Z	Internal code	N/A	N/A

a. In many daisy chain components, there is no fab-dependent content. If the fab code = Z, then the daisy chain component is fully manufactured by the assembly/bumping supplier.

9 Daisy Chain Part Variations

Table 7: Daisy Chain Part Variations

Part Number	Notes	Package Marking	Assembly House
BCM4329SDCB0NKUBG	Solder=SACX	BCM4329SKUBDCG ZNYYWW P20	SPIL
BCM4329DCB0NKUBG	Solder=SAC405	BCM4329KUBDCG ZNYYWW P20	SPIL
BCM4329SDCB0EKUBG	Solder=SACX	BCM4329SKUBDCG ZEYYWW P20	ASE
BCM4329DCB0EKUBG	Solder=SAC405	BCM4329KUBDCG ZEYYWW P20	ASE
BCM4329SDCB0TKUBG	Solder=SACX	BCM4329SKUBDCG ZTYYWW P20	TSMC
BCM4329DCB0TKUBG	Solder=SAC405	BCM4329KUBDCG ZTYYWW P20	TSMC

10 Application Notes

Various package types have application notes associated with them; the appropriate application note should be reviewed prior to design and manufacturing. Application notes are available on docSAFE or from the Cypress sales, marketing, and field application engineers departments.

When retrieving documents from docSAFE, replace the “vv” in the document number with the largest number available in the repository to ensure access to the most current version of the document.

Table 8: Package-Specific Application Notes

Package Type	Document Number	Description
WLCSP	PACKAGING-AN3vv-R	Wafer-scale chip-sized package (WSCSP) overview and assembly guidelines.
WLBGA	PACKAGING-AN6vv-R	Wafer-level ball grid array (WLBGA) overview and assembly guidelines.
FBGA, PBGA, and other laminate-based BGA variants	PACKAGING-AN1vv-R	Reflow process guidelines for surface mount assemblies. Printed circuit board land pattern recommendations for ball grid array.
	PACKAGING-AN5vv-R	

Document History Page

Document Title: AN214926 - CYW4329 WLBGA Daisy Chain Package Document Number: 002-14926				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	-	-	03/26/2010	4329-AN500-R Initial release
*A	5454051	UTSV	09/30/2016	Updated in Cypress template
*B	5877746	AESATMP9	09/11/2017	Updated logo and copyright.

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturers' representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709