AN214923

Power Topologies and Regulator Component Guide

Associated Part Family: CYW4325

This application note documents the regulator resources provided by the CYW4325 and provides details on the various power topologies available to optimally match these resources with the requirements of the target host system. The application note addresses the production version of the CYW4325.

Contents

1 About This Document

1.1 Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM4325	CYW4325

1.2 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary.

2 IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

3 Introduction

The CYW4325 has been designed to meet the varied and demanding requirements of embedded systems such as cellular and smart phones, music players, game devices, and other mobile systems. These systems require a WLAN/Bluetooth® solution that has low power consumption, low cost, and a small foot print. The systems can also vary widely in the power supply rails they have available to the WLAN/Bluetooth subsystem.

The CYW4325 addresses these requirements by providing a comprehensive set of integrated switching and linear regulators. All of the regulators are independent and have their inputs and outputs brought out to pins on the CYW4325. This functionality enables each regulator to be used or bypassed to optimally match the resources and needs of the target system.

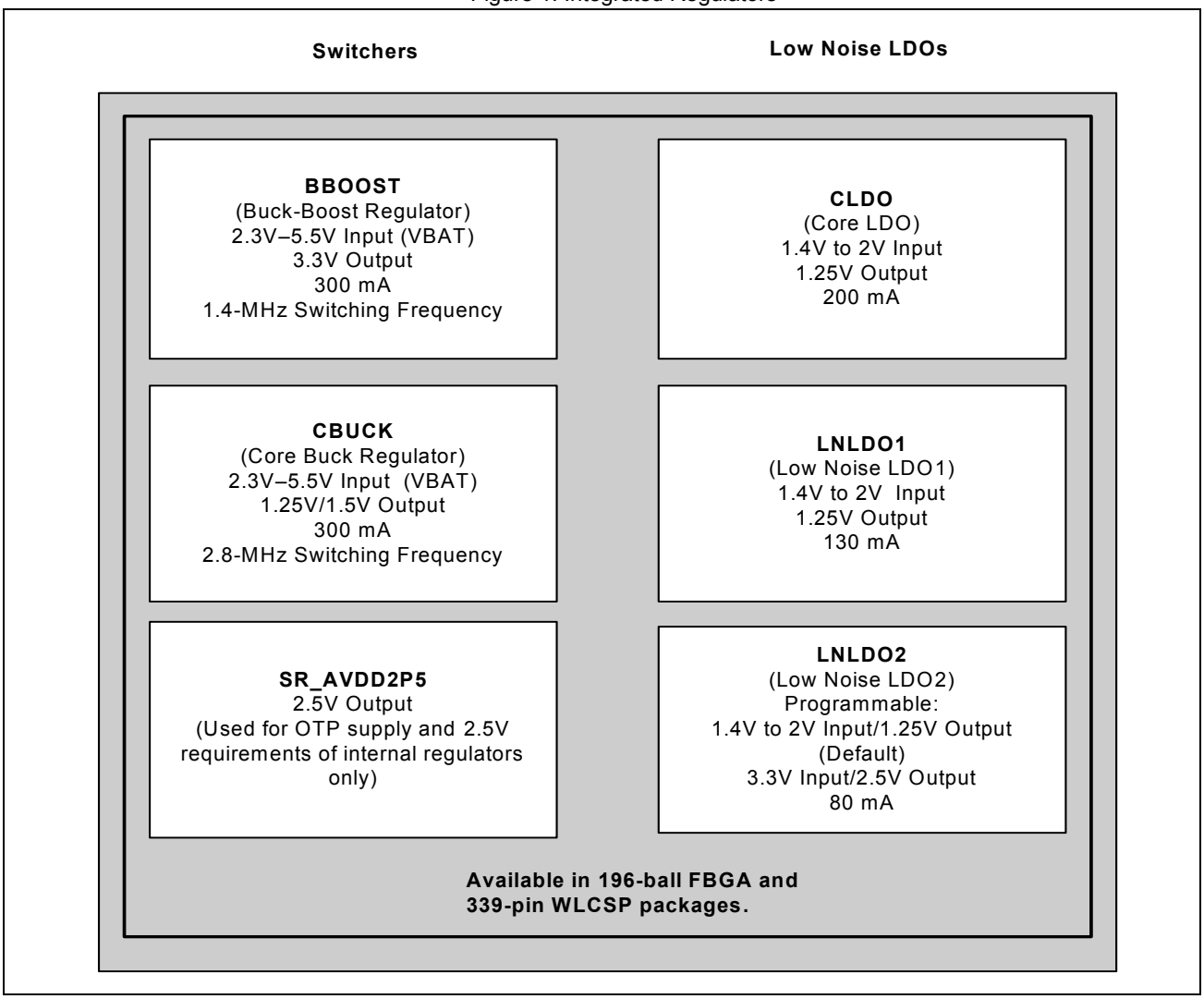
For example, if a system has only VBAT (battery voltage, 2.3V to 5.5V) available for the CYW4325, a combination of integrated CYW4325 regulators can be used to provide all of the voltages needed by the WLAN/Bluetooth subsystem, all of which are derived from VBAT. Conversely, if a system already has a 3.3V and 1.25V rail available to the CYW4325, then most of the CYW4325 regulators can be bypassed and the host-supplied rails can be used directly. This technique allows the number of external components in the CYW4325 circuit to be reduced.

This application note documents the regulator resources provided by the CYW4325 and provides details on the various power topologies available to optimally match these resources with the requirements of the target host system. The application note addresses the production version of the CYW4325.

4 CYW4325 Integrated Regulators

Figure 1 illustrates the CYW4325 integrated regulators. Integrated regulators include the CBUCK and BBOOST (buck-boost) switchers. Linear regulators include: CLDO, LNLDO1, and LNLDO2. There is also an additional 2.5V LDO (SR_AVDD2P5) that is dedicated to supplying the 2.5V rail required by the CBUCK and BBOOST switching regulators. It is also used to supply 2.5V to the CYW4325 OTP block. The inputs and outputs of the regulators are both brought out to CYW4325 pins, allowing the designer to use or bypass the regulators as is appropriate for the target platform. If a linear regulator (such as LNLDO2) is not used, its input pins should be grounded and its output pins should be left floating. If a switcher is not used, its inputs should be connected to VBAT/3.3V. Its outputs should be left floating. If the CBUCK regulator is not used, the **sr_vfb1** input should be connected to ground. Also note that on the WLCSP package, there are pins for an additional unsupported regulator. Refer to the CYW4325 data sheet for more detailed regulator specifications. Also note that if CBUCK is not used, then there needs to be a 4.7-µF input capacitor near the inputs of CLDO and LNLDO1. The external power supply trace that feeds these regulators should have an ESR of less than 50 mohms.

Figure 1. Integrated Regulators



5 CYW4325 Power Supply Requirements

The CYW4325 requires the following voltages to operate: 3.3V, 2.5V, 1.25V and VDDIO (I/O power supply).

5.1 3.3V Supply

The 3.3V rail is used primarily for the integrated WLAN power amplifier. It is also used for the VDDIO_RF pins, which are explained later in more detail. This supply could also be used for the generic VDDIO and VDDIO_SD supplies if the host uses 3.3V signaling. Finally, it is typically used as the power source for LNLDO2 when LNLDO2 is used to generate 2.5V. If 3.3V is supplied externally (BBOOST not used), the supply should be capable of supporting 300-mA loads (with 400-mA peaks with durations of several milliseconds).

5.2 2.5V Supply

The CYW4325 requires a 2.5V supply for its OTP (One-Time Programmable memory) block. This 2.5V supply is generally derived using the CYW4325 on-chip SR_AVDD2P5 regulator, so an external 2.5V supply is not required. Note that the SR_AVDD2P5 regulator is strictly used for OTP and the CYW4325 switching regulators. It has limited current capability and is not available for other uses. Depending on the application requirements regarding FM and higher output power Class 1 Bluetooth, an external 2.5V supply (80 mA) might be required for the Bluetooth PA. For more details, see FM and Bluetooth PA Supply Choices on page 4.

5.3 1.25V Supplies

Two types of 1.25V supplies are required. The first is a basic 1.25V supply, which is used to provide power to the digital logic portions of the CYW4325. It also provides power to the noise-insensitive blocks in the CYW4325 radio blocks. The second 1.25V supply must be a clean filtered supply, as it provides power to the noise-sensitive blocks (in the CYW4325) such as the radios, AFEs, LNAs, and clock circuits. If FM is required by the system, then an additional filtered 1.25V rail is required for the FM circuitry. This separate supply is required for optimal FM performance. For more details, see FM and Bluetooth PA Supply Choices on page 4. If 1.25V is provided externally (CLDO, LNLDO1, and so on, are not used), the external supply should be capable of 300-mA loads.

5.4 VDDIO Supplies

There are three types of VDDIO (I/O power supplies) in the CYW4325. The first, which is generally labeled VDDIO, is for the generic digital I/Os in the chip. This covers most of the I/Os including the GPIOs, reset lines, and so on. The second I/O supply is the VDDIO_SD supply. This supply provides power just to the SDIO/SPI interfaces I/O pads. Finally, the VDDIO_RF supply provides power to the I/Os that control external RF components such as the 3PST RF switch used to select which RF function (Bluetooth transmit, WLAN transmit, BT/WLAN receive) is connected to the antenna. These three separate I/O supplies give the CYW4325 additional flexibility in adapting to a given system. For example, generic I/Os could use 1.8V signaling, whereas the SDIO interface could function at 3.3V. The most common configuration is likely to be 1.8V signaling for the generic I/Os and SDIO interface (VDDIO and VDDIO_SD), with 3.3V signaling for the VDDIO_RF I/Os. This configuration is the most common because most RF switches do not support control voltages as low as 1.8V. Refer to the CYW4325 data sheet for a detailed list of which supply domain (VDDIO, VDDIO_SD, VDDIO_RF) each I/O belongs to. Total I/O currents are less than 10 mA.

Note: The currents listed above are conservative values that are intended for sizing power supplies. They are not appropriate for battery life estimation as they do not represent the lower typical currents seen in normal or low-power operation. Contact your Cypress representative for the latest current consumption numbers appropriate for battery life estimation.

6 FM and Bluetooth PA Supply Choices

If FM is required in a target design, the FM circuitry needs a dedicated filtered 1.25V supply for optimal performance. Cypress recommends using LNLDO2 (configured by software for 1.25V output) for this purpose.

If FM is not required in a design, the FM pins should be configured as follows:

- No bypass capacitors are required if FM is not used.
- All FM ground pins should be connected to ground.
- All FM supply pins should be connected to 1.25V. This supply does *not* need to be a dedicated filtered 1.25V supply because the FM will not be functional. Consequently, LNLDO2 can be left for other uses such as for the Bluetooth PA supply, and an already existing shared 1.25V can be used for the FM supply pins.
- All other FM pins will be left floating (NO_CONNECT).

There are two options for the Bluetooth PA. For Class 2 operation, the Bluetooth PA supply (BT_VDDTF) is connected to 1.25V. If the CBUCK regulator is being used, then Cypress recommends using a filtered version of the CBUCK 1.5V output for BT_VDDTF. This will provide additional output power in Class 2 mode. For higher output power Class 1 Bluetooth operation (typically, 6 dBm at CYW4325 output) the BT_VDDTF pin is connected to a 2.5V supply. If FM is *not* being used in the design, then LNLDO2 can be configured under software control for 2.5V output and used to supply the BT_VDDTF pin. Conversely, if FM is required, then LNLDO2 will be needed for the 1.25V FM supply, and an external 2.5V supply (80 mA) will be needed for the Bluetooth PA Supply (BT_VDDTF).

Note that when LNDLO2 is used as a 2.5V supply, its input will be connected to 3.3V. When it is used as a 1.25V supply, the input voltage must be lowered. If the design is using the CYW4325 CBUCK regulator, the ideal approach is to connect the LNLDO2 input to the output of the CBUCK (1.5V).

7 Initializing the LNLDO2 Regulator

The LNLDO2 regulator is controlled by the Bluetooth core via a configuration file. By default, LNLDO2 is set for 1.25V output and is DISABLED. The Bluetooth configuration file must program the LNLDO2 output to be either 1.25V or 2.5V (depending on if it will be used for FM or for Class 1 Bluetooth). After that, it needs to enable LNLDO2.

8 Power Topologies

8.1 Power Topology 1: VBAT with FM and Class 1 Bluetooth

In this power topology (see Figure 2 and Figure 3), the host provides VBAT (2.3V to 5.5V), 2.5V, and VDDIO (typically 1.8V). The topology uses the CYW4325 CBUCK, BBOOST, CLDO, LNLDO1, and LNLDO2 regulators to generate all other voltages. This topology is targeted at systems that do not have 3.3V or 1.25V regulated supplies that are available for the CYW4325 to use. It provides the best possible efficiency for such systems. The trade-off to this approach is that it requires a larger number of external components such as inductors for the two switchers. This topology also assumes that the application needs FM support and higher output power Class 1 Bluetooth. LNLDO2 is used in 1.25V output mode for the FM core. An external 2.5V supply (80-mA) is required for the Bluetooth PA supply.

Figure 2. Power Topology 1 Block Diagram

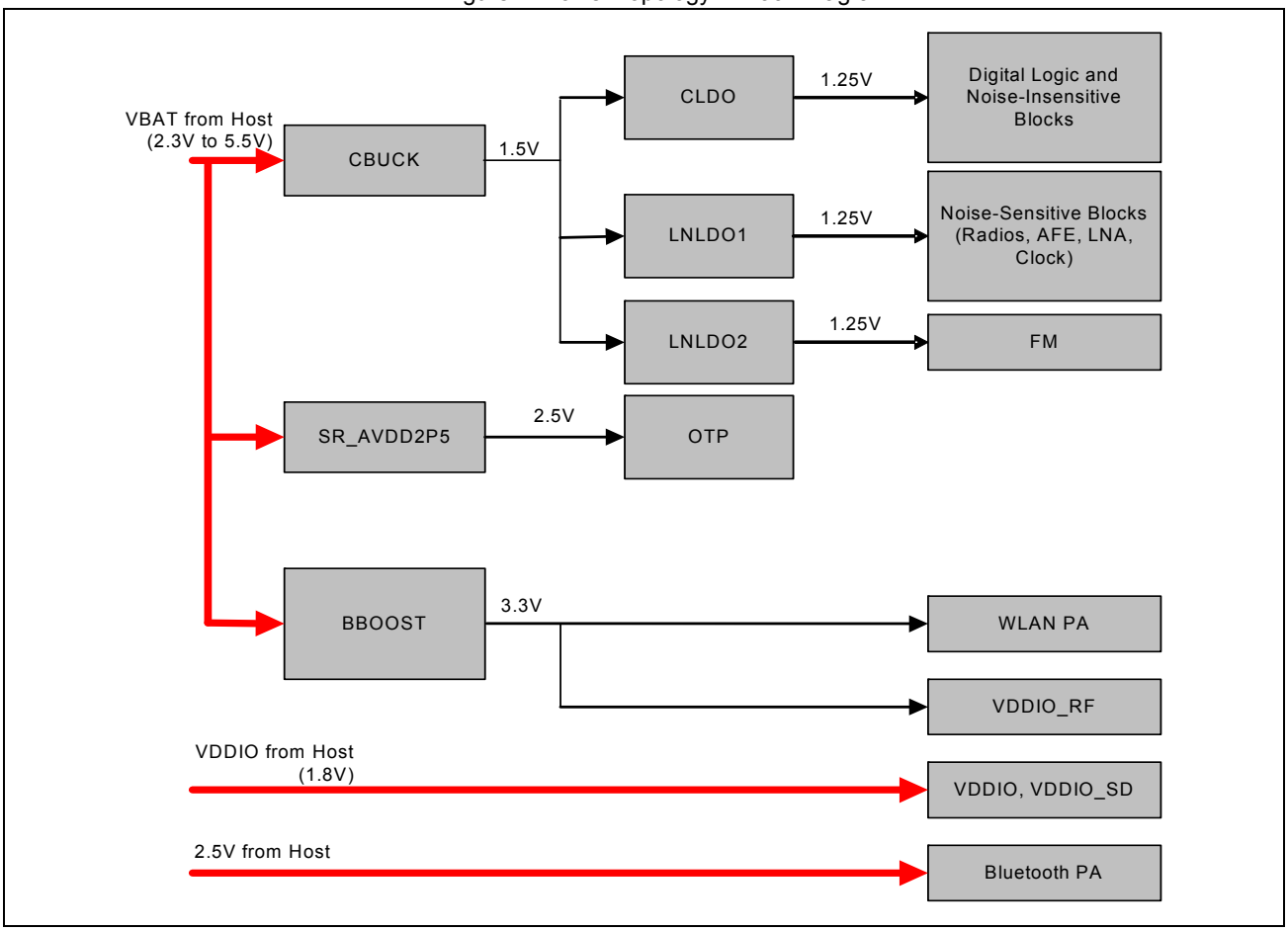
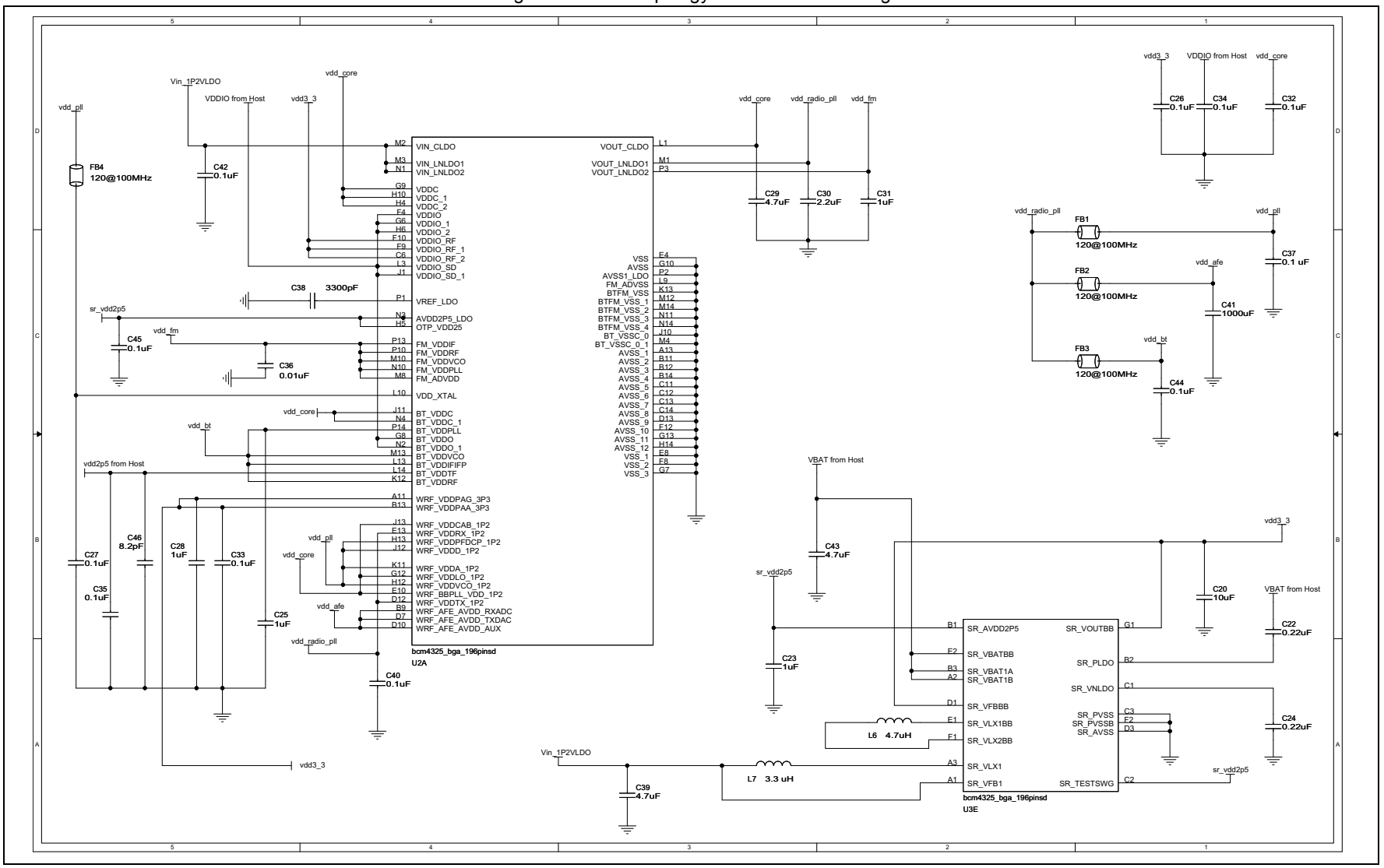


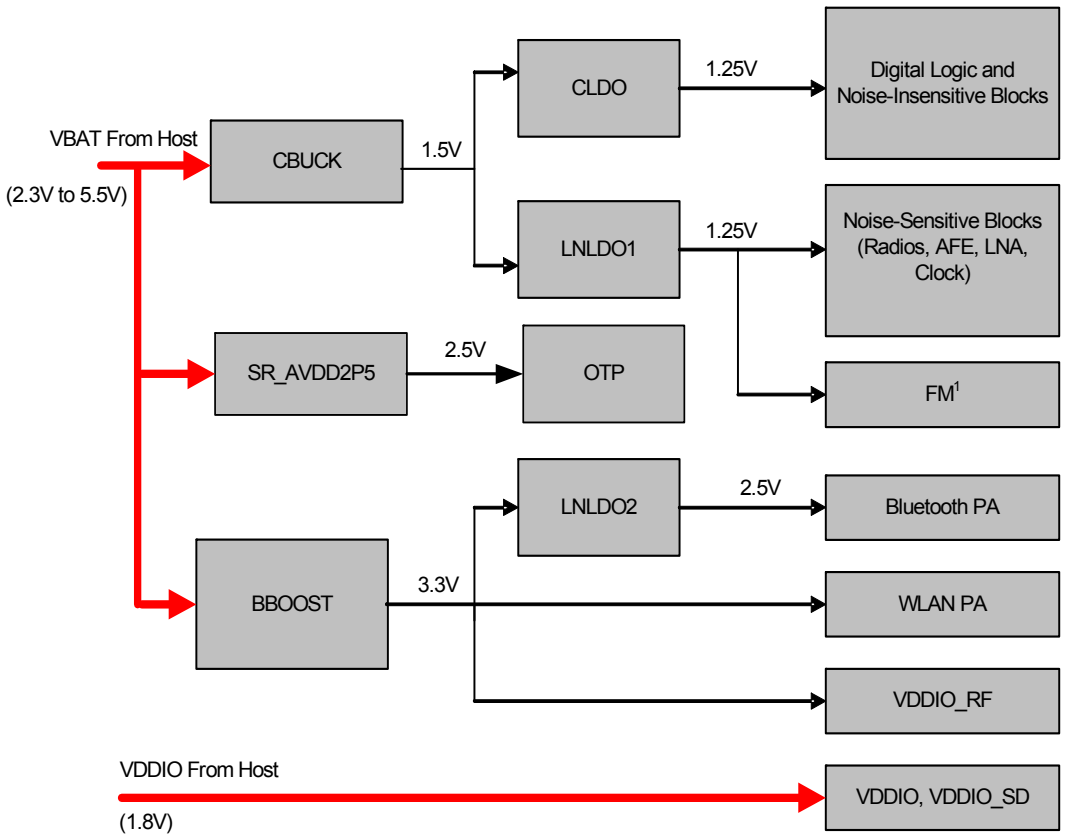
Figure 3. Power Topology 1 Schematic Drawing



8.2 Power Topology 2: VBAT with Class 1 Bluetooth, No FM

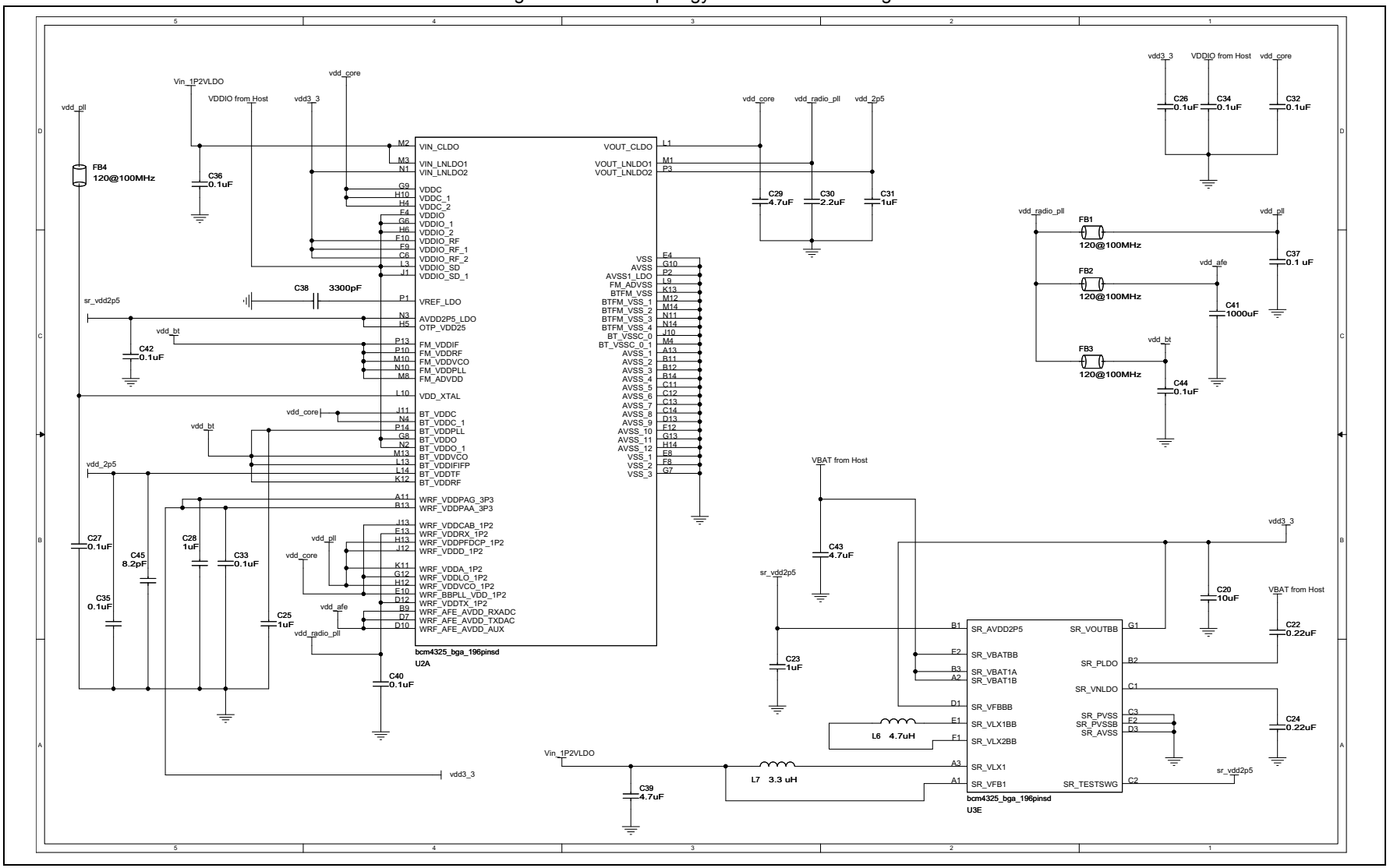
In this power topology (see Figure 4 and Figure 5), the host provides only VBAT (2.3V to 5.5V) and VDDIO (typically 1.8V). The topology uses the CYW4325 CBUCK, BBOOST, CLDO, LNLDO1, and LNLDO2 regulators to generate all other voltages. This topology is targeted at systems that do not have 3.3V or 1.25V regulated supplies that are available for the CYW4325 to use. It provides the best possible efficiency for such systems. The trade-off to this approach is that it requires a larger number of external components, such as inductors, for the two switchers. This topology also assumes that the application does *not* need FM. Because of the absence of FM operation, LNLDO2 can be used in 2.5V output mode to support Class 1 Bluetooth operation.

Figure 4. Power Topology 2 Block Diagram



1. The FM block must have power and ground connected even when it is *not* used. Other FM pins can be NO_CONNECTS.

Figure 5. Power Topology 2 Schematic Drawing



8.3 Power Topology 3: VBAT with FM and Class 2 Bluetooth

In this power topology (see Figure 6 and Figure 7), the host provides only VBAT (2.3V to 5.5V) and VDDIO (typically 1.8V). The topology uses the CYW4325 CBUCK, BBOOST, CLDO, LNLDO1, and LNLDO2 regulators to generate all other voltages. This topology is targeted at systems that do not have 3.3V or 1.25V regulated supplies that are available for the CYW4325 to use. It provides the best possible efficiency for such systems. The trade-off to this approach is that it requires a larger number of external components, such as inductors for the two switchers. This topology also assumes that the application needs FM support. LNLDO2 provides 1.25V for the FM core. If the CBUCK regulator is being used, then Cypress recommends using a filtered version of the CBUCK 1.5V output for BT_VDDTF. This will provide additional output power in Bluetooth Class 2 mode.

Figure 6. Power Topology 3 Block Diagram

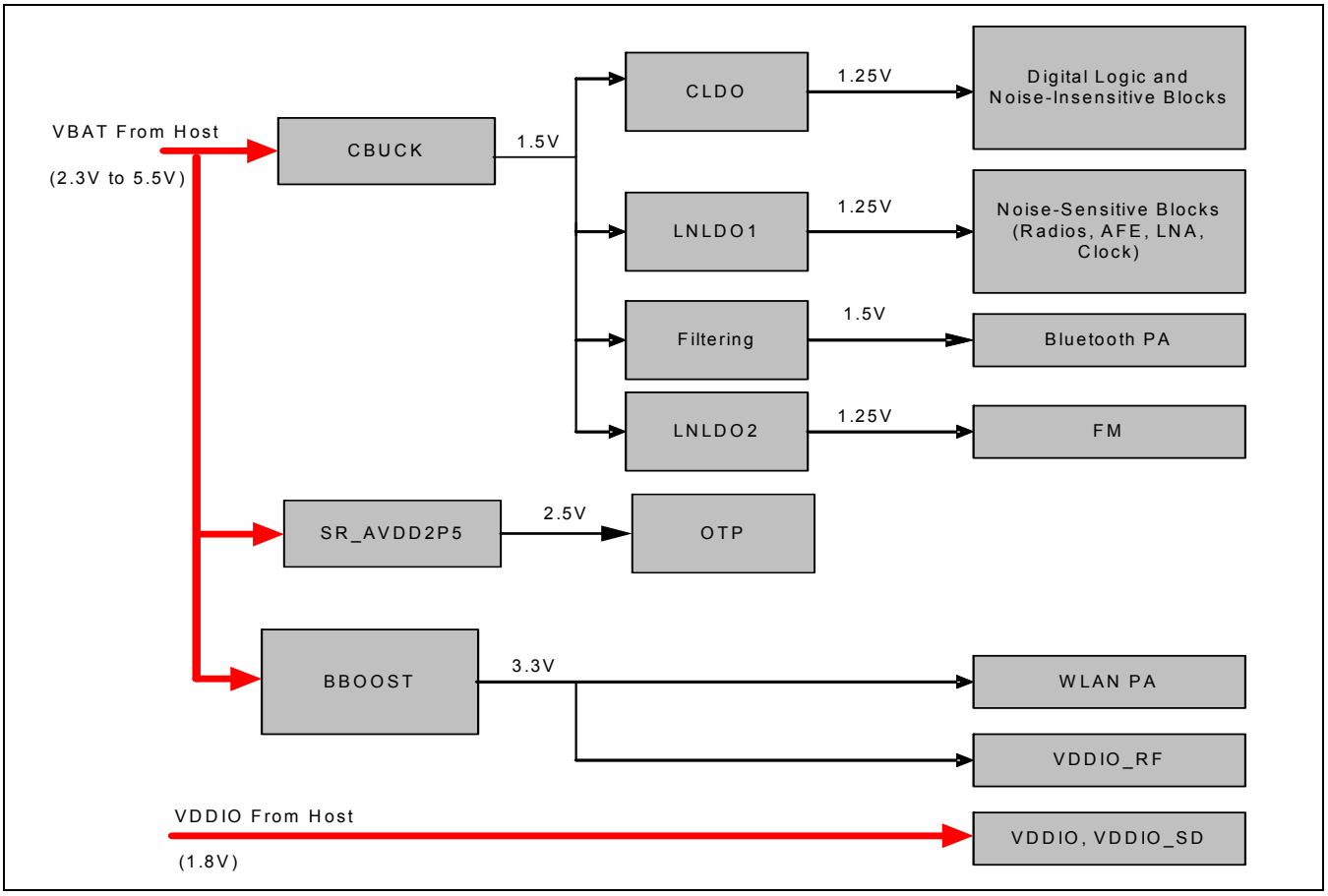
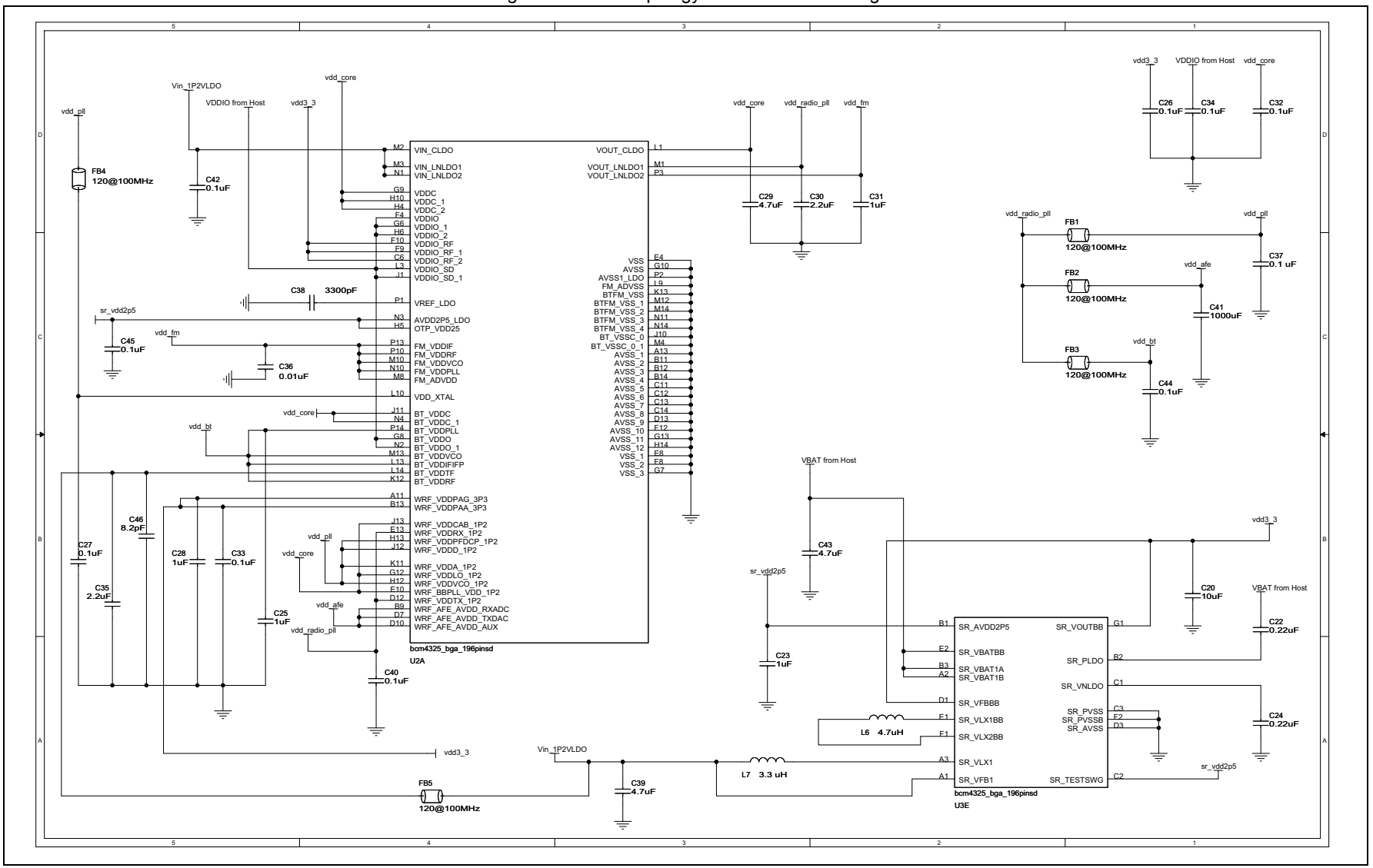


Figure 7. Power Topology 3 Schematic Drawing



8.4 Power Topology 4: Host Provides 3.3V, FM, and Class 2 Bluetooth Support

In this power topology (see Figure 8 and Figure 9), the host provides only 3.3V and VDDIO (typically 1.8V). The topology uses the CYW4325 CBUCK, CLDO, LNLDO1, and LNLDO2 regulators to generate all other voltages. This topology is targeted at systems that have a regulated 3.3V rail with sufficient current allocated for the CYW4325 (direct support of VBAT is not required). The CYW4325 provides 2.5V and 1.25V regulated supplies using its integrated regulators. This topology provides high efficiency and has fewer external components than Topology 3. The topology assumes FM support, but only Class 2 Bluetooth support. If the CBUCK regulator is being used, then Cypress recommends using a filtered version of the CBUCK 1.5V output for BT_VDDTF. This will provide additional output power in Bluetooth Class 2 mode. There is another variation of this topology for applications where the 3.3V supply of the host does not have enough load capacity to supply both the CBUCK and WLAN PA. In this case, an alternate topology could be used where the 3.3V supply of the host is used for the WLAN PA and VBAT is used to supply CBUCK.

Figure 8. Power Topology 4 Block Diagram

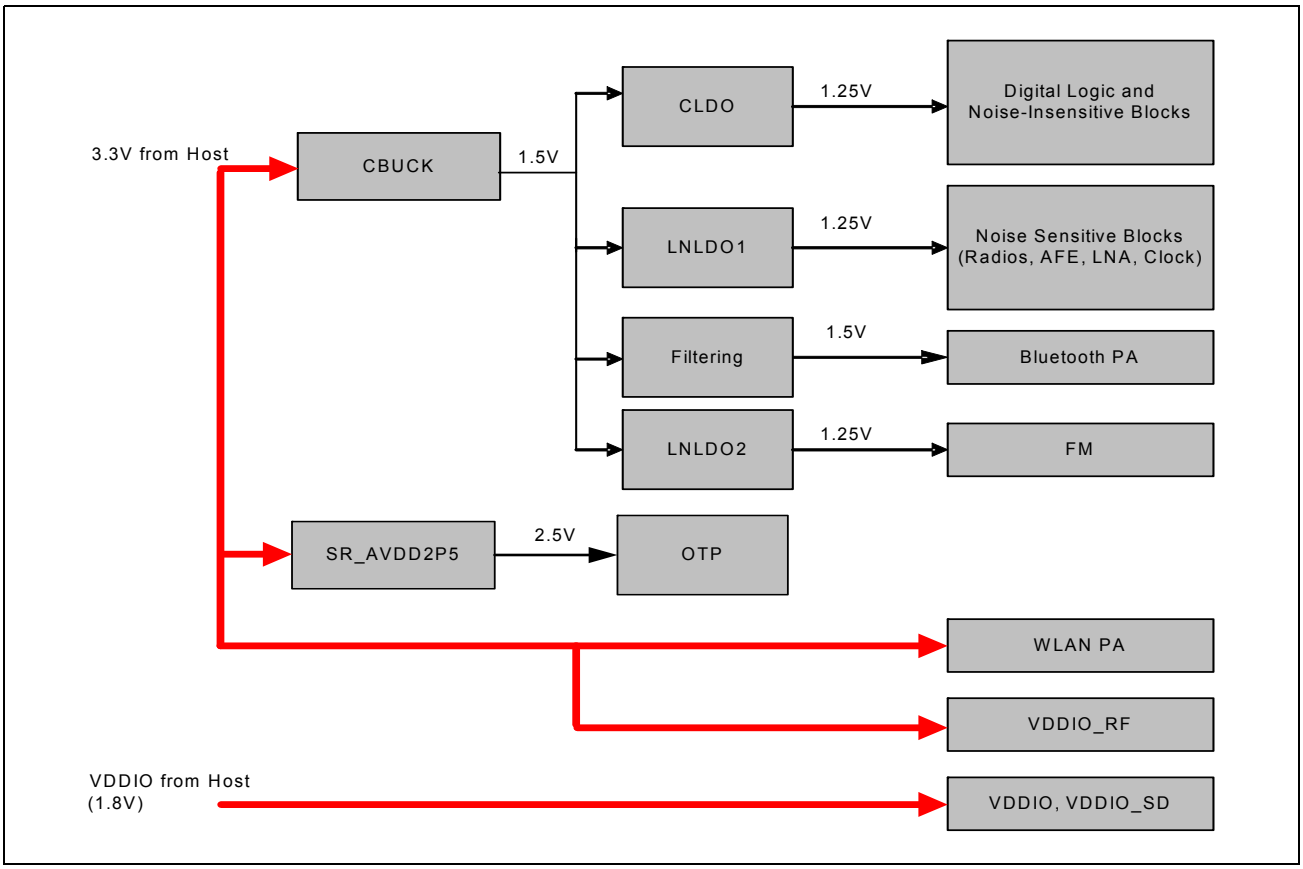
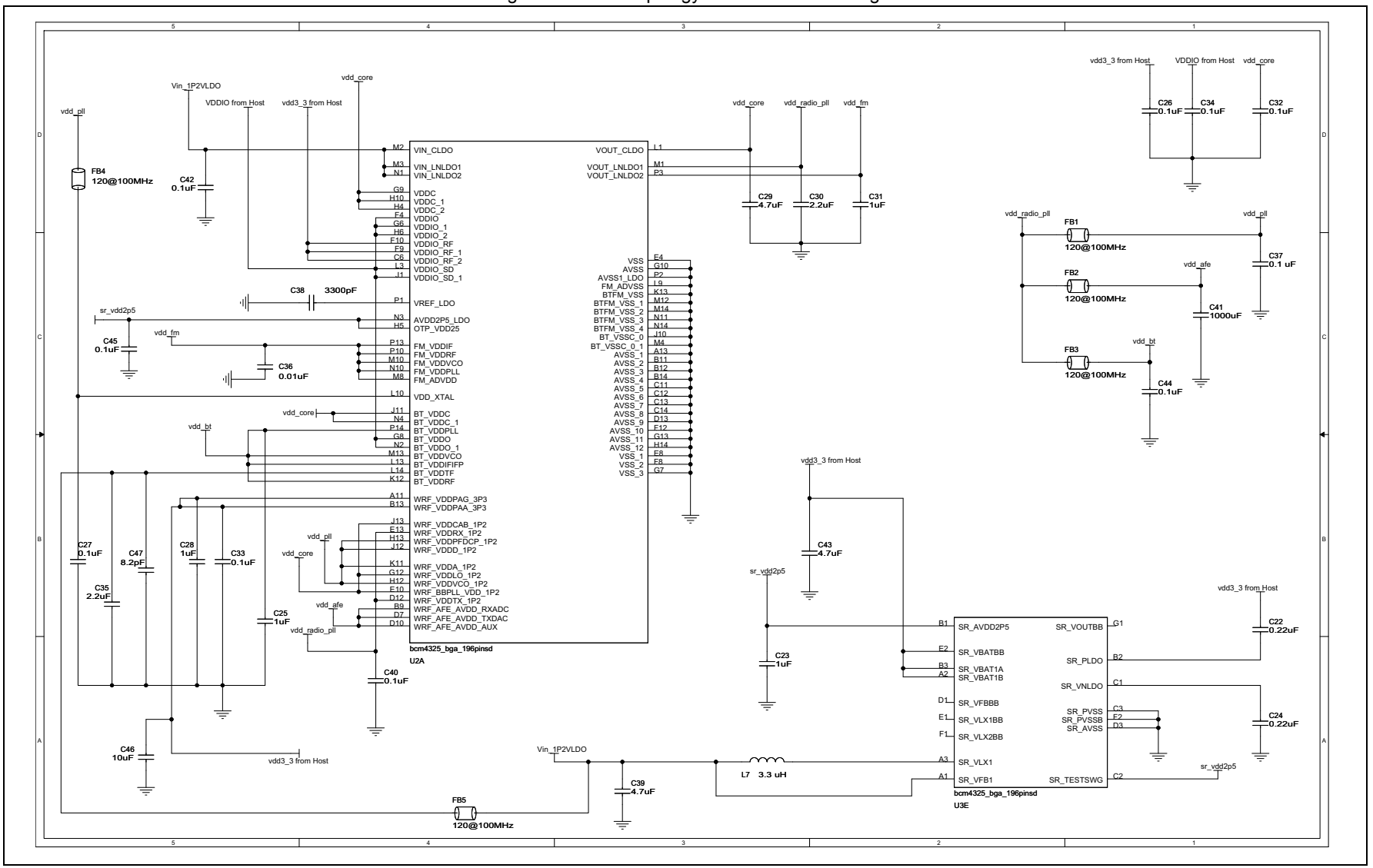


Figure 9. Power Topology 4 Schematic Drawing



8.5 Power Topology 5: Host Provides 3.3V and 1.8V, FM, and Class 2 Bluetooth Support

In this power topology (see Figure 10 and Figure 11), the host provides regulated 3.3V and 1.8V supplies. The 1.8V rail, however, is not just for VDDIO. It also has enough current to directly feed the CYW43251.25V LDO inputs. This capability results in a reduction of external components as the CYW4325 CBUCK regulator is no longer used. The trade-off for this approach is that it will be less efficient than Topology 2 because the voltage drop from 1.8V to 1.25V is handled completely by linear regulators. This functionality is in contrast to Topologies 1–4, in which the CBUCK outputs 1.5V, and the less efficient LDOs only have to drop the voltage from 1.5V to 1.25V. This topology assumes FM support but only Class 2 Bluetooth support.

Also note that, as an example, this topology uses a 1.8V host supply as the input for the CLDO, LNLDO1, and LNLDO2 regulators. However, these regulator support a range of input voltages. As long as it has enough current available, a host supply rail at any voltage from 1.4V to 2V could be used to feed these regulators. Lower voltages have the benefit of improved efficiency.

Figure 10. Power Topology 5 Block Diagram

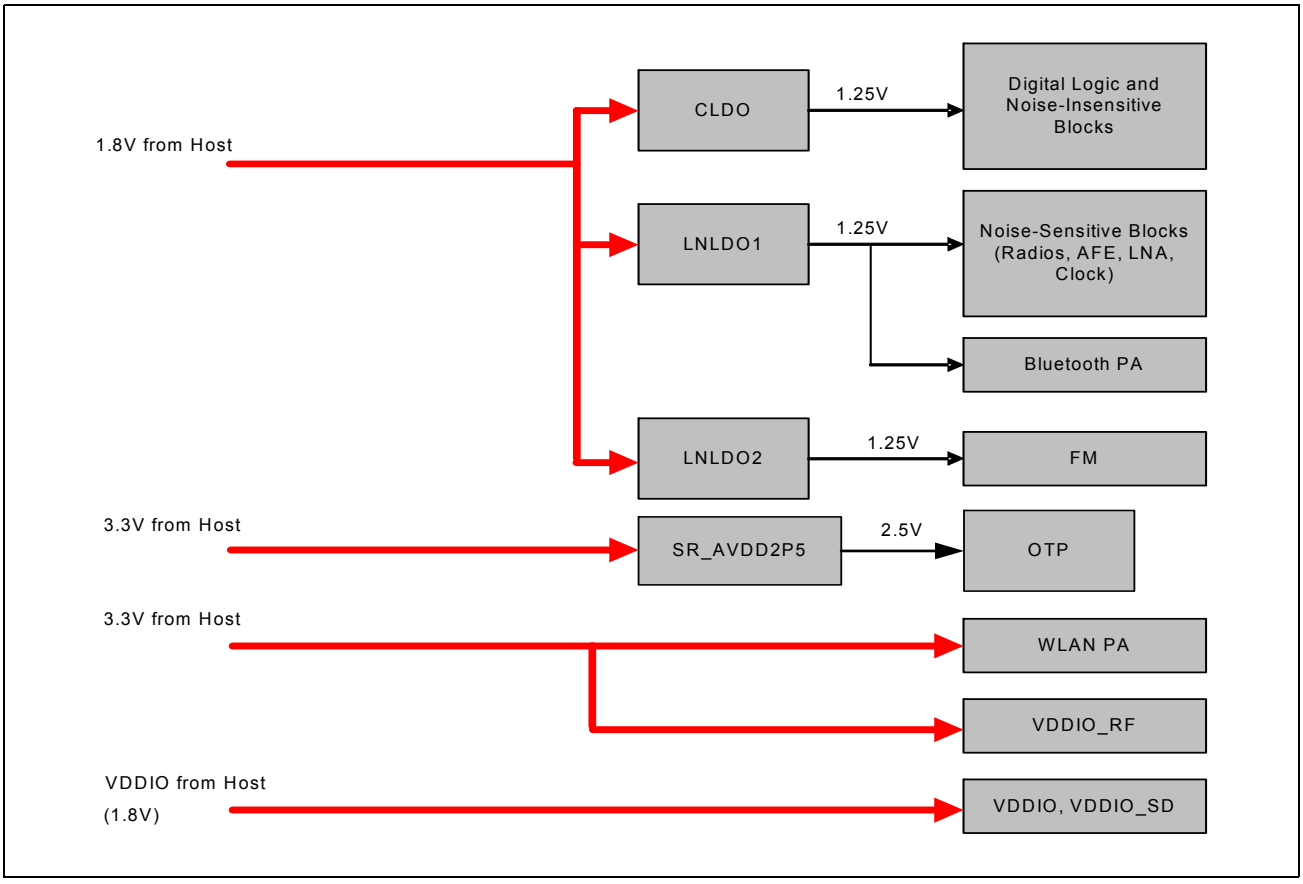
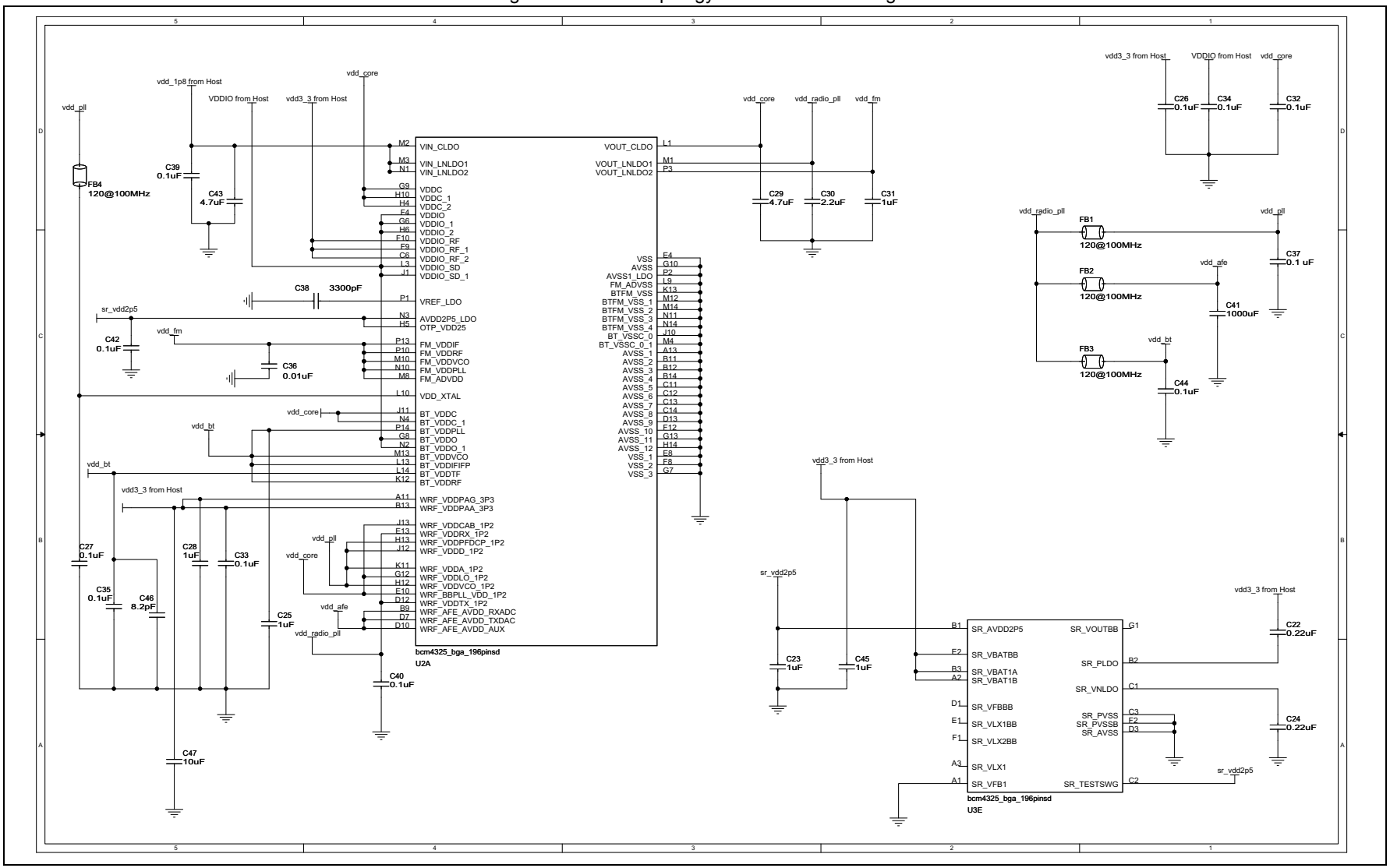


Figure 11. Power Topology 5 Schematic Drawing



8.6 Power Topology 6: Host Provides 3.3V and 1.25V, FM, and Class 2 Bluetooth Support

In this power topology (see Figure 12 and Figure 13), the host provides regulated power rails for 3.3V, 1.8V (for VDDIO), and 1.25V supplies. The host-supplied 1.25V rail directly feeds the 1.25V digital logic and noise-insensitive blocks of the CYW4325. This 1.25V rail is also filtered and then used to provide 1.25V to the noise-sensitive (radio, AFE, LNA, Bluetooth PA, and so on) portions of the CYW4325. FM support is also provided, and the FM core gets a dedicated filtered version of the host's 1.25V supply. Effectively, all of the CYW4325 regulators (switching and LDOs) are bypassed except for the low-current LDO that outputs 2.5V for the CYW4325 OTP block. This topology is ideal for systems that have regulated 3.3V and 1.25V supplies available (with sufficient load currents) that can be allocated to the CYW4325. It provides the lowest external component count and also provides the best efficiency. Other than the small 3.3V to 2.5V LDO for OTP, no other regulation occurs in the CYW4325 circuit. The end efficiency is based on the efficiency of the system regulators only. One trade-off to this approach is that the cleanliness of the 1.25V rail is critical because it does not benefit from the noise rejection characteristics of the CYW4325 on-chip LNLDOs. The topology assumes Class 2 Bluetooth support.

Figure 12. Power Topology 6 Block Diagram

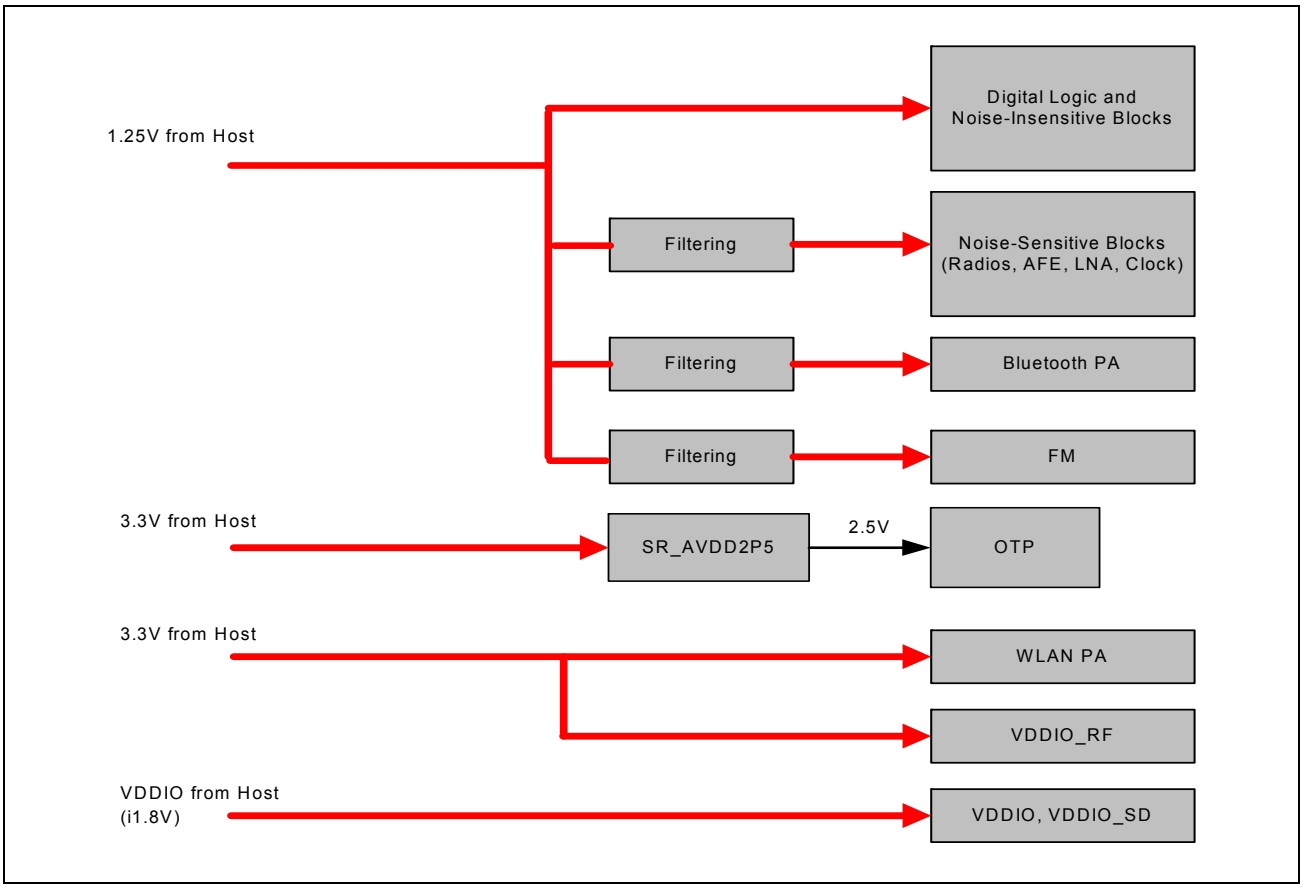
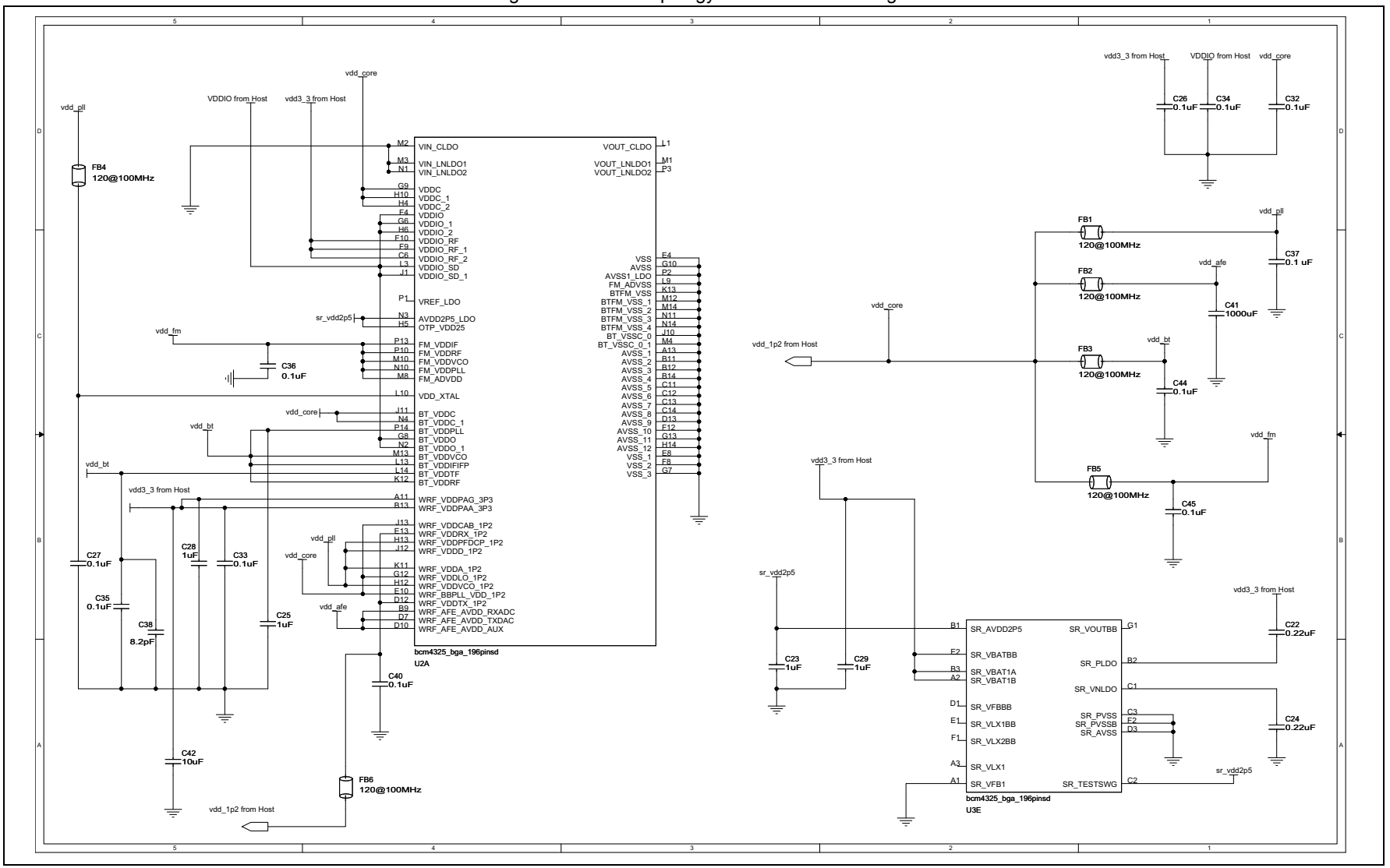


Figure 13. Power Topology 6 Schematic Drawing



8.7 Power Topology 7: Host Provides 3.3V and 1.25V, FM, and Class 1 Bluetooth Support

In this power topology (see Figure 14 and Figure 15), the host provides regulated power rails for 3.3V, 1.8V (for VDDIO), and 1.25V. The host-supplied 1.25V rail directly feeds the 1.25V digital logic and noise-insensitive blocks of the CYW4325. This 1.25V rail is also filtered and then used to provide 1.25V to the noise-sensitive (radio, AFE, LNA, FM core, and so on) portions of the CYW4325. LNLDO2 is used in 2.5V output mode and supplies the Bluetooth PA for Class 1 support. The only other CYW4325 regulator that is used is the low-current LDO that outputs 2.5V for the CYW4325 OTP block. This topology is ideal for systems requiring FM and Class 1 Bluetooth that have regulated 3.3V and 1.25V supplies available (with sufficient load currents) that can be allocated to the CYW4325. It provides the lowest external component count and also provides the best efficiency. Other than the LNLDO2 current, the end efficiency of the design is largely based on the efficiency of the system regulators only. One trade-off to this approach is that the cleanliness of the 1.25V rail is critical because it does not benefit from the noise-rejection characteristics of the CYW4325 on-chip LNLDOs.

Figure 14. Power Topology 7 Block Diagram

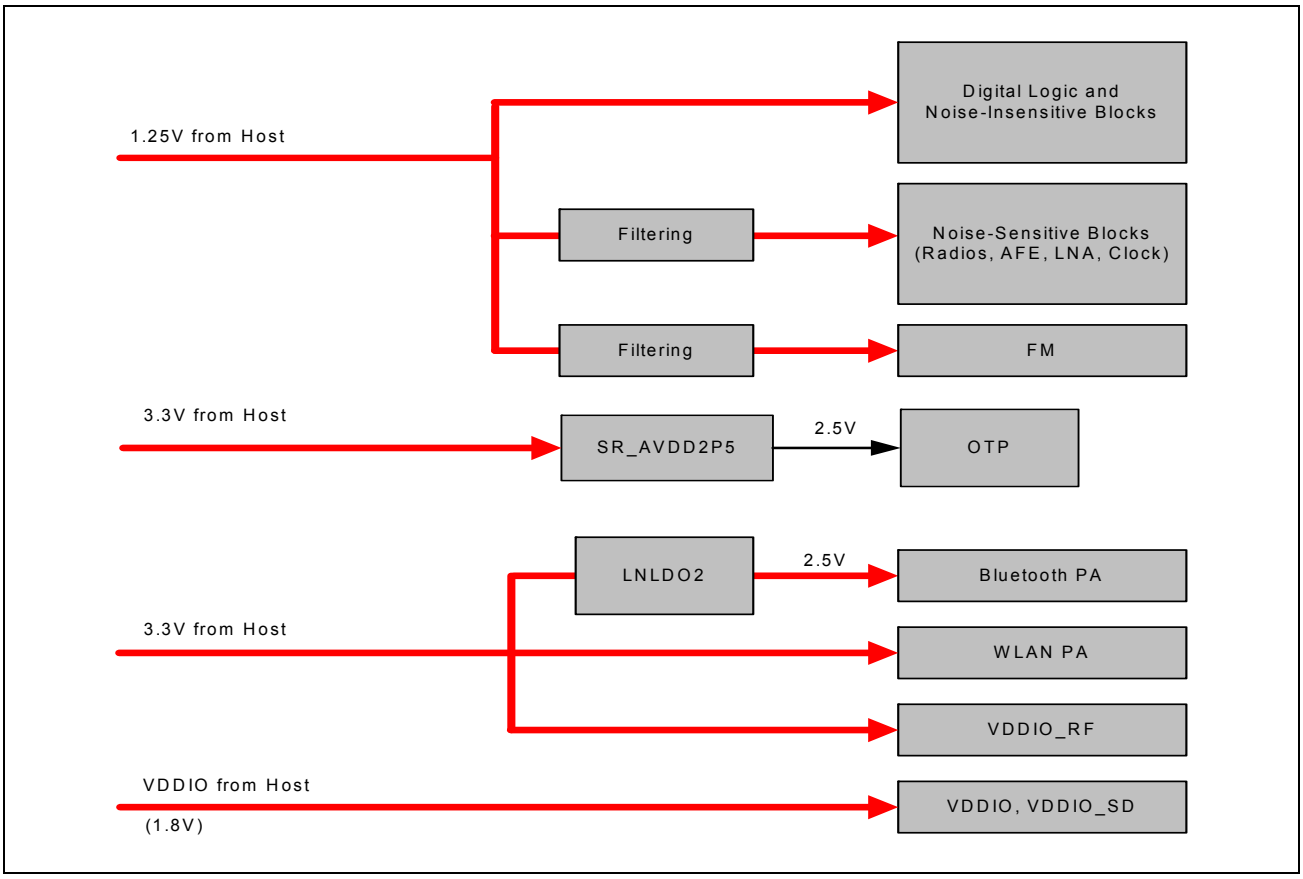
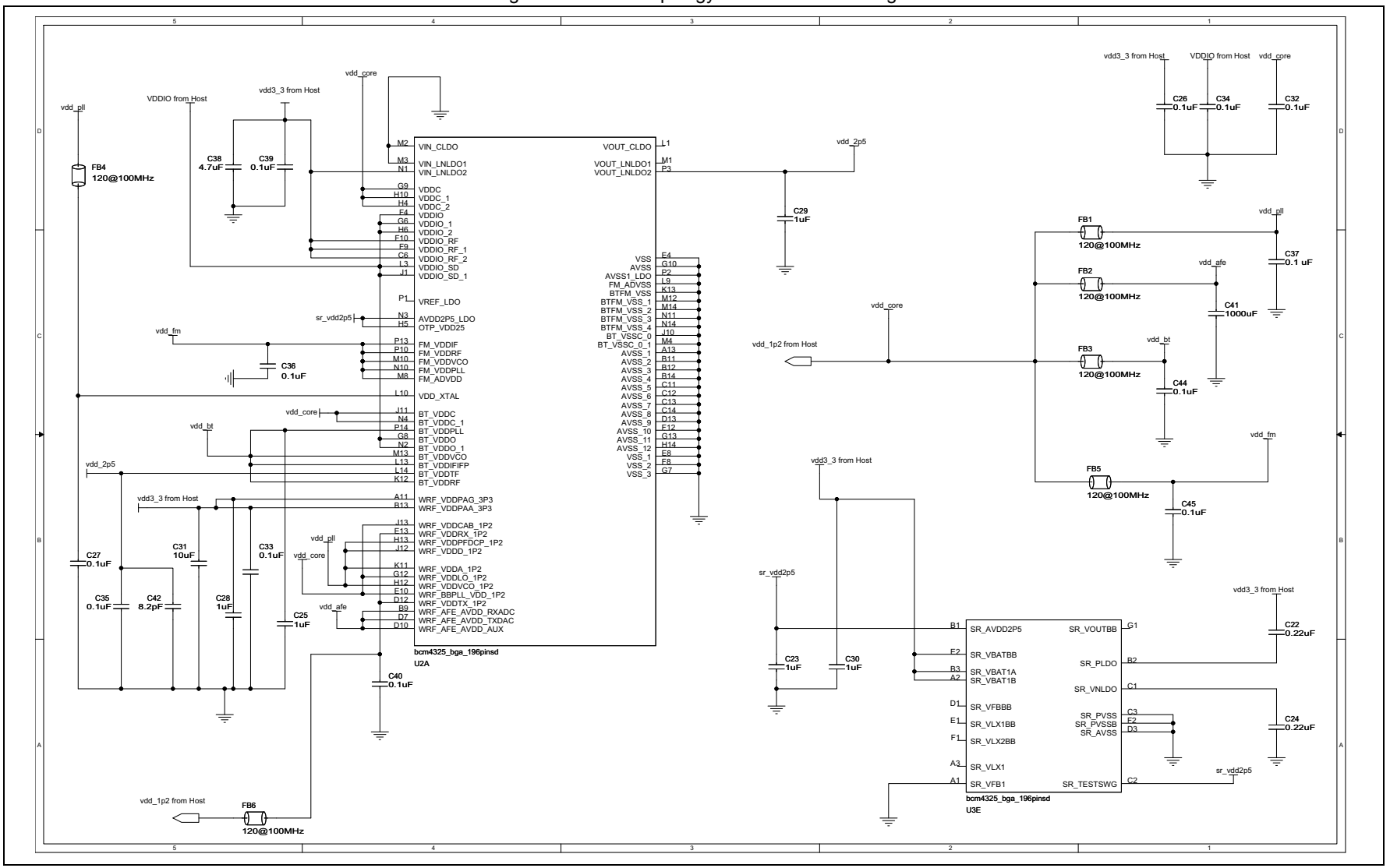


Figure 15. Power Topology 7 Schematic Drawing



9 Sequencing of Reset and Regulator Control Signals

The CYW4325 has four signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below. Additionally, diagrams are provided to indicate proper sequencing of the signals for various operational states (see Figure 16 and Figure 17 on page 20, Figure 18 and Figure 19 on page 21, and Figure 20 on page 21). The timing values indicated are minimum required values; longer delays are also acceptable.

Note that the WL_REG_ON and BT_REG_ON are ORed in the CYW4325. The diagrams show both signals going high at the same time (as would be the case if both REG signals were controlled by a single host GPIO). If two independent host GPIOs are used (one for WL_REG_ON and one for BT_REG_ON), then only one of the two signals needs to be high to enable the CYW4325 regulators.

Also note that the reset requirements for the Bluetooth core are also applicable for the FM core. In other words, if FM is to be used, then the Bluetooth core must be enabled.

Wait at least 100 ms after VDDC is available before initiating SDIO accesses.

9.1 Description of Control Signals

- **WL_REG_ON**: Used by the PMU (along with BT_REG_ON) to decide whether to power down the internal CYW4325 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators will be disabled.
- **BT_REG_ON**: Used by the PMU (along with WL_REG_ON) to decide whether to power down the internal CYW4325 regulators. If both the BT_REG_ON and WL_REG_ON pins are low, the regulators will be disabled.
- **WL_RST_N**: Low Asserting Reset for WLAN Core. This pin must be driven high or low (not left floating). *If WL_RST_N is low (regardless of BT_RST_N state), the WLAN core will be powered off*.
- **BT_RST_N**: Low asserting reset for Bluetooth core. This pin must be driven high or low (not left floating).

9.2 Control Signal Timing Diagrams

Figure 16. WLAN = ON, Bluetooth = ON

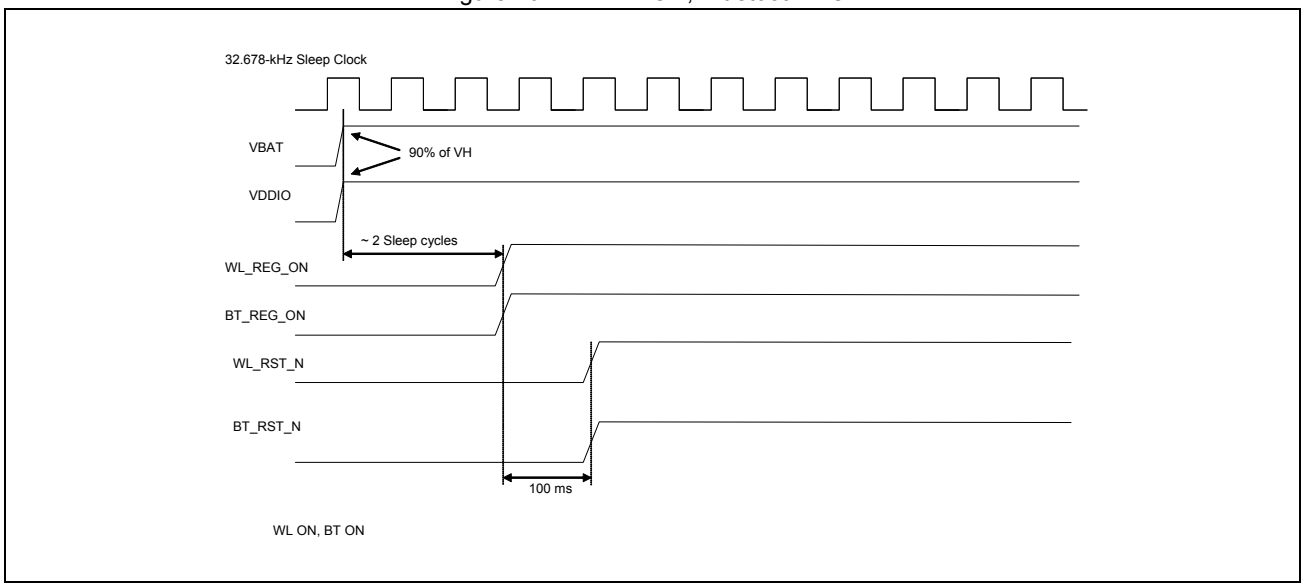


Figure 17. WLAN = OFF, Bluetooth = OFF, VDDC Provided by CYW4325 (See Power Topologies 1–5)

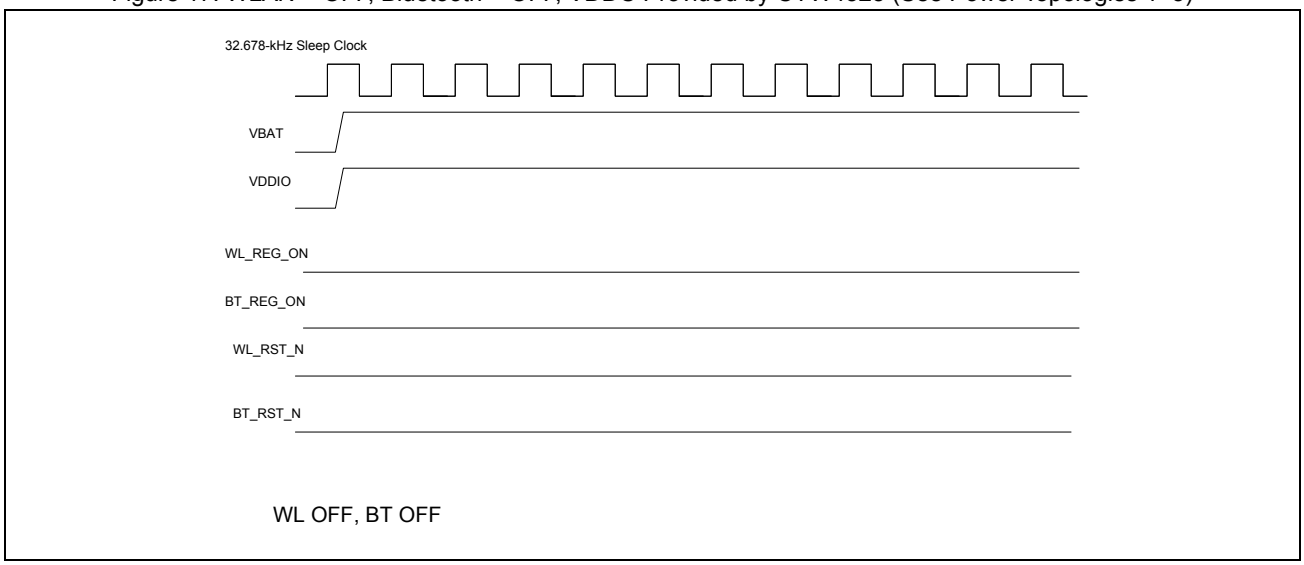


Figure 18. WLAN = OFF, Bluetooth = OFF, VDDC Provided Externally (See Power Topologies 6–7)

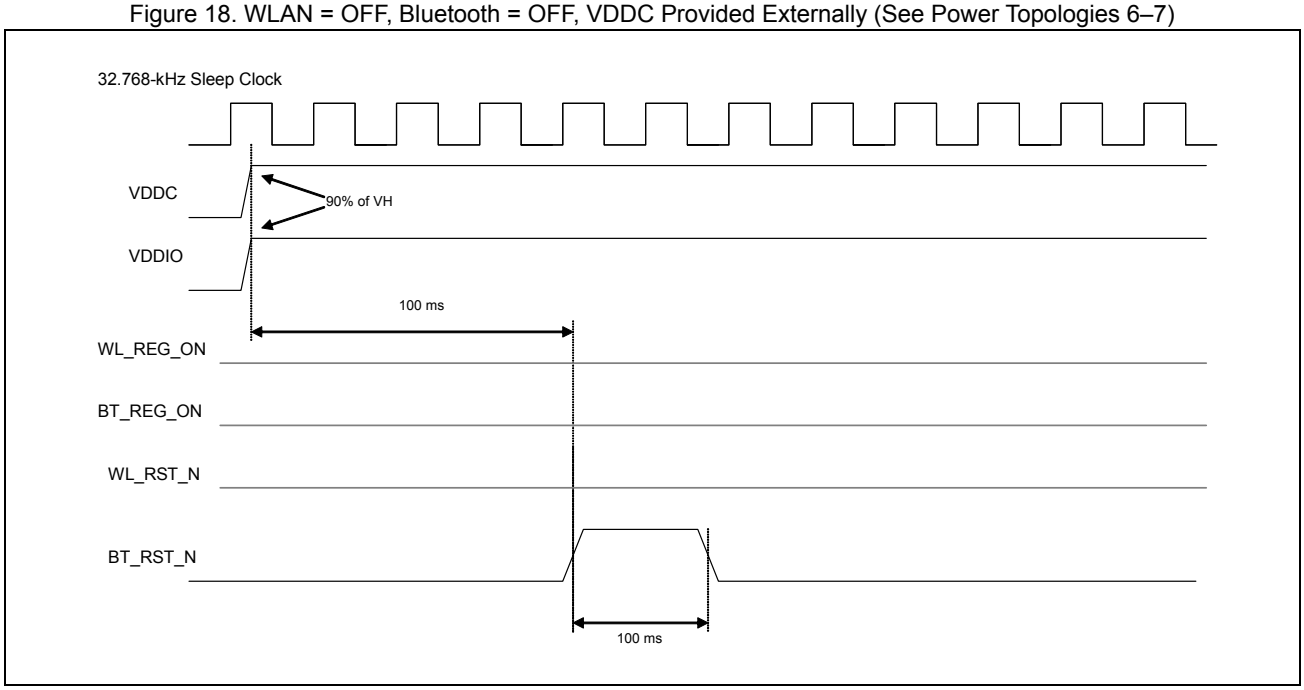


Figure 19. WLAN = ON, Bluetooth = OFF

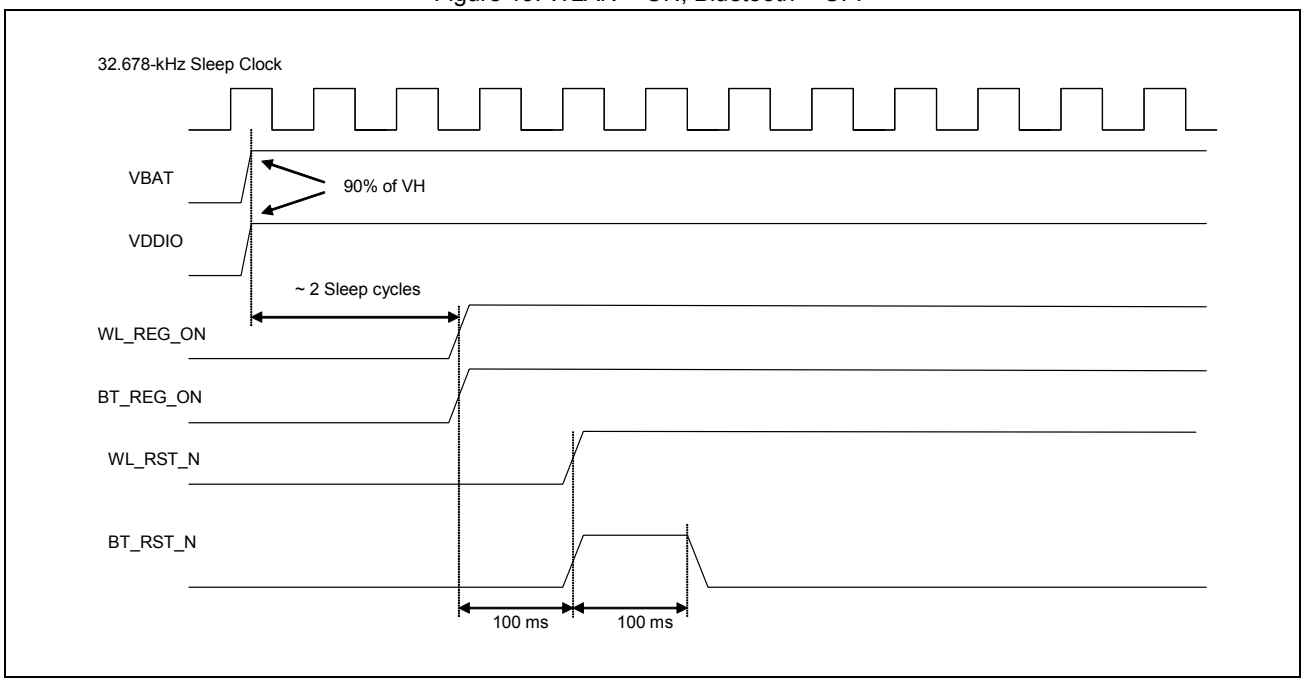
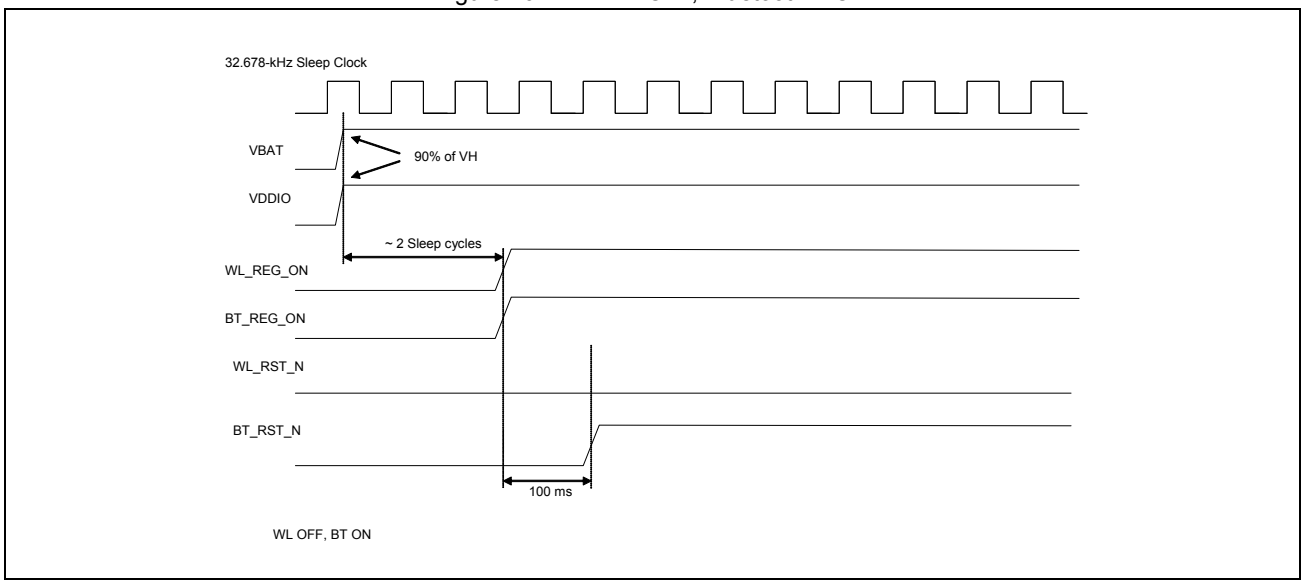


Figure 20. WLAN = OFF, Bluetooth = ON



10 Low Power States

The CYW4325 has four external controls lines, BT_RST_N, WL_RST_N, BT_REG_ON, and WL_REG_ON, in addition to clocks and power supplies that enable control of the state of the device. To cover all low power states, however, it is necessary to also include firmware control, which results when the WLAN driver, the Bluetooth Configuration file, or both are loaded. It is especially important to understand these states to be able to minimize current consumption in the end product.

The details of controlling the external control lines relative to clocks and supply rails have already been discussed earlier. The information in Table 2 explains each state and the associated required controls.

Table 2. Low Power States

State	State Description	Power[a]	Sleep CLK	REG_ON[b]	BT_RST_N	WL_RST_N	BT Config Loaded	WL Driver Loaded	FW Commands/ Comments	*Power Status* [c]
0	OFF (No Power)	OFF	OFF	LOW	LOW	LOW	NO	NO	–	Disabled (0 µA)
1	OFF (VBAT + VDDIO enabled)	ON	Don't Care	LOW	Don't Care	Don't Care	NO	NO	–	Lowest power (typically <25 µA)
2	RESET	ON	ON	HIGH	LOW	LOW	NO	NO	–	Not low power[d] (typically 6 mA)
3	Default ON	ON	ON	HIGH	HIGH	HIGH	NO	NO	–	Not low power[f] (typically 10 mA)
4	ON (WL Only)	ON	ON	HIGH	HIGH	HIGH	NO	YES	WL Driver may be loaded before BT Config to read BD ADDR from OTP.	Application and FW dependent[e] Not low power
5	ON (BT Only)	ON	ON	HIGH	HIGH	HIGH	YES	NO	BT Config loaded. BD_ADDR set.	Application and FW dependent[g] Not low power
6	ON (BT + WL)	ON	ON	HIGH	HIGH	HIGH	YES	YES	BT Config loaded. BD_ADDR set.	Application and FW dependent[g] Not low power
7	BT & WL Sleep	ON	ON	HIGH	HIGH	HIGH	YES	YES	WL in Low power mode, BT in Sleep.	System Sleep (typically <250 µA)
8	WL Sleep (BT HW Rst)	ON	ON	HIGH	LOW	HIGH	NO[f]	YES	WL entered into low power mode.	WL sleep (typically <200 µA)
9	BT Sleep (WL HW Rst)	ON	ON	HIGH	HIGH	LOW	YES	NO[g]	BT entered into Sleep.	BT Sleep (typically <160 µA)

a. Power can be in applied in many possible topologies, which are not distinguished in the table. Therefore, if there are any questions about application power sequences that are not addressed, contact Cypress support for assistance.

b.For the state table, "REG_ON" represents WL_REG_ON or BT_REG_ON. The signals are OR'd internal to the device.

c.Current values listed under **Power Status** are best estimates. Actual current values might vary, depending on the application design. Current values listed are combined VBAT and VDDIO values.

d.Although the device is held in hardware reset, the regulators are in the default state. The device must be controlled either from WL Driver or BT Config to transition to a controlled low power mode.

e.This table is not intended to detail all operating modes relative to software control and associated currents.

f.When BT_RST_N is transitioned to LOW the loaded BT config and any other HCI command settings will be lost.

g.When WL_RST_N is transitioned to LOW the loaded WL driver and any other WL specific commands will be lost.

The following example illustrates the transitioning from OFF to a WL Low-Power Sleep mode:

1. The device is OFF.
2. VBAT and VDDIO are applied (plus other voltage supplies relevant to the specific application).
3. Sleep CKLK enabled and REG_ON set to Logic High (note sequence in previous section of this document).
4. WL_RST_N set to logic High (note sequence in previous section of this document that includes BT_RST_N momentary pulse).
5. WL Driver is downloaded.
6. WL is commanded to transition to Low power.

10.1 Sequence for Transitioning CYW4325 to Bluetooth Sleep Mode

The CYW4325 can transition to Bluetooth Sleep mode only through the combined procedure of loading the configuration file and issuing a set of HCI commands, as shown in the following example. Although there are variants of Sleep mode operation, this example focuses on the most common model using external GPIOs for Host Wake and BT Wake (known as Sleep Mode 1).

Transition to Bluetooth Sleep Mode 1 (top-level steps):

1. From the OFF state, the device is powered into the ON state (with either WL_RST_N being high or low).
2. An HCI reset command is sent via the UART interface.
3. The UART baud rate is set for the application using an HCI Vendor-Specific command.
4. The Config file download process commences (a set of HCI is commands is required).
5. The BD ADDR is written to the device using an HCI Vendor-Specific command).
6. An HCI reset command is sent via the UART interface.
7. The HCI **Set_Sleepmode_Param** command is sent to the device.

- This command sets the sleep mode (Sleep mode 1 "UART" uses GPIOs to wake the device from sleep and also to signal that the host is required to wake. Refer to application note *UART Sleep Mode Operation*, for more details).
- BT WAKE polarity is essential to transitioning the device to sleep mode. The **Set_Sleepmode_Param** command allows you to set the polarity. If the device is to be in sleep when BT_Wake (BT_GPIO_0) is LOW, ensure that the polarity of BT_Wake is set to *Active High*.

8. Toggle the polarity of BT_Wake (BT_GPIO_0) to enter and exit sleep mode.

10.2 Sequence for Transitioning CYW4325 to WLAN Low-Power Sleep Mode

In the low-power sleep state, WLAN is not associated and does not wake up to listen for beacons. This is the lowest power consumption state for WLAN in which WLAN is not being held in reset, and power is being applied to the CYW4325. In this state, the system clock is disabled but the Sleep CLK is still running. The CYW4325 WLAN radio is disabled. Finally, the SDIO interface is put into Power Save mode.

To disable Bluetooth functionality and transition the WLAN operation to low-power Sleep mode:

1. From OFF, the device is powered into the WLAN ON state following the RST and REG_ON sequencing requirements described earlier.
2. Execute the following commands:

wl up

wl deepsleep 1

dhd idleclock stopped

11 Power Supply Layout Guidelines

11.1 EMI Reduction (Forward and Return Paths)

To reduce EMI, the areas enclosed by the following loops must be minimized:

- SR_VLX1 to inductor and capacitor to SR_PVSS1
- SR_VLX2 to inductor and capacitor to SR_PVSS2
- SR_VLX1BB to inductor to SR_VLX2BB
- SR_VOUTBB to capacitor to SR_PVSSBB
- SR_VBAT1A to supply bypass capacitors to SR_PVSS1
- SR_VBATBB to supply bypass capacitors to SR_PVSSBB

These lines must be as wide and short as possible to maximize efficiency for large current flow (up to 1-amp transients possible) and minimize line inductance.

Place the inductors and capacitors as close as possible to SR_VLX1, SR_VLX2, SR_VLX1BB, SR_VLX2BB, and SR_VOUTBB. Keep all RF, clock, and other sensitive analog lines as far away as possible from these lines.

11.2 Switcher Inductors

- Use only inductors that meet the guidelines described in Switcher Inductor Recommendations on page 28.
- Keep these inductors as far away as possible from the RF section.
- Use the top layer for direct connection to SR_VLX1, SR_VLX2, SR_VLX1BB, and SR_VLX2B.
- Avoid using vias as they add excessive resistance and inductance.

11.3 Switcher Output Capacitors

- Use low ESR (<30-mohm) capacitors. X5R ceramic capacitors are recommended.
- Ensure that these capacitors have a low-resistance connection to the ground plane by using more vias.
- Place these capacitors near to their respective switcher outputs.

11.4 Switcher LDO Capacitor Connections

- Place one terminal of the SR_VSSPLDO capacitor close to the CYW4325 SR_VSSPLDO pin. The other terminal should have a short, low-resistance route to the SR_VBAT1A, SR_VBAT1B, and SR_VBATBB pins.
- Place one terminal of the SR_VDDNLDO capacitor close to the CYW4325 SR_VDDNLDO pin. The other capacitor terminal should be connected to the ground plane with short, low-resistance traces.
- If vias are needed to access the supply/ground plane, use as many vias as possible.

11.5 Switcher Power and Analog Grounding

- SR_PVSS1 and SR_PVSS2 are connected in the 196-pin FCBGA package as SR_PVSS. In the case of the WLCSP package where there are separate bumps, separately connect each bump (SR_PVSS1, SR_PVSS2, SR_PVSSBB, and SR_AVSS) through its own via for a direct, low-resistance connection to the ground plane. This ground plane goes to the negative terminal of the Li-ion battery. If vias must be used, use as many vias as possible to reduce via resistance and inductance.
- Do not short SR_PVSS and SR_AVSS pins at any board layer other than the solid board ground plane. This requirement is to avoid possible interference from SR_PVSS, which has high switching ground currents to SR_AVSS during switcher operation.

11.6 Switcher Input Supplies

- Connect SR_VBATBB, SR_VBAT1A, and SR_VBAT1B to a solid a VBAT power plane with traces that are as wide as possible.
- If it is necessary to go through multiple layers to access the power plane, use more than one via (3 to 4 vias is ideal) to reduce via inductances that may cause excessive ringing due to switching transients.
- Place supply bypass capacitors as close and with as wide traces as possible to SR_VBAT1A, SR_VBAT1B, SR_VBATBB to absorb the switching transients. The traces to the supply pins could see very high transient current spikes (>1 amp), and it is critical that the traces be as wide as possible and with as short a path as possible to the bypass capacitor terminal. Connect the other terminal of the supply bypass capacitor to a solid ground plane.
- The VBAT power plane or traces should preferably be on the top layer with ground on the layer adjacent to it. This is to minimize vias and inductance on this supply. The VBAT supply should pass through the 4.7-µF decoupling capacitor before connecting to the BBOOST and CBUCK input pins.

11.7 Multiple Power/Ground Planes

- If large VBAT or ground planes are not possible, implement large, thick traces to avoid degrading the efficiency.
- If supply and ground pins must go through multiple planes, use as many vias as possible near the supply and ground chip pins.

11.8 Low-Noise LDO Band Gap Bypass Capacitor

- Keep the line from the VREF_LDO pin to its capacitor to the AVSS_LDO pin as short as possible and away or shielded from noisy signals. This signal is the low-noise reference for the low-noise LDOs.
- Use a thick route from VREF_LDO pin to its capacitor.
- Connect the capacitor to the ground plane directly. If vias are needed, use multiple vias.

11.9 Switcher Voltage Feedback Sensing

Do not route SR_VFB1, SR_VFB2, and SR_VFBB pins near oscillators or noise sources. These voltage feedback traces are usually connected near the load ends for better voltage regulation at the load end, especially when the load is far away.

11.10 LDO Input and Output Capacitors

Place LDO input and output capacitors as close as possible to their respective pins. Otherwise, their ESR and any trace impedance may present stability and transient settling issues. These capacitors should have good low-resistance connection to supply/ground planes. If a via must be used, use multiple vias.

11.11 Switcher Output to Load Routing

For good load regulation, minimize the resistance of the power lines from the regulators to their respective loads by using wide, short power traces.

11.12 WLAN Power Amplifier (PA) Supplies

The routing of the 3.3V PA supply to the WRF_VDDPAA_3P3 ("PAA") and WRF_VDDPAG_3P3 ("PAG") pins is very critical. The BGA package has a single "PAG" pin (A11) and a single "PAA" pin (B13). The WLCSP package has two pins for each ("PAG" = pins 7 and 8, "PAA" = pins 3 and 4).

The "PAG" pins are the main PA supply and require significant current. Therefore make the traces to these pins as wide as possible and have at least two vias if changing layers is required. The "PAA" pins are lower current (approximately 30 mA), so a single via is adequate. Note that if IEEE 802.11a operation is also used, the PAA pins are also high current and should be fat with multiple vias.

- Split the 3.3V source to these pins into two separate branches, one for the "PAG" pins, and one for the "PAA" pins. Start these two branches from the main 3.3V source as soon as possible so that there is as much distance/inductance between them as possible. The separation between the two branches should be long enough to create at least 4 to 5 nH of inductance.
- Place a 1-µF decoupling capacitor as close as possible to the CYW4325 "PAG" pin. Place a 0.1-µF decoupling capacitor as close as possible to the CYW4325 "PAA" pin. If IEEE 802.11a operation is used, then use a 1-µF capacitor for the “PAA” pin instead. See Figure 21 for more details. The WLCSP package is used in this example.

Figure 21. CYW4325 WLAN PA Supply Recommendations

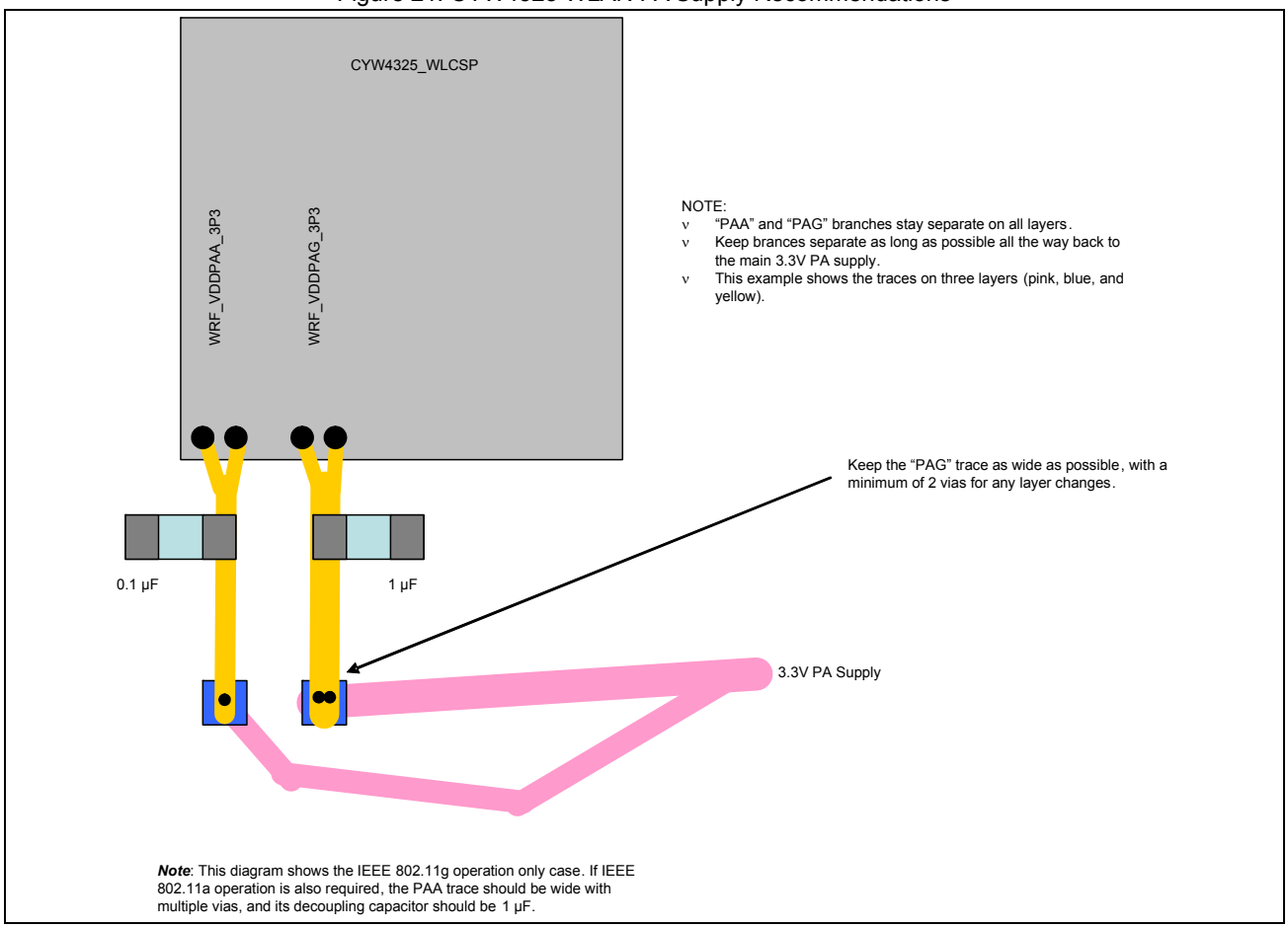


Figure 22. PCB Trace Recommendations for High-Current Paths

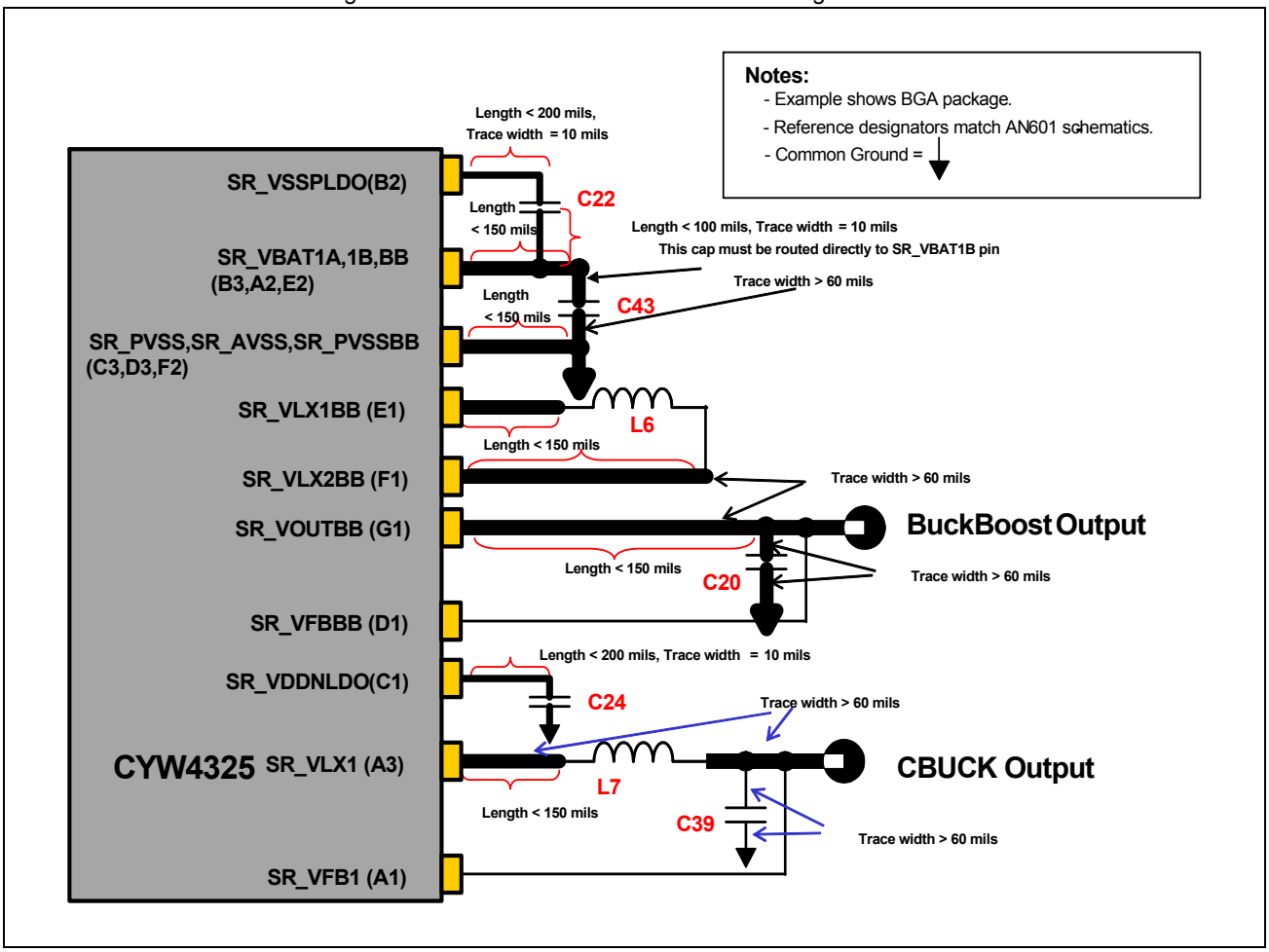
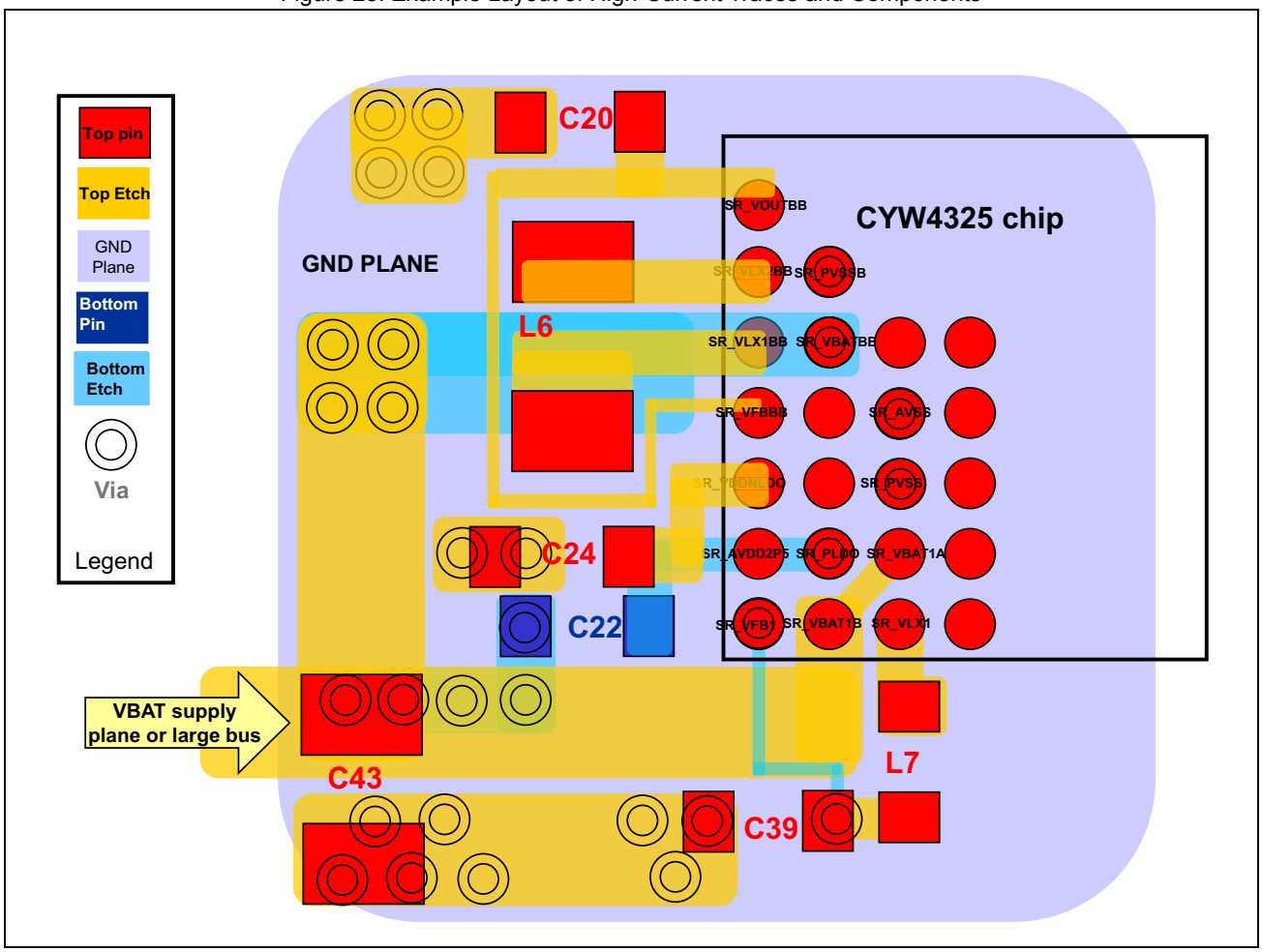


Figure 23. Example Layout of High-Current Traces and Components



12 Switcher Inductor Recommendations

The following inductors are used for the CBUCK and BBOOST Cypress reference designs:

CBUCK: TDK VLF3010AT-3R3MR87

BBOOST: TDK VLF4012AT-4R7M1R1

These components benefit from having received the most extensive amount of testing at Cypress. It is understood, however, that some target systems have mechanical requirements that will require different inductors. This section describes critical items that must be considered when a substitute for these inductors is being considered. Note that complete qualification of an inductor requires more than a review of the data sheet. It also requires in-system component testing, which can be time consuming. We recommend using only the substitute parts that we have already evaluated (see Recommended Inductors for the CBUCK Regulator on page 30 and Recommended Inductors for the BBOOST Regulator on page 30).

12.1 Inductor Specifications and Implications

The follow specifications are critical to proper switcher stability and functionality and *cannot* be compromised:

- Nominal Inductance value:
  - Usually measured at 1-MHz test frequency at 20°C.
  - Nominal values are 3.3 µH for the CBUCK regulator and 4.7 µF for the BBOOST regulator.
- Tolerance of nominal inductance value:
  - L ≤ ±30%
- Inductors for both the CBUCK and BBOOST must not collapse to too low an inductance value causing the switcher to oscillate before the over-current limit protection activates.

- For the CBUCK, the inductor is nominally 3.3 µH and must be at least 1.5 µH at currents of 500 mA and across temperature. Because inductor data sheets typically show only "Inductance versus DC current" plots at nominal values, the plot should be shifted to account for the worst case tolerance (–30%, for example) of the part as well.
- For the BBOOST, the inductor is nominally 4.7 µH and must be at least 2.6 µH at currents of 910 mA with the default 10-µF capacitor on the BBOOST output. If an additional 4.7-µF capacitor is added to the BBOOST output, the
  2.6-µH requirement is relaxed to 610 mA. Regarding placement of these components, the 10-µF capacitor should be close to the BBOOST output. The new 4.7-µF inductor can replace the 1-µF capacitor used for WRF_VDDPAG_3P3. Alternately, a single 22-µF capacitor can be used instead of the 10-µF + 4-µF combination. Regarding component placement for this option, the 22-µF capacitor should be close to the BBOOST output. Note that in this case, the
  1-µF capacitor close to WRF_VDDPAG_3P3 is still required. As with the CBUCK, the requirements must be met across temperature and must account for the worst-case tolerances of the inductor.
- Inductor structure:
  - Wire-wound or multilayered compound.
  - Recent developments have seen new multilayered compound inductors, which are lower profile and have a smaller footprint compared to wire-wound inductors. Multilayered compound inductors are also typically less expensive. However, a big disadvantage with multilayered parts is that there is a significant droop in inductance over loads. Multilayered inductor data sheets typically show inductance droop versus DC loads. However, bench testing has shown that these inductors actually droop almost instantaneously in response to fast transient load levels.
  - Some of the new ultralow-profile wire-wound inductors also exhibit inductance droop problems similar to the multilayered devices.
  - Extensive bench testing with the actual switchers is required to ensure that these types of devices are suitable in presence of switcher transients.
  - In testing thus far, Cypress has found that multilayered components are suitable only for use with the CBUCK regulator (not the BBOOST regulator).

The following specifications affect switcher efficiency. Design trade-offs (smaller footprint at the cost of lower efficiency, for example) can be considered for these specifications:

- DCR (also known as Rdcor ESR) ≤ 200 mohm to avoid reduced efficiency (approximately 5% reduction). Make sure that DCR does not exceed 320 mohm.

Other specifications that depend on the requirements of the target system:

- Shielding (metal case/magnetic) versus nonshielding
- Footprint and height

12.2 Recommended Inductors for the CBUCK Regulator

The following inductors are recommended alternatives to use with the CBUCK regulator.

Table 3. Recommended Parts for Use with the CBUCK Regulator

Part No.	Mfgr	Dimensions (mm) W	L	H	Inductance (µH)	Tolerance (± µH in %)	Maximum DCR (mohm)	Typical DCR (mohm)	Peak Efficiency (1.5V out, 3.3VBAT, 150-mA Load)	Notes	Isat Based on +40°C (mA)	Isat Based on 30% L Change (mA)
VLF3010AT-3R3MR87	TDK	2.6	2.8	1.0	3.3	20	170	150	90%	a	1000	870
CDRH2D18/HP-3R3NC	Sumida	3.0	3.0	2.0	3.3	30	86	69	90%	–	1550	1450
1117AS-3R3M	TOKO	2.8	3.0	1.0	3.3	20	156	130	–	–	1300	1200
MIPSA2520D3R3	FDK	2.5	2.0	1.2	3.3	30	156	120	87%	b	1000	–
VLS252010T-3R3M	TDK	2.0	2.5	1.0	3.3	20	304	253	–	c	940	1200
LQM31PN4R7M00	Murata	1.6	3.2	0.95	4.7	20	300	240	85%	d	800	–
LQM2HPN3R3MG0	Murata	2.0	2.5	0.9	3.3	20	125	100	–	b	1200	–
CPL2512T3R3M	TDK	1.5	2.5	1.2	3.3	20	312	240	85%	e	730	730
VLS3012T3R3M1R3	TDK	3.0	3.0	1.2	3.3	20	120	100	–	–	1700	1500
FLF3215T-3R3M	TDK	2.5	3.2	1.65	3.3	20	78	65	–	–	1600	1200
CDRH26D09NP-3R3PC	Sumida	2.8	2.6	1.0	3.3	25	260	208	85%	–	750	900

a.Used in Cypress reference designs.

b.Limited bench testing

c.Efficiency expected to drop by approximately 5% due to high DCR.

d.Efficiency drops by approximately 5% due to high DCR. The 4.7-µH inductor was chosen in this specific case so that the inductance of the component will be greater than 2 µH in spite of drooping at 700-mA loads.

e.Efficiency drops by approximately 5% due to high DCR.

12.3 Recommended Inductors for the BBOOST Regulator

The following inductors are recommended alternatives to use with the BBOOST regulator.

Table 4. Recommended Parts for Use with the BBOOST Regulator (Output Capacitor = 10 µF)

Part No.	Mfgr	Dimensions (mm) W	L	H	Inductance (µH)	Tolerance (± µH in %)	Maximum DCR (mohm)	Typical DCR (mohm)	Peak Efficiency (1.5V out, 3.3Vbat, 150-mA Load)	Notes	Isat Based on +40°C (mA)	Isat Based on 30% L Change (mA)
VLF4012AT-4R7M1R1	TDK	3.7	3.5	1.2	4.7	20	160	140	–	a	1100	1100
DO1606T-472	Coilcraft	6.5	5.23	2.0	4.7	20	150	–	92	–	1100	1200
LPS4012-472ML	Coilcraft	3.9	3.9	1.1	4.7	20	175	–	93	–	–	1400
VLS3012T4R7M1R0	TDK	3.0	3.0	1.2	4.7	20	156	130	–	–	1400	1200
FLF3215T-4R7M	TDK	2.5	3.2	1.65	4.7	20	108	90	–	–	1360	1000

a.Used in Cypress reference designs.

Table 5. Recommended Parts for Use with the BBOOST Regulator (Output Capacitor = 10 µF + 4.7 µF or Single 22 µF[a])

Part No.	Mfgr	Dimensions (mm) W	L	H	Inductance (µH)	Tolerance (± µH in %)	Maximum DCR (mohm)	Typical DCR (mohm)	Peak Efficiency (1.5V out, 3.3Vbat, 150-mA Load)	Notes	Isat Based on +40°C (mA)	Isat Based on 30% L Change (mA)
1117AS-4R7M	TOKO	3.0	2.8	1.0	4.7	20	204	170	–	–	950	680
VLF3010AT-4R7MR70	TDK	2.8	2.6	1.0	4.7	20	280	240	–	b	820	700
VLF3012AT-4R7MR74	TDK	2.6	2.8	1.2	4.7	20	190	–	–	–	–	740

a.See item 3b in Inductor Specifications and Implications on page 28 for details on where these capacitors should be placed.

b.Not tested yet, but a good option for VBAT ≥ 2.7V.

12.4 Regulator Capacitor Considerations

When choosing capacitors for the CYW4325 regulators, it is important to make sure that across tolerance, temperature, and with aging that the capacitor continues to provide the minimum required capacitance required by the regulators. One factor that also needs to be considered is how the capacitor's value is affected by DC bias. If a capacitor is biased at a voltage close (3.3V bias is "close" to a 6.3V rating) to its rating, a significant drop in capacitance can occur. This DC bias effect can be particularly severe in smaller form factor capacitors. For cases where the DC bias is significant, it is recommended that the highest possible voltage rating is used when a capacitor is chosen. If a higher voltage rating is not available, a capacitor with a larger value can be used.

Table 6 lists the nominal and minimum required capacitance for each regulator. The nominal capacitance is the value listed by the capacitor vendor for a given part number. The minimum value is the actual capacitance after factoring in the following:

- Part-to-part variance (tolerance)
- DC bias capacitance droop effect
- Temperature capacitance droop effect

Because of these effects, there may be cases where a higher nominal value needs to be chosen to meet the minimum capacitance requirements. For example, If a the 4.7-µF capacitor chosen for the VBAT_Input droops below 3 µF due to the DC bias droop effect, then that device either needs to be changed for a 4.7-µF part with a higher voltage rating (and less DC bias droop) or for a part with a higher nominal capacitance, such as a 6.8-µF part.

If the CBUCK regulator requires alternate capacitor, see Table 7 on page 32. The parts are listed in order of their preference. The parts that are not on the recommended list require Cypress approval.

Table 6. Nominal and Minimum Capacitance Requirements

Supply	Nominal Capacitance	Minimum Capacitance	Recommended Device
CBUCK output	4.7 µF	3 µF	TDK® C1608X5R0J475MT
BBOOST output	10 µF	5.5 µF	TDK C1608X5R0J106M
CLDO output	4.7 µF	3 µF	TDK C1608X5R0J475MT
LNLDO1 output	2.2 µF	1.7 µF	Murata® GRM188R61A225KE34
LNLDO2	1 µF	0.76 µF	Murata GRM155R61A105KE15
VBAT (SWR's shared input)	4.7 µF	3 µF	TDK C1608X5R0J685K Murata GRM188R61A475K

The following tools give a good simulation of Murata and TDK capacitors regarding effects of DC bias and so on:

http://www.tdk.co.jp/eseat/

http://www.murata.com/designlib/mccdl/index.html

Table 7. Recommended Parts for Usage of Alternate Capacitor with the CBUCK Regulator

Preference Order	*Part No.*	*Package*	*Dielectric*	*Capacitance* (µF)	*Tolerance* (%)	*Voltage Rating (V)*	*Mfgr*
1	GRM188R60J475ME84D	0603	X5R	4.7	20	6.3	Murata
2	GRM188R60J475ME19D	0603	X5R	4.7	20	6.3	Murata
3	GRM188R61A475KE15	0603	X5R	4.7	20	10	Murata
4	GRM155R60G106M	0402	X5R	10	20	4	Murata
5	ADK105BJ106MV-_D	0402	X5R	10	20	4	Taiyo Yuden
6	This is a parallel combination of:						
a	GRM155R61A105K	0402	X5R	1	10	10	Murata
b	GRM155R60J475M	0402	X5R	4.7	20	6.3	Murata

13 Leakage Considerations

To achieve the lowest possible power consumption in low power modes, leakage current must be considered and minimized. The following recommendations will aid in this goal:

- Avoid external pull-up or pull-down resistors:
  - 10 kilohm @ 3.3V = 330 µA, even 100 kilohm @ 3.3V is 33 µA
  - The CYW4325 has internal PU/PD resistors where necessary. These resistors can be turned off when not needed.
  - There are no internal PU/PD resistors on the xRST_N signals. These signals should always be driven from the host.
- Stop the host SDIO clock (or slow it down) for lowest power consumption.
- Consider external components such as LNAs and so on: How much current do they take in their bypass or disable modes?
- Consider shutting off the supply voltages of external components when they are not being used. This can be done using the BBOOST output for their supply or by using an external FET enabled by XTAL_PU.

Document History Page

Document Title: AN214923 - Power Topologies and Regulator Component Guide Document Number: 002-14923				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	02/13/2008	4325-AN600-R Initial release
*A	–	–	07/24/2008	4325-AN601-R **Updated:** • CYW4325 Integrated Regulators on page 2 • Output voltages on Figure 1 on page 3 • Pin count in WLCSP packages on Figure 1 on page 3 • 3.3V Supply on page 3 • 1.25V Supplies on page 4 • VDDIO Supplies on page 4 • All power topology block diagrams and schematic drawings • WLAN Power Amplifier (PA) Supplies on page 25 • Figure 21 on page 26 • Inductor Specifications and Implications on page 28 • Recommended Inductors for the CBUCK Regulator on page 30 • Recommended Inductors for the BBOOST Regulator on page 30 **Added:** • Initializing the LNLDO2 Regulator on page 4 • Low Power States on page 21 • Leakage Considerations on page 32 • Capacitor recommendations • Additional layout recommendations
*B	–	–	05/23/2011	4325-AN602-R Updated: • Regulator Capacitor Considerations on page 31 **Added:** • Table 7, “Recommended Parts for Usage of Alternate Capacitor with the CBUCK Regulator,” on page 32
*C	5466683	UTSV	10/13/2016	Updated in Cypress template Added Cypress part numbering scheme
*D	5840320	AESATMP8	08/01/2017	Updated logo and Copyright.

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709