AN214843

Cypress Bluetooth® SoC, Crystal, TCXO, RFIC, and LPO Application Note

Associated Part Family: CYW43XX/CYW20XX

This application note provides a general guideline and reference for implementation and design of various frequency reference sources (crystal, TCXO, RFIC, and LPO). An overall requirement is presented and discussed. General source-specific issues and solutions are also addressed.

This application note applies to the CYW2046, CYW4325, and CYW4329.

Contents

1 Introduction

This application note provides a general guideline and reference for implementation and design of various frequency reference sources (crystal, TCXO, RFIC, and LPO). An overall requirement is presented and discussed. General source-specific issues and solutions are also addressed.

This application note applies to the CYW2046, CYW4325, and CYW4329

1.1 Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM2046	CYW2046
BCM4325	CYW4325
BCM4329	CYW4329

1.2 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use. For a more complete list of acronyms and other terms used in Cypress documents, go to: http://www.cypress.com/glossary.

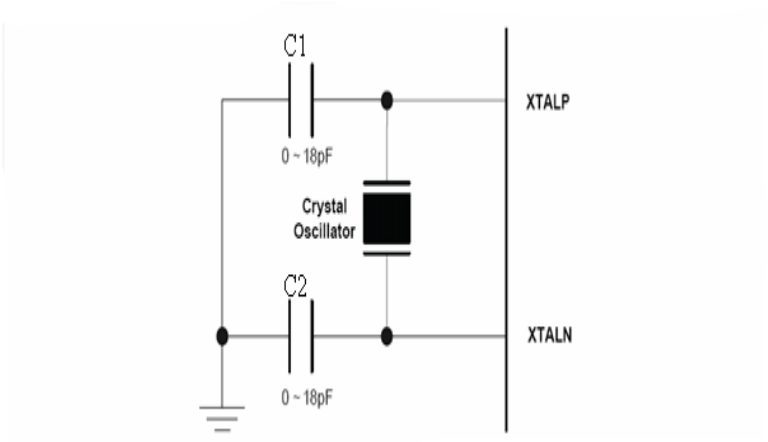
2 IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design.
Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

3 Crystal Oscillator as Frequency Reference

All Cypress Bluetooth chips can use a crystal oscillator as frequency reference. Figure shows the configuration of a parallel resonance crystal and its tuning capacitors.

Figure 1. Recommended Crystal Configuration

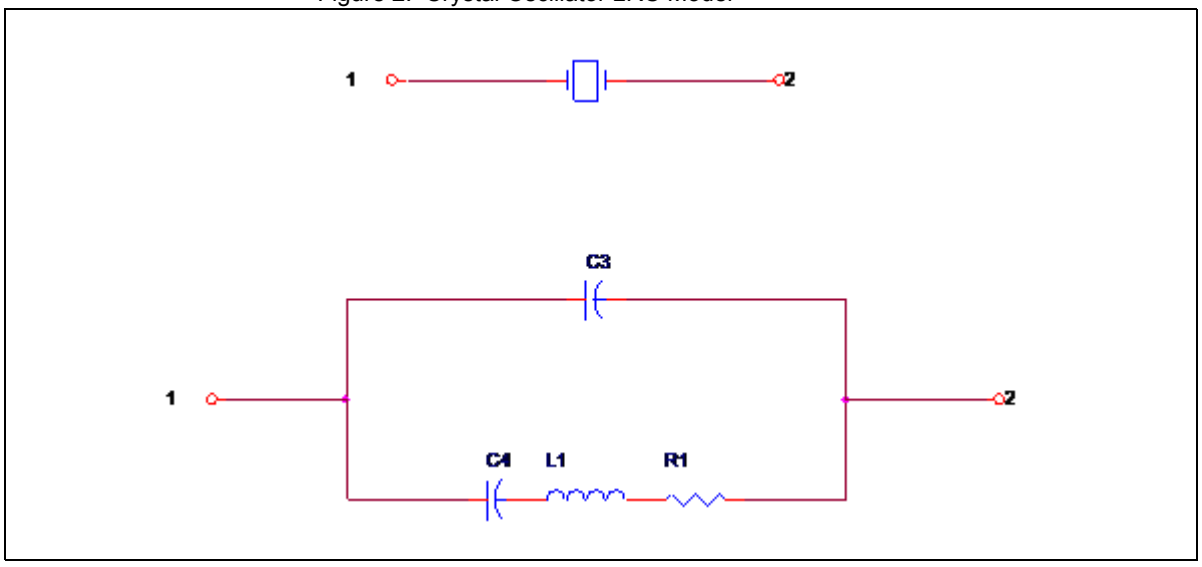


3.1 Crystal Tuning

For a parallel resonance crystal, the resonance frequency can be calculated by:

$$f = \frac{1}{2\pi}\left(\sqrt{\frac{C_4 + C_3}{L_1 \cdot C_4 \cdot C_3}}, C_3 \gg C_4\right)$$

Figure 2. Crystal Oscillator LRC Model



Many crystal manufacturers state a load capacitance in their part specifications. A load capacitance of 9 pF for a 26 MHz crystal means that the crystal is cut so that it will oscillate at 26 MHz, providing a 9 pF total shunt capacitance.

On a PCB with the crystal configuration shown on Figure on page 2, load capacitance can be defined as:

$$C_L = \frac{C_1 \cdot C_2}{C_1 + C_2} + C_{\text{Stray}}$$

where

C_{Stray} is the total stray capacitance present in the circuit.

C_1 and C_2 are shunt tuning capacitors at the input and output pin.

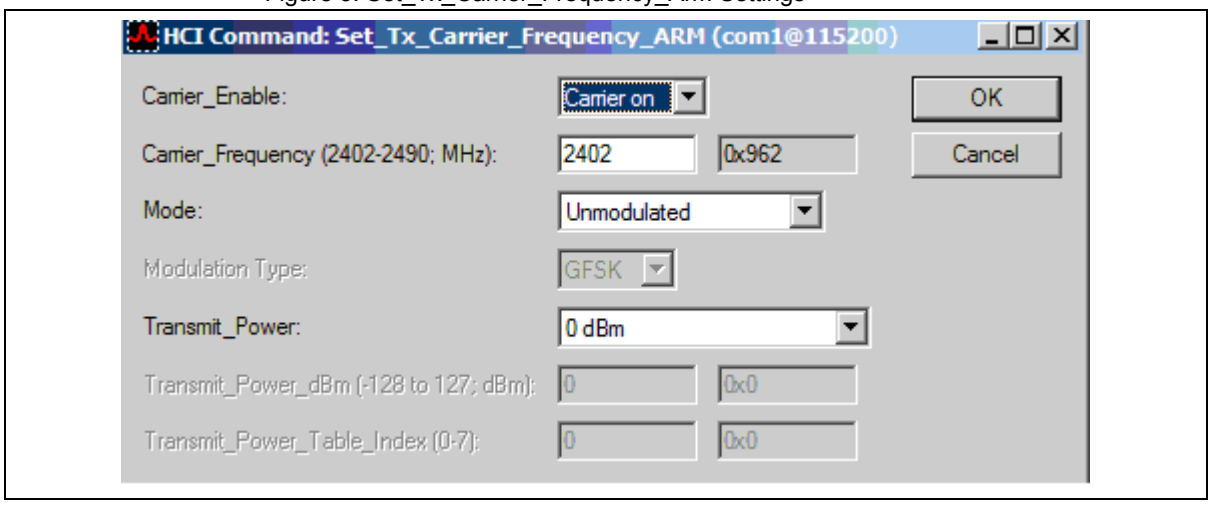
To tune the crystal, start with values of C_1 and C_2 that produce the C_L value stated in the crystal data sheet. Measure the frequency of the crystal on the PCB using a spectrum analyzer and an active probe. If the measured frequency is below the expected value, decrease the values of either C_1 or C_2 or both. If the measured frequency is over the expected value, increase the values of either C_1 or C_2 or both.

3.2 Tuning a Crystal Using BlueTool™

Crystals can also be tuned by measuring the accuracy of the Bluetooth® carrier tone.

1. Interface the device with a host PC running BlueTool™ and connect the RF port of the device to a spectrum analyzer.
2. Set the center frequency of the spectrum analyzer to 2402 MHz with a span of 200 kHz.
3. Issue a **7.0:Set_Tx_carrier_Frequency_ARM** command in **BlueTool** with the settings shown on Figure on page 4.

Figure 3. Set_Tx_Carrier_Frequency_Arm Settings



4. Measure the frequency of the carrier on the spectrum analyzer using a peak marker. If the measured frequency is below the expected value, decrease the values of either C_1 or C_2 or both. If the measured frequency is over the expected value, increase the values of either C_1 or C_2 or both.

For example, using the formula $C_L = \frac{C_1 \cdot C_2}{C_1 + C_2} + C_{\text{Stray}}$ for a load capacitance of 12 pF and a stray capacitance of

3 pF, a 15 pF capacitor at the input pin and a 22 pF capacitor at the output pin make an ideal configuration.

3.3 Choosing a Crystal

The default frequency for crystal reference is 26 MHz. An internal factional-N synthesizer, however, allows for use of many other popular frequencies. Acceptable frequencies are 12, 13, 14.4, 15.36, 16.2, 16.8, 18, 19.2, 19.44, 19.68, 19.8, 20, 24, 26, and 38.4 MHz. Frequencies other than 26 MHz require special tuning. Consult your applications engineer for assistance.

A recommended crystal will have a load capacitance of between 8 and 15 pF, a maximum ESR of 60 ohms, and a maximum ±20 ppm tolerance stability including manufacturing and over-temperature variations. For instance, the Epson® FA-128 crystal has a standard tolerance of ±10 ppm, an over-temperature tolerance of ±10 ppm, and a 10 pF load capacitance.

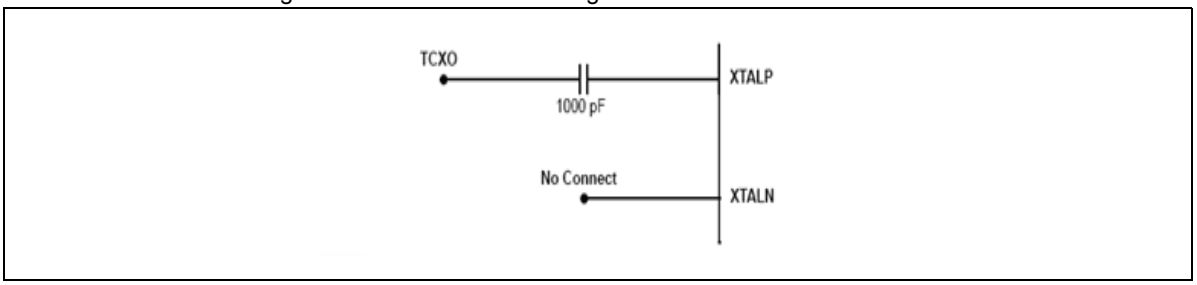
3.4 CYW2045 Specific Crystal Considerations

For the CYW2045, a 1 MΩ shunt resistor is required on the oscillator input (XTAL_P) pin. This resistor is not required for other Cypress Bluetooth chips. This resistor is not required for any clock sources other than a crystal oscillator.

3.4.1 TCXO as Frequency Reference

A temperature-compensated external oscillator (TXCO) can also be used as a frequency reference. The loading on the external clock generation device will not change when the Cypress chip is powered on or off. Figure 2 shows the configuration for using a TCXO.

Figure 4. Recommended Configuration for TCXO



4 Signal Characteristics for External Frequency Reference

The clock signal provided to the Cypress Bluetooth IC by any device must meet the specifications presented in the data sheet. As an example, the characteristics of the clock signal for CYW2046 are shown in Table 2. The required specification might be different for some chips. Consult the corresponding chip data sheet for detailed specifications.

Table 2. CYW2046 Clock Signal Characteristics

Parameter	Value	Unit
Input signal amplitude	400 – VDDRF	mV p-p
Signal shape	Square or sine wave	–
Input impedance	≥ 1 megohm, ≤ 2 pF	–
Phase noise		
@ 1 kHz	≤ 100	dBc/Hz
@ 10 kHz	≤ 115	dBc/Hz
@100 kHz	≤ 120	dBc/Hz
@1 MHz	≤ 140	dBc/Hz
Autodetection frequencies when using external LPO	12,13,14.4,15.36,16.2,16.8, 18,19.2, 19.44, 19.68, 19.8, 20, 24, 26, and 38.4	MHz
Tolerance (over-temperature)	±20	ppm

5 Signal Amplitude and Shape Adjustments

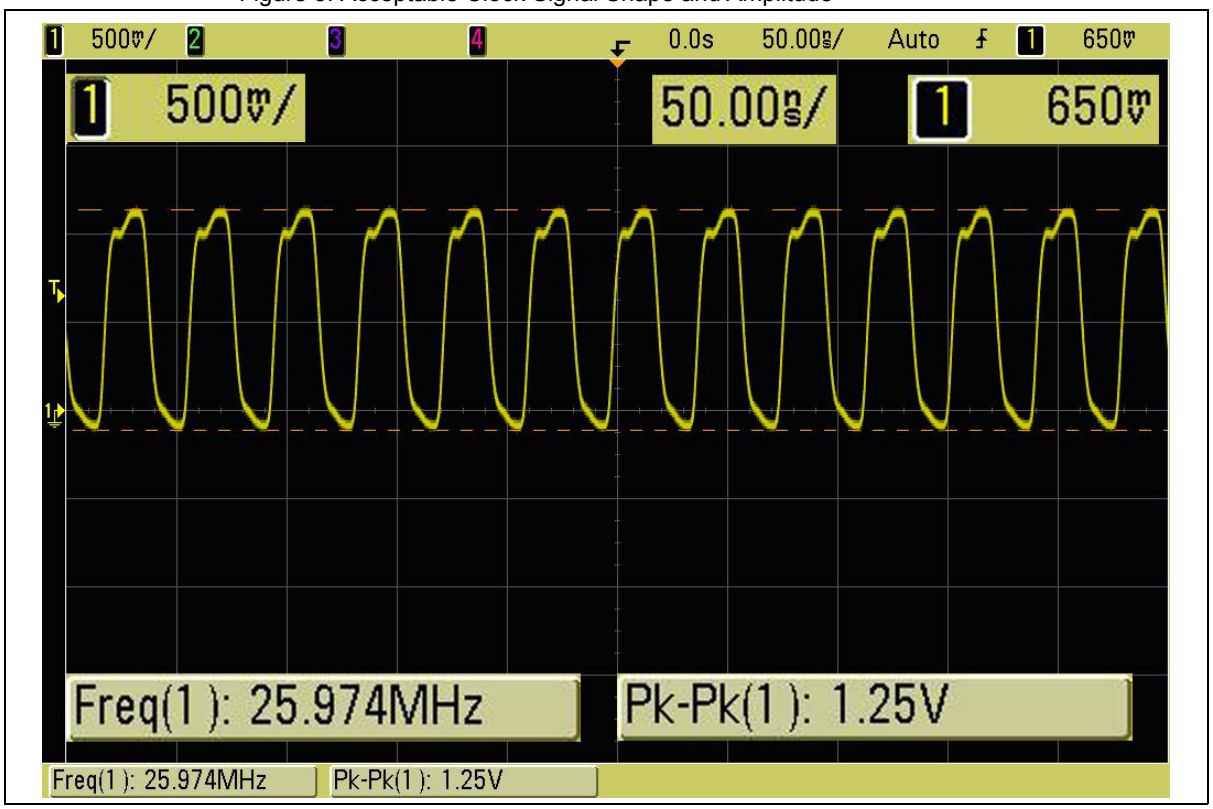
If the p-p swing of the input clock signal is greater than VDDRF, a series capacitor on the input pin can be used to adjust the p-p voltage swing. If the input signal is DC-coupled, use a series capacitor to remove the DC component. Recommended values are 1000 pF or 100 pF. The p-p swing of the signal decreases as the value of the series capacitor decreases. A series 0402 × 7R 1000 pF capacitor, for example, has an impedance of about 6 ohms at 26 MHz, which is low impedance while providing adequate DC blocking. A resistor divider circuit should not be used to reduce the p-p swing of the signal because it can adversely affect the signal shape.

A series capacitor is also used to produce a desired signal shape; nevertheless, care must be taken not to overly distort the shape and amplitude of the clock.

Note that frequency values other than 26 MHz may require special tuning. Consult the field application engineer (FAE) for assistance.

If the amplitude of the clock signal is too small, it can cause degradations in modulation characteristics and DEVM performance of the Bluetooth transceiver. Consult Cypress Bluetooth application engineers when using amplitudes below 600 mV p-p. An acceptable clock shape and amplitude is illustrated on Figure 5.

Figure 5. Acceptable Clock Signal Shape and Amplitude



6 TCXO and Sleep Mode

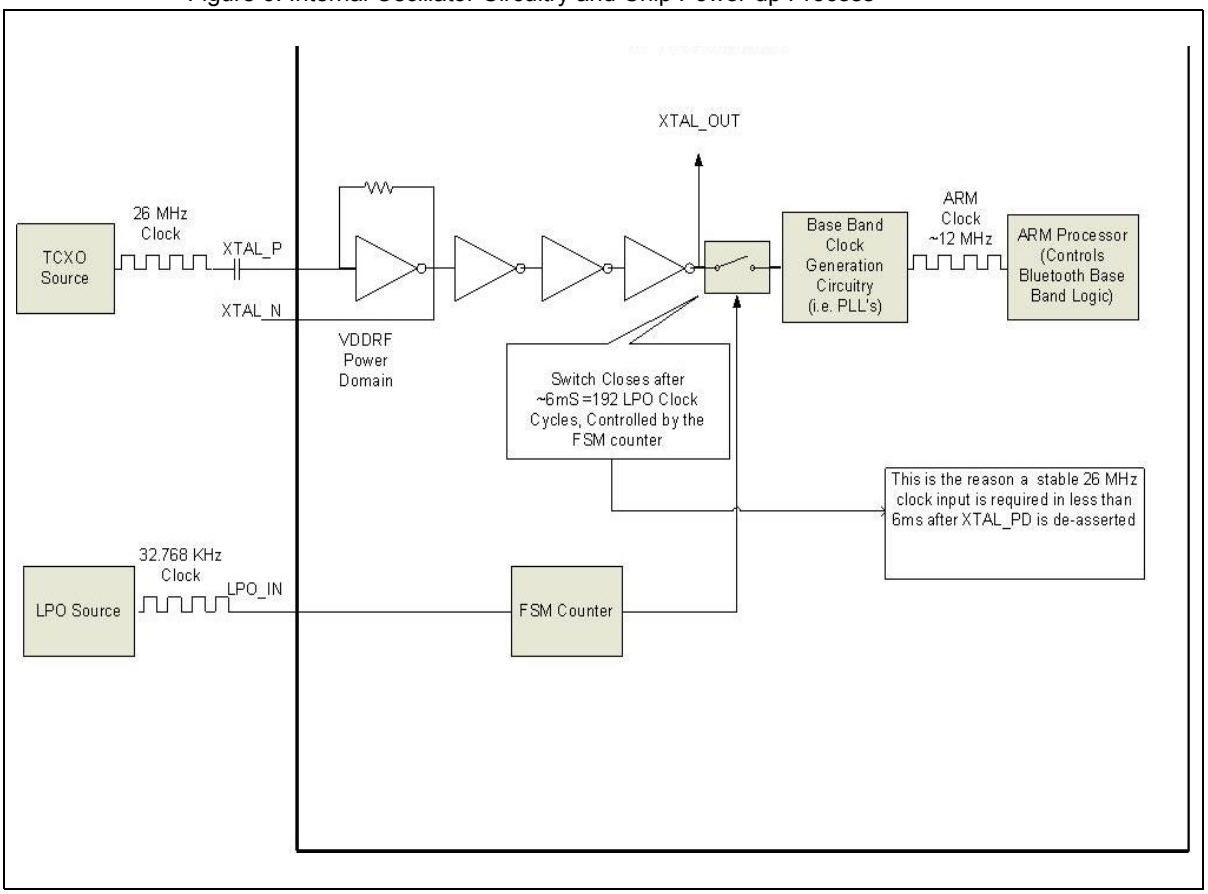
If a TCXO is used as frequency reference, it must be shut down when the Cypress chip enters sleep mode to conserve power. GPIO5 can act as Clock Power-Down or Power-Up signal (XTAL_PD or CLK_REQ). The polarity of this signal can be controlled by the digital state of TM0. Note that TM1 and TM2 are to be pulled low. Refer to the product-specific data sheet for the relationship between theTM0 state and the polarity of the XTALPU/XTAL_PD signal.

The low voltage level for GPIO5 and TM0 is 0V, and the high voltage level for TM0 and GPIO5 is VDDIO.

Note: For some chips, such as the CYW4325 and CYW4329, a dedicated XTAL_PU pin handles this role instead of GPIO5

When the chip is awoken in a sniff window or by the host, it deasserts the XTAL_PD signal. A stable clock signal must be provided in less than 6 ms after XTAL_PD is deasserted. If a stable clock is not provided within 6 ms or less, it can cause the ARM® processor to be driven by an invalid clock signal. This can put the internal logic block in an indeterminate state. After the internal logic enters an indeterminate state, it will no longer respond to host commands or will be unable to process Bluetooth functions. During the chip start-up process, GPIO5 is asserted immediately after the core is powered up, and an stable clock must be provided within 6 ms as well. Figure illustrates the chip power-up process and internal circuitry that imposes the 6 ms maximum delay requirement.

Figure 6. Internal Oscillator Circuitry and Chip Power-up Process

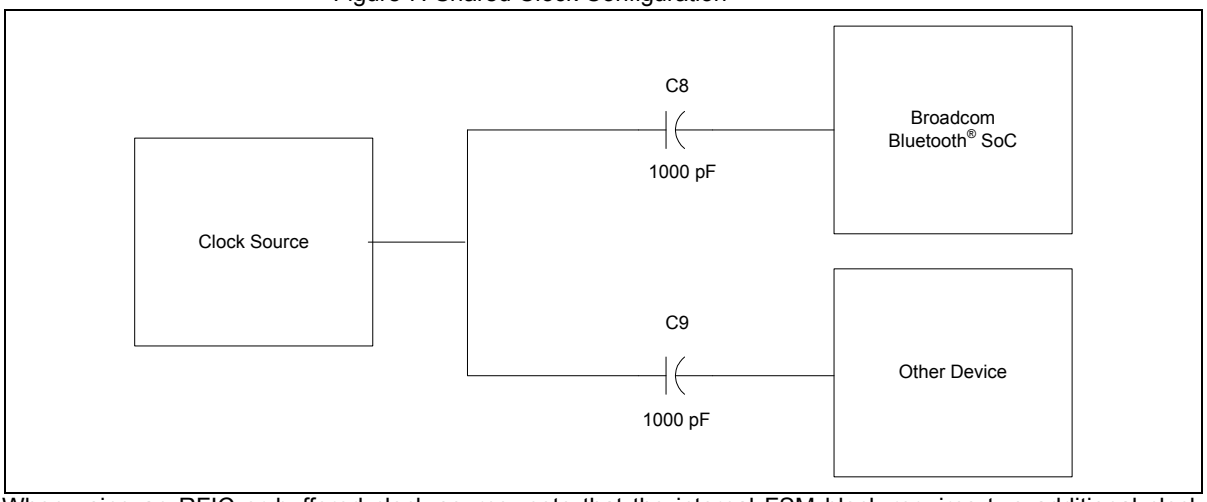


7 RFIC/Buffered Clocks as Frequency Reference

The frequency reference can also be provided by an RFIC or buffered clock source. This clock signal is often shared with other devices.

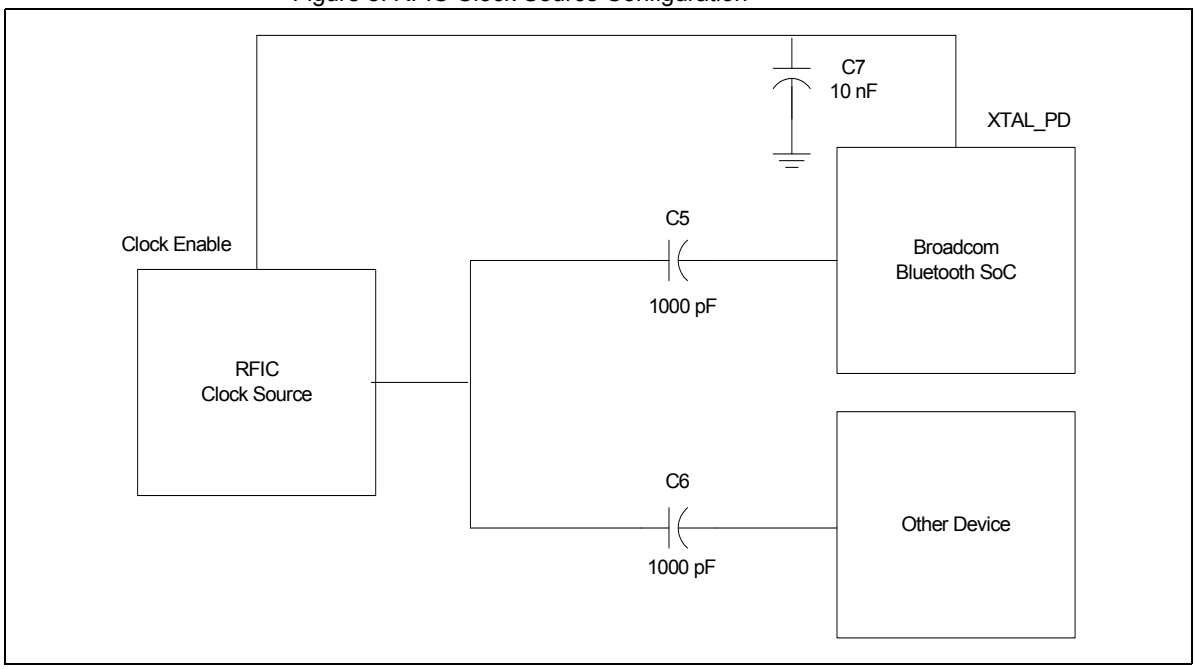
The required signal specification is similar to a signal provided by a TCXO. Special care must be taken when using buffered or shared clocks to ensure that clock quality is consistent. Signal quality, phase noise, shape, and amplitude must not be altered at any time. For instance, if another device is using the shared clock, it should not introduce digital noise into the signal or cause the clock frequency to drift. Series capacitors can be used to decouple shared clock signals.

Figure 7. Shared Clock Configuration



When using an RFIC or buffered clock source, note that the internal FSM block requires two additional clock cycles after XTAL_PD (GPIO5) is asserted to correctly disable internal oscillator and BT baseband blocks. If the RFIC clock is disabled too quickly after XTAL_PD is asserted, it can cause additional current draw in sleep mode due to improper shutdown of internal blocks. The required delay between XTAL_PD and Clock signal shut-off is 100 ns. If the delay is too small, it can be increased by using a shunt capacitor on the XTAL_PD signal. A 10 nF capacitor will provide enough delay. Note that this is not required for TCXO clock sources because they have a slower shut-off time.

Figure 8. RFIC Clock Source Configuration



8 Layout Considerations for Clock Traces

Clock traces must be kept well isolated from all noisy signals including PCM, UART, SDIO, Flash, and other digital signals. Keep the traces as short as possible and run on a minimum number of layers. Ensure the clock generation device has proper grounding and a clean supply. Routing the clocks near RF inputs may result in degraded or failing RF performance. Therefore, be careful not to route the clocks near RF inputs.

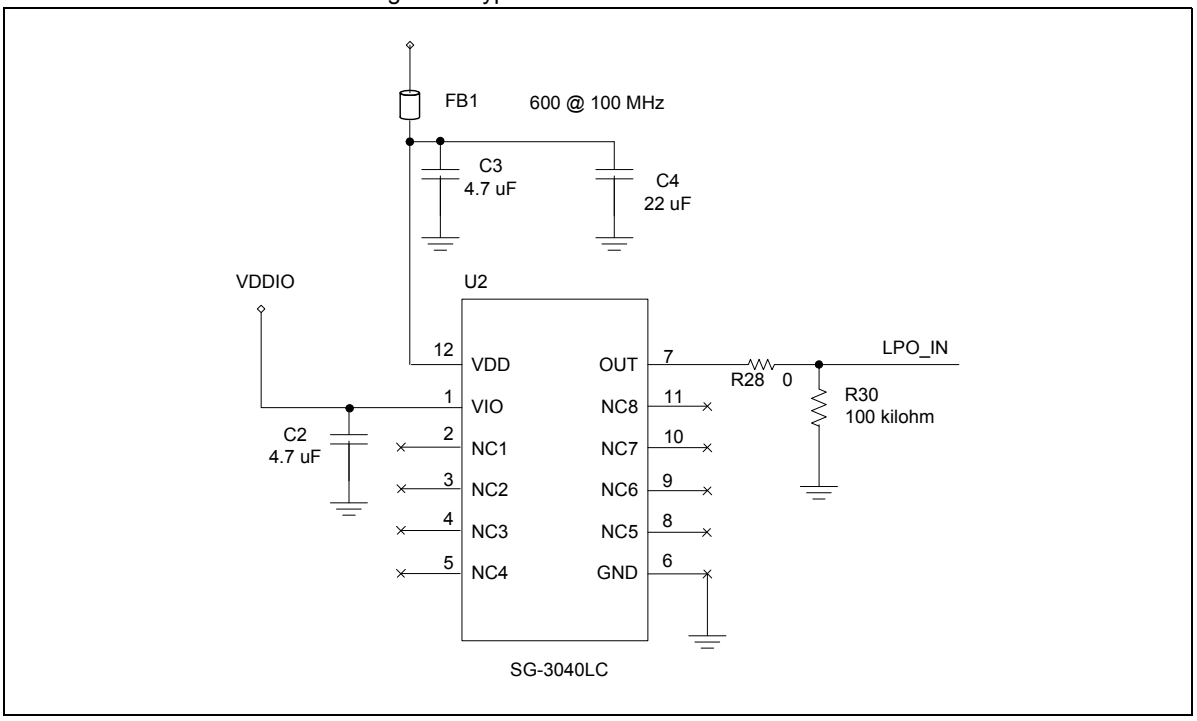
9 32.768 kHz External LPO Clock

The External 32.768 kHz LPO clock provides low power mode timing for Hold, Sleep, and Sniff modes. This clock can be generated by an oscillator or other clock generation circuitry. Note that the internal LPO clock cannot be used in chips with FM functionality or cell phone/embedded designs where accurate sniff intervals are needed. If the internal LPO is used, the LPO input pin must be pulled down. A DC blocking capacitor is not needed for this clock. If the chip is configured to use an external LPO, an accurate and stable signal is necessary upon POR. The maximum signal level must remain less than 1800 mV p-p to ensure that the device does not draw excessive current when the Bluetooth chip is in deep sleep mode. In a case in which the p-p swing of the LPO clock is over 1800 mV, additional current is drawn from the source that supplies the clock generation circuitry (VDD3P3 on Figure). The additional current draw is dependent on the circuit and/or device. A maximum signal level of 3600 mV, however, can be tolerated in most cases. In many 32.768 kHz oscillator packages, p-p swing can be adjusted by applying the desired voltage level to a specified pin (VIO pin on Figure). Figure shows a typical LPO circuit using an EPSON SG-3040LC 32.768 kHz oscillator.

10 Automatic Frequency Detection

For automatic frequency detection to function correctly, an external 32.768 kHz LPO clock must be present and stable during power-on reset.

Figure 9. Typical LPO Circuit



11 External 32 kHz Reference for FM

An external 32.768 kHz oscillator also provides the reference frequency for the FM block in chips with FM RX or TX features. Care must be taken to ensure the quality of the signal. The traces carrying the clock signal must be properly shielded and kept away from all noise sources. Also a clean supply must be provided to the clock generation circuitry. As shown on Figure on page 9, supply cleanliness is ensured by use of a 600 ohm ferrite bead (FB1) and decoupling capacitors (C_3 and C_4).

For CYW4325 and CYW4329, the amplitude of the signal must also be kept below 1800 mV p-p to prevent degradation in the FM performance. For other FM-specific LPO clock considerations and information, refer to the chip data sheets for CYW4325, and CYW4329.

12 LPO Clock Specifications

For devices without the FM option, the requirements of Table 3 apply to the 32.768 kHz LPO clock.

Table 3. 32.768 kHz LPO Clock Requirements for Devices Without the FM Option

Parameter	Description
Frequency error	±200 ppm maximum
Duty cycle	30% to 70%
Amplitude	1.8 Vp-p to avoid additional current consumption. 3.3 Vp-p maximum.

For devices with the FM option, the requirements of Table 4 generally apply to the 32.768 kHz LPO clock.

Table 4. 32.768 kHz LPO Clock Requirements for Devices with the FM Option

Parameter	Description
Frequency error	If FM Rx is used: ±150 ppm maximum with frequency error indication, ±50 ppm without frequency error indication. If FM Tx is used: ±100 ppm maximum with frequency error indication, ±50 ppm without frequency error indication.
Duty cycle	30% to 70%
Jitter	Less than 1 Hz, integrated from 300 Hz to 15 kHz
Amplitude	1.8 Vp-p to avoid additional current consumption and degradation in FM SNR. 3.3 Vp-p maximum.

Note:

1.1 Hz frequency error is equal to 30.5 ppm.

2.Failure to meet the duty cycle requirement will cause gross failures.

3.Failure to meet the jitter requirement will cause degradation in FM mono and stereo SNR.

4.Failure to meet the frequency error requirements will cause degradation in FM mono and stereo SNR and FM channel search robustness.

Document History Page

Document Title: AN214843 - Cypress Bluetooth® SoC, Crystal, TCXO, RFIC, and LPO Application Note Document Number: 002-14843				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	06/27/2008	43XX_20XX-AN100-R Initial release
*A	–	–	08/29/2008	43XX_20XX-AN101-R **Updated:** • "TCXO and Sleep Mode"
*B	–	–	01/26/2009	43XX_20XX-AN102-R **Added:** • "LPO Clock Specifications"
*C	–	–	05/18/2009	43XX_20XX-AN103-R **Updated:** • "Introduction" • "TCXO and Sleep Mode" Table 2
*D	–	–	01/22/2010	43XX_20XX-AN104-D1: **Updated:** • Table 3: "32.768 kHz LPO Clock Requirements for Devices with the FM Option,"
*E	5528218	UTSV	12/19/2016	Updated to Cypress template. Added Cypress part numbering scheme
*F	5821309	AESATMP8	07/17/2017	Updated logo and Copyright.

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709