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Spec No: 002-14801

Spec Title: AN214801 - 2-WIRE, 3-WIRE, AND 4-WIRE COEXISTENCE

Replaced by: NONE

AN214801

2-Wire, 3-Wire, and 4-Wire Coexistence

Associated Part Family: CYW20710

This document provides pin assignment information about 2-wire, 3-wire, and 4-wire Bluetooth/WLAN coexistence schemes for Cypress customers to use when configuring devices equipped with the CYW20710 chip.

1 About this Document

1.1 Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM20710	CYW20710

1.2 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use. For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: www.cypress.com/glossary.

2 IoT Resources

Cypress provides a wealth of data at http://www.cypress.com/internet-things-iot to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (http://community.cypress.com/).

3 CYW20710 2-Wire, 3-Wire, and 4-Wire Coexistence

3.1 2-Wire Coexistence

The CYW20710 Bluetooth (BT) solution provides a simple two-wire coexistence scheme.

Two wires are defined and have dedicated pins on the CYW20710 fpBGA package (20710CA0KUFBXG), as shown in Table 2. The WLBGA package (20710A0KUBXG) has the 2-wire coex pins multiplexed on the pins shown in Table 3.

For UART transport operation, the SCL pin for the WLBGA package must not be driven low when the BT device powers up. The Host pin that drives the SCL input must either drive high or float upon BT power up. Once the BT device asserts UART_CTS, then the Host can drive the SCL input to any state. If SCL is driven low upon the BT device power up, it selects SPI transport operation.

Table 2. CYW20710 fpBGA Two-Wire Pin Assignments

Coexistence Signal	802.11 Names	Pin Assignment
BT_ACTIVITY	TX_REQUEST	COEX_OUT0
WLAN_ACTIVITY	TX_CONFIRM_STATUS	COEX_IN

Table 3. CYW20710 WLBGA Two-Wire Pin Assignments

Coexistence Signal	802.11 Names	Pin Assignment
BT_ACTIVITY	TX_REQUEST	SPIM_CS_N (COEX_OUT0)
WLAN_ACTIVITY	TX_CONFIRM_STATUS	GPIO_0 (COEX_IN)

Table 4. Additional Pin Mapping for the CYW20710 WLBGA Package

Host Side	802.11 Names	Pin Assignment
GPIO_x (BT_WAKE)	Not applicable	SCL (BT_WAKE)
GPIO_x (HOST_WAKE)	Not applicable	GPIO_1 (HOST_WAKE)

The config file must have the 2-wire coex patch entry added to the baseline for the coexistence to operate properly. The supporting Broadcom software application engineer can include this patch in the config file.

3.2 3-Wire Coexistence

The CYW20710 Bluetooth solution follows the guidelines of IEEE 802.15.2, which recommends that a 3-wire coexistence scheme be provided. Priority and status information are passed between the BT and WLAN devices. Table 5 shows how the three wires are defined for the CYW20710 fpBGA package (20710CA0KUFBXG). The WLBGA package (20710A0KUBXG) has the 3-wire coex pins multiplexed on the pins shown in Table 6. Figure 1 shows the 3-wire coexistence block diagram proposed by the IEEE802.15.2 recommended practice Packet Traffic Arbitration (PTA) scheme. The PTA is provided by the WLAN module. The Bluetooth module interfaces with the PTA by way of three pins defined as:

- WLAN_ACTIVITY [TX_CONFIRM (STATUS)] — Driven by PTA to signal BT/WLAN priority.
- BT_ACTIVITY (TX_REQUEST) — Driven by the Bluetooth device to signal BT_ACTIVITY.
- BT_PRIORITY_AND_STATUS — Driven by the Bluetooth device to signal Rx/Tx and High/Normal priority.

Table 5. CYW20710 fpBGA 3-Wire Pin Assignment

Coexistence Signal	802.11 Names	CYW20710 fpBGA Pin Assignment
BT_PRIORITY_AND_STATUS	STATUS	COEX_OUT1
BT_ACTIVITY	TX_REQUEST	COEX_OUT0
WLAN_ACTIVITY	TX_CONFIRM_STATUS	COEX_IN

Table 6. CYW20710 WLBGA Three-Wire GPIO Pin Assignment

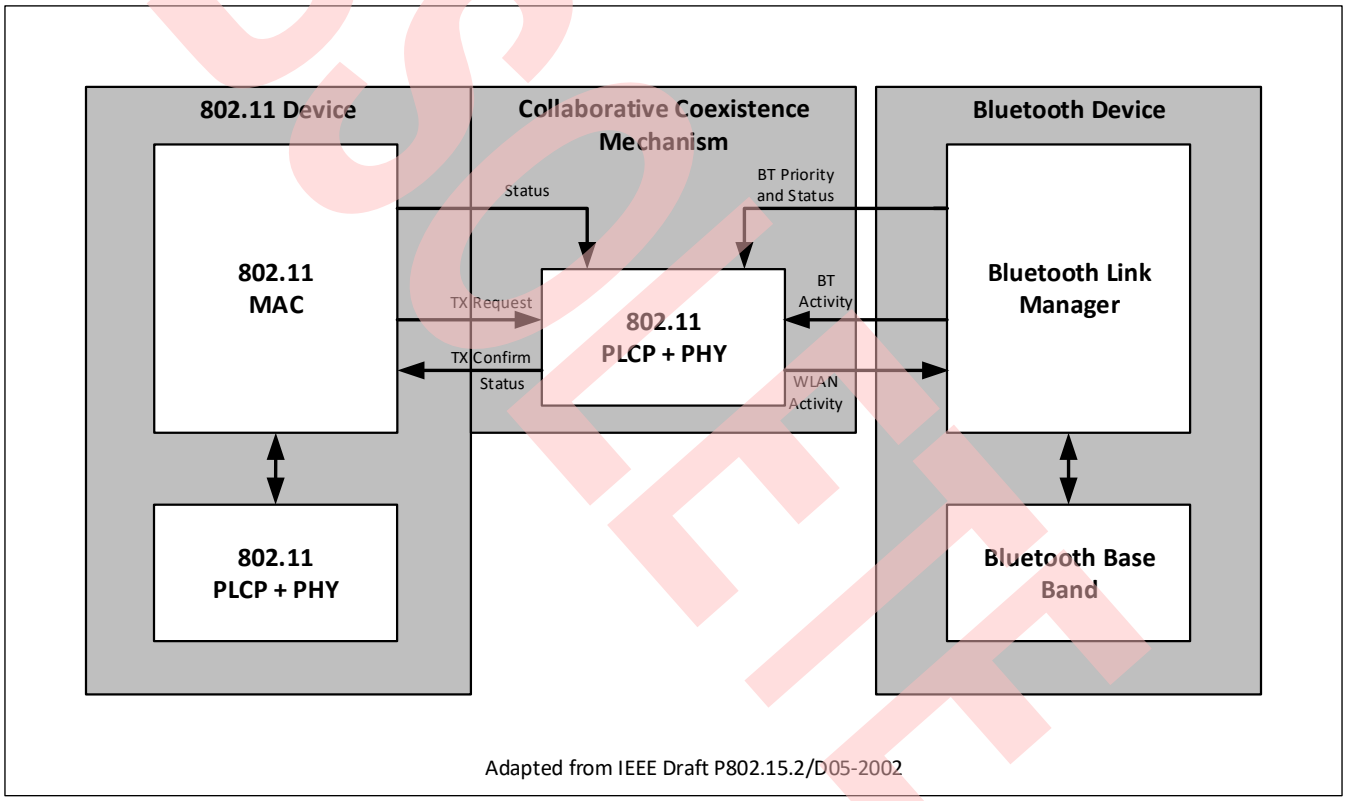
Coexistence Signal	802.11 Names	CYW20710 WLBGA Pin Assignment
BT_PRIORITY_AND_STATUS	STATUS	SPIM_CLK (COEX_OUT1)
BT_ACTIVITY	TX_REQUEST	OTP_DIS (COEX_OUT0)
WLAN_ACTIVITY	TX_CONFIRM_STATUS	GPIO_1 (COEX_IN)

Table 7. Additional Pin Mapping for the CYW20710 WLBGA Package

Host Side	802.11 Names	CYW20710 WLBGA Pin Assignment
GPIO_x (BT_WAKE)	Not applicable	GPIO_0 (BT_WAKE)
GPIO_x (HOST_WAKE)	Not applicable	SPIM_CS_N (HOST_WAKE)

The config file must have the 3-wire coex patch entry added to the baseline for the coexistence to operate properly. The supporting Broadcom software application engineer can include this patch in the config file.

Figure 1. IEEE 802.11 b/g Bluetooth Coexistence Mechanism Structure



3.3 4-Wire Coexistence

An additional coex pin, COEX_OUT2, is added for 4-wire coexistence. This pin is the second bit in combination with the COEX_OUT1 (BT_STATUS) bit for priority signaling. This pin is mapped to GPIO_7 on the fpBGA package, as shown in Table 8. On the WLBGA package, this pin is mapped to the SDA pin as shown in Table 9. On the CYW20710, the SDA pin is no longer used to detect SDIO transport. Therefore, this pin can be multiplexed as COEX_OUT2.

Table 8. CYW20710 fpBGA Four-Wire Pin Assignment

Coexistence Signal	802.11 Names	CYW20710 fpBGA Pin Assignment
BT_PRIORITY_AND_STATUS	STATUS	COEX_OUT1
BT_ACTIVITY	TX_REQUEST	COEX_OUT0
WLAN_ACTIVITY	TX_CONFIRM_STATUS	COEX_IN
BT_STATUS_2	Not applicable	GPIO_7 (COEX_OUT2)

Table 9. CYW20710 WLBGA 4-Wire Pin Assignment

Coexistence Signal	802.11 Names	CYW20710 WLBGA Pin Assignment
BT_PRIORITY_AND_STATUS	STATUS	SPIM_CLK (COEX_OUT1)
BT_ACTIVITY	TX_REQUEST	OTP_DIS (COEX_OUT0)
WLAN_ACTIVITY	TX_CONFIRM_STATUS	GPIO_1 (COEX_IN)
BT_STATUS_2	Not applicable	SDA (COEX_OUT2)

Table 10. Additional Pin Mapping for the WLBGA Package

Host Side	802.11 Names	20710 WLBGA Pin Assignment
GPIO_x (BT_WAKE)	Not applicable	SPIM_CS_N (HOST_WAKE)
GPIO_x (HOST_WAKE)	Not applicable	SPIM_CS_N (HOST_WAKE)

The config file must have the 4-wire coex patch entry added to the baseline for the coexistence to operate properly. The supporting Broadcom software application engineer can include this patch in the config file.

Document History

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Document Number: 002-14801

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**			02/02/2011	20710-AN200-R Initial release
*A	5464818	UTSV	10/06/2016	Updated in Cypress template. Added Cypress Part Numbering Scheme.
*B	5827745	AESATP12	07/21/2017	Updated logo and copyright.
*C	6506125	WENL	03/11/2019	Obsoleted

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