



Please note that Cypress is an Infineon Technologies Company.

The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content

The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers

Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.



THIS SPEC IS OBSOLETE

Spec No: 002-14801

Spec Title: AN214801 - 2-WIRE, 3-WIRE, AND 4-WIRE
COEXISTENCE

Replaced by: NONE

2-Wire, 3-Wire, and 4-Wire Coexistence

Associated Part Family: CYW20710

This document provides pin assignment information about 2-wire, 3-wire, and 4-wire Bluetooth/WLAN coexistence schemes for Cypress customers to use when configuring devices equipped with the CYW20710 chip.

1 About this Document

1.1 Cypress Part Numbering Scheme

Cypress is converting the acquired IoT part numbers from Broadcom to the Cypress part numbering scheme. Due to this conversion, there is no change in form, fit, or function as a result of offering the device with Cypress part number marking. The table provides Cypress ordering part number that matches an existing IoT part number.

Table 1. Mapping Table for Part Number between Broadcom and Cypress

Broadcom Part Number	Cypress Part Number
BCM20710	CYW20710

1.2 Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use. For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: www.cypress.com/glossary.

2 IoT Resources

Cypress provides a wealth of data at <http://www.cypress.com/internet-things-iot> to help you to select the right IoT device for your design, and quickly and effectively integrate the device into your design. Cypress provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates. Customers can acquire technical documentation and software from the Cypress Support Community website (<http://community.cypress.com/>).

3 CYW20710 2-Wire, 3-Wire, and 4-Wire Coexistence

3.1 2-Wire Coexistence

The CYW20710 Bluetooth (BT) solution provides a simple two-wire coexistence scheme.

Two wires are defined and have dedicated pins on the CYW20710 fpBGA package (20710CA0KUF BXG), as shown in Table 2. The WL BGA package (20710A0KUBXG) has the 2-wire coex pins multiplexed on the pins shown in Table 3.

For UART transport operation, the SCL pin for the WL BGA package must not be driven low when the BT device powers up. The Host pin that drives the SCL input must either drive high or float upon BT power up. Once the BT device asserts UART_CTS, then the Host can drive the SCL input to any state. If SCL is driven low upon the BT device power up, it selects SPI transport operation.

Table 2. CYW20710 fpBGA Two-Wire Pin Assignments

Coexistence Signal	802.11 Names	Pin Assignment
BT_ACTIVITY	TX_REQUEST	COEX_OUT0
WLAN_ACTIVITY	TX_CONFIRM_STATUS	COEX_IN

Table 3. CYW20710 WLPGA Two-Wire Pin Assignments

Coexistence Signal	802.11 Names	Pin Assignment
BT_ACTIVITY	TX_REQUEST	SPIM_CS_N (COEX_OUT0)
WLAN_ACTIVITY	TX_CONFIRM_STATUS	GPIO_0 (COEX_IN)

Table 4. Additional Pin Mapping for the CYW20710 WLPGA Package

Host Side	802.11 Names	Pin Assignment
GPIO_x (BT_WAKE)	Not applicable	SCL (BT_WAKE)
GPIO_x (HOST_WAKE)	Not applicable	GPIO_1 (HOST_WAKE)

The config file must have the 2-wire coex patch entry added to the baseline for the coexistence to operate properly. The supporting Broadcom software application engineer can include this patch in the config file.

3.2 3-Wire Coexistence

The CYW20710 Bluetooth solution follows the guidelines of IEEE 802.15.2, which recommends that a 3-wire coexistence scheme be provided. Priority and status information are passed between the BT and WLAN devices. Table 5 shows how the three wires are defined for the CYW20710 fpBGA package (20710CA0KUF BXG). The WLPGA package (20710A0KUBXG) has the 3-wire coex pins multiplexed on the pins shown in Table 6. Figure 1 shows the 3-wire coexistence block diagram proposed by the IEEE802.15.2 recommended practice Packet Traffic Arbitration (PTA) scheme. The PTA is provided by the WLAN module. The Bluetooth module interfaces with the PTA by way of three pins defined as:

- WLAN_ACTIVITY [TX_CONFIRM (STATUS)] — Driven by PTA to signal BT/WLAN priority.
- BT_ACTIVITY (TX_REQUEST) — Driven by the Bluetooth device to signal BT_ACTIVITY.
- BT_PRIORITY_AND_STATUS — Driven by the Bluetooth device to signal Rx/Tx and High/Normal priority.

Table 5. CYW20710 fpBGA 3-Wire Pin Assignment

Coexistence Signal	802.11 Names	CYW20710 fpBGA Pin Assignment
BT_PRIORITY_AND_STATUS	STATUS	COEX_OUT1
BT_ACTIVITY	TX_REQUEST	COEX_OUT0
WLAN_ACTIVITY	TX_CONFIRM_STATUS	COEX_IN

Table 6. CYW20710 WLBGA Three-Wire GPIO Pin Assignment

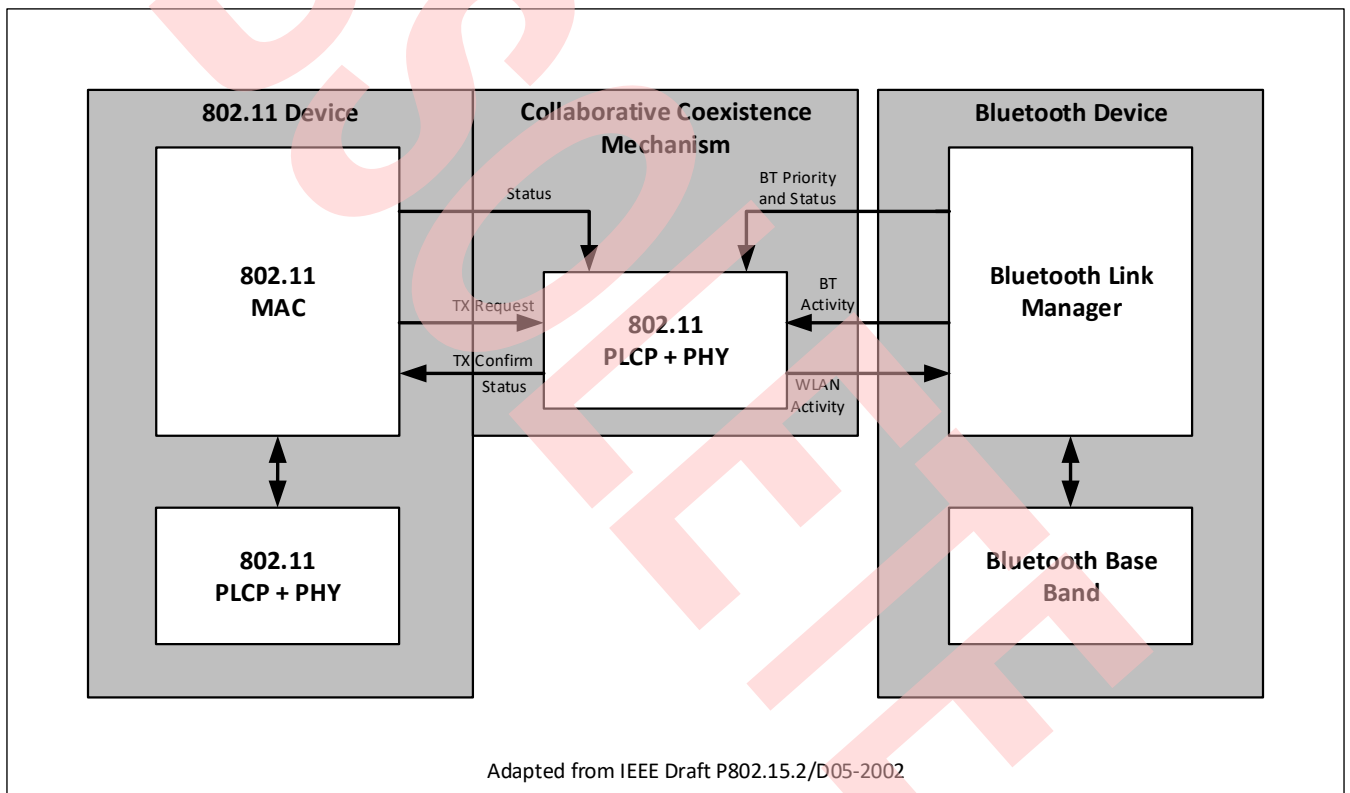
Coexistence Signal	802.11 Names	CYW20710 WLBGA Pin Assignment
BT_PRIORITY_AND_STATUS	STATUS	SPIM_CLK (COEX_OUT1)
BT_ACTIVITY	TX_REQUEST	OTP_DIS (COEX_OUT0)
WLAN_ACTIVITY	TX_CONFIRM_STATUS	GPIO_1 (COEX_IN)

Table 7. Additional Pin Mapping for the CYW20710 WLBGA Package

Host Side	802.11 Names	CYW20710 WLBGA Pin Assignment
GPIO_x (BT_WAKE)	Not applicable	GPIO_0 (BT_WAKE)
GPIO_x (HOST_WAKE)	Not applicable	SPIM_CS_N (HOST_WAKE)

The config file must have the 3-wire coex patch entry added to the baseline for the coexistence to operate properly. The supporting Broadcom software application engineer can include this patch in the config file.

Figure 1. IEEE 802.11 b/g Bluetooth Coexistence Mechanism Structure



3.3 4-Wire Coexistence

An additional coex pin, COEX_OUT2, is added for 4-wire coexistence. This pin is the second bit in combination with the COEX_OUT1 (BT_STATUS) bit for priority signaling. This pin is mapped to GPIO_7 on the fpBGA package, as shown in Table 8. On the WLBGA package, this pin is mapped to the SDA pin as shown in Table 9. On the CYW20710, the SDA pin is no longer used to detect SDIO transport. Therefore, this pin can be multiplexed as COEX_OUT2.

Table 8. CYW20710 fpBGA Four-Wire Pin Assignment

Coexistence Signal	802.11 Names	CYW20710 fpBGA Pin Assignment
BT_PRIORITY_AND_STATUS	STATUS	COEX_OUT1
BT_ACTIVITY	TX_REQUEST	COEX_OUT0
WLAN_ACTIVITY	TX_CONFIRM_STATUS	COEX_IN
BT_STATUS_2	Not applicable	GPIO_7 (COEX_OUT2)

Table 9. CYW20710 WLBGA 4-Wire Pin Assignment

Coexistence Signal	802.11 Names	CYW20710 WLBGA Pin Assignment
BT_PRIORITY_AND_STATUS	STATUS	SPIM_CLK (COEX_OUT1)
BT_ACTIVITY	TX_REQUEST	OTP_DIS (COEX_OUT0)
WLAN_ACTIVITY	TX_CONFIRM_STATUS	GPIO_1 (COEX_IN)
BT_STATUS_2	Not applicable	SDA (COEX_OUT2)

Table 10. Additional Pin Mapping for the WLBGA Package

Host Side	802.11 Names	20710 WLBGA Pin Assignment
GPIO_x (BT_WAKE)	Not applicable	SPIM_CS_N (HOST_WAKE)
GPIO_x (HOST_WAKE)	Not applicable	SPIM_CS_N (HOST_WAKE)

The config file must have the 4-wire coex patch entry added to the baseline for the coexistence to operate properly. The supporting Broadcom software application engineer can include this patch in the config file.

Document History

Document Title: AN214801 - 2-Wire, 3-Wire, and 4-Wire Coexistence

Document Number: 002-14801

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**			02/02/2011	20710-AN200-R Initial release
*A	5464818	UTSV	10/06/2016	Updated in Cypress template. Added Cypress Part Numbering Scheme.
*B	5827745	AESATP12	07/21/2017	Updated logo and copyright.
*C	6506125	WENL	03/11/2019	Obsoleted

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

Arm® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6 MCU](#)

Cypress Developer Community

[Community](#) | [Projects](#) | [Videos](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

All other trademarks or registered trademarks referenced herein are the property of their respective owners.



Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709

© Cypress Semiconductor Corporation, 2011-2019. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress does not assume any liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.