AN212930

How to Use Partial Wakeup for Traveo™ Family

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Associated Part Family: Traveo Family S6J3110/3360/3370/3400 series

Related Documents: for a complete list, Related Documents

This application note describes how to use the partial wakeup feature of the Traveo™ family S6J3110/3360/3370/3400 series.

Contents

1 Introduction

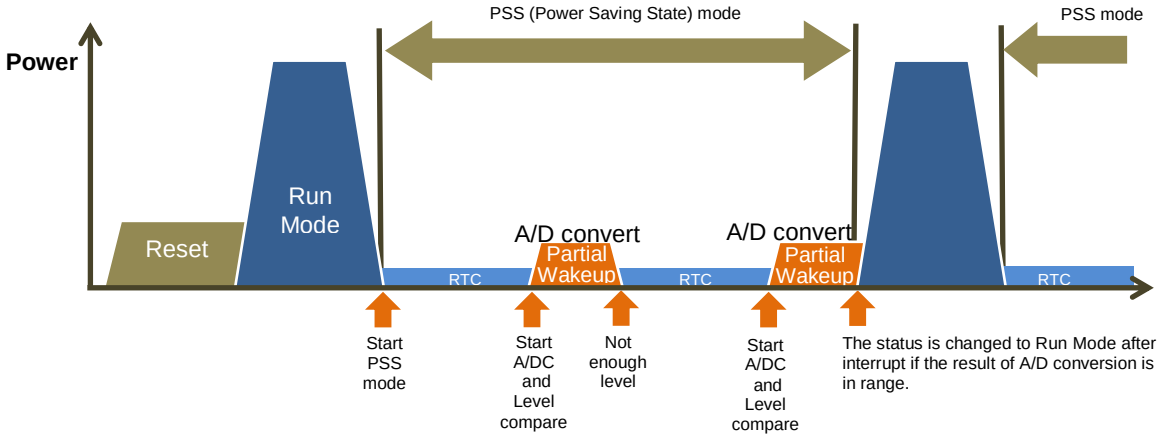
This application note is intended for users of the Cypress Traveo family MCUs. It describes how to Use Partial Wakeup. Refer to the datasheet for more details on features, packages, and memory size variations.

2 How Partial Wakeup Works

The Partial Wakeup (PWU) functionality uses the A/D converter, with a low current consumption mode of the microcontroller. The PWU mode is one of the Power Saving State (PSS) modes. In this mode, only the features required for voltage monitoring by the A/D converter are functional.

Effective use of PWU function enables monitoring of the voltage, such as in the output of a sensor, with low power consumption and without starting the CPU.

Figure 1. Partial Wakeup Timeline

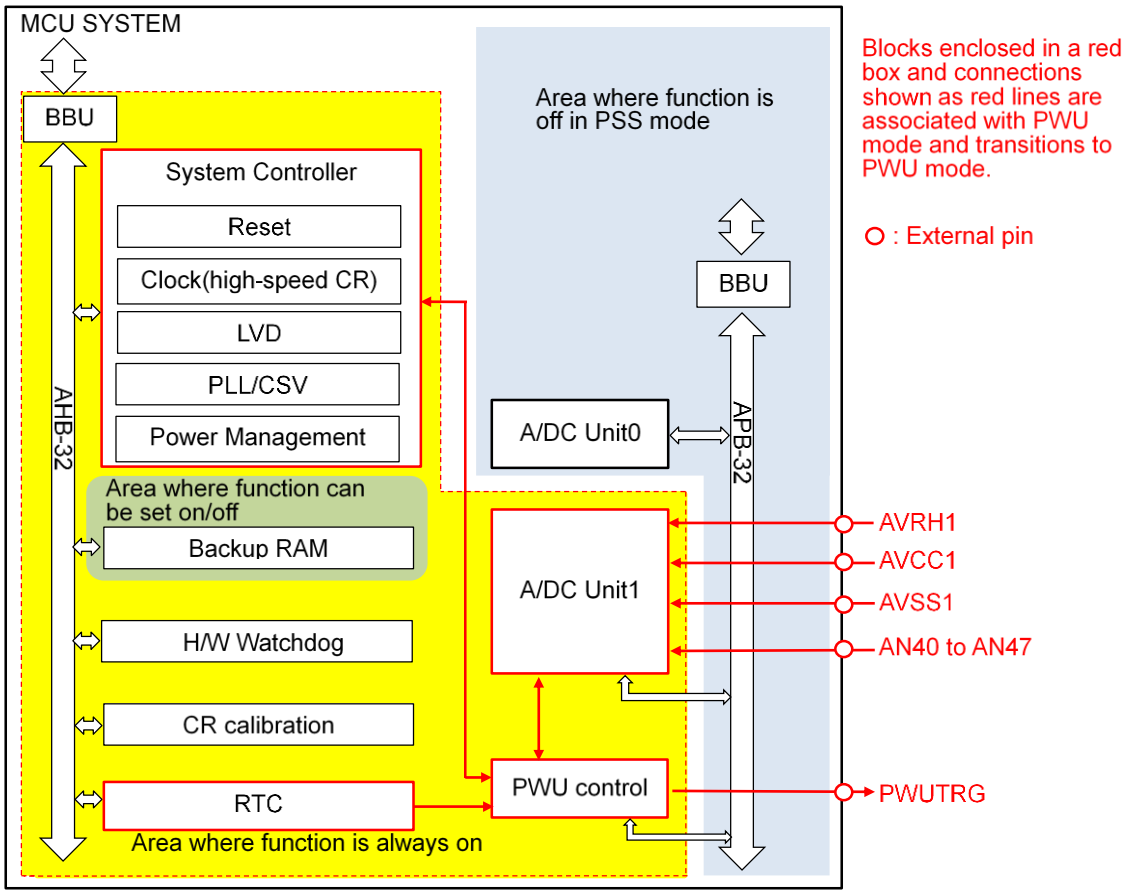


1. The CPU mode is changed to PSS mode from Run mode. MCU goes into Sleep mode (with RTC).
2. The MCU is periodically put in the PWU mode. The ADC is started and the voltage input from the AN terminal is observed automatically.
3. When the A/D value is not in the programmed range, the MCU continues in the PSS mode.
4. When the A/D value is in the programmed range, the CPU wakes up. The MCU is put into the RUN mode.

3 Configuration

The following diagram shows the partial wakeup configuration. Note that the diagram shows only the relationship with relevant blocks.

Figure 2. Relationship between the Entire System and the Partial Wakeup Function



3.1.1 RTC

The RTC block counts the cycles for transitioning to the PWU mode. The cycles can be set in steps of 7.8125 ms, between 7.8125 ms and 62.5 ms. The sample cycle value of 7.8125 ms is based on the following calculation:

Sample Cycle = 0.25 s (period of the RTC operation with a low-speed CR (100 kHz typical) in PWU mode)/32.

For more information about the 0.25-s value, see the "2-1" sequence in Table 2. RTC Calibration Setting, and the "Partial Wakeup Trigger Control Register (RTC_PWUTRGCR)" section of the “Real Time Clock" chapter in the Hardware Manual.

3.1.2 PWU Control

The PWU Control block controls the high-speed CR oscillator, the "PWUTRG" pin output function, and ADC Unit1. In the PWU mode, the block outputs "H" from the "PWUTRG" pin. The block starts the A/D conversion within a certain time after the PWUTRG pin outputs "H". The time until the A/D conversion starts can be set in steps of 50 µs, between 50 and 5100 µs.

3.1.3 System Controller

The System Controller block manages the device mode (PSS or RUN). The block turns on the high-speed CR oscillator when transitioning to the PWU mode.

3.1.4 A/DC Unit1

In PWU mode, when you use S6J3110 or S6J3400 series the A/D converter can be used only with the eight channels from AN40 to AN47.

In PWU mode, when you use S6J3360 or S6J3370 series, the A/D converter can be used only with the eight channels from AN6-8 and AN12-16.

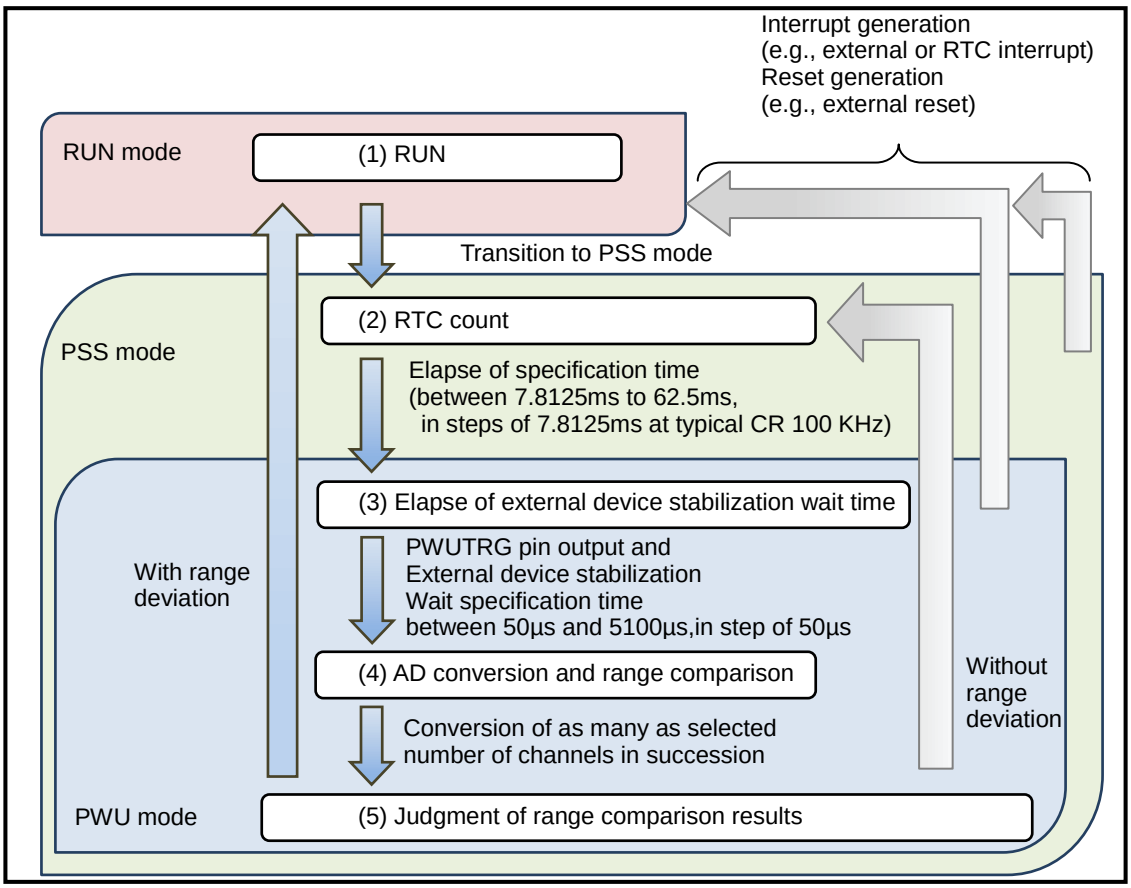
In PWU mode, only the range comparison function of the A/D converter can be used.

4 Explanation of Operation

4.1 Mode Transition Diagram

The following diagram shows the relationship between the partial wakeup mode and other modes. The figure outlines the operations. For a more detailed explanation of the operations, see the next section.

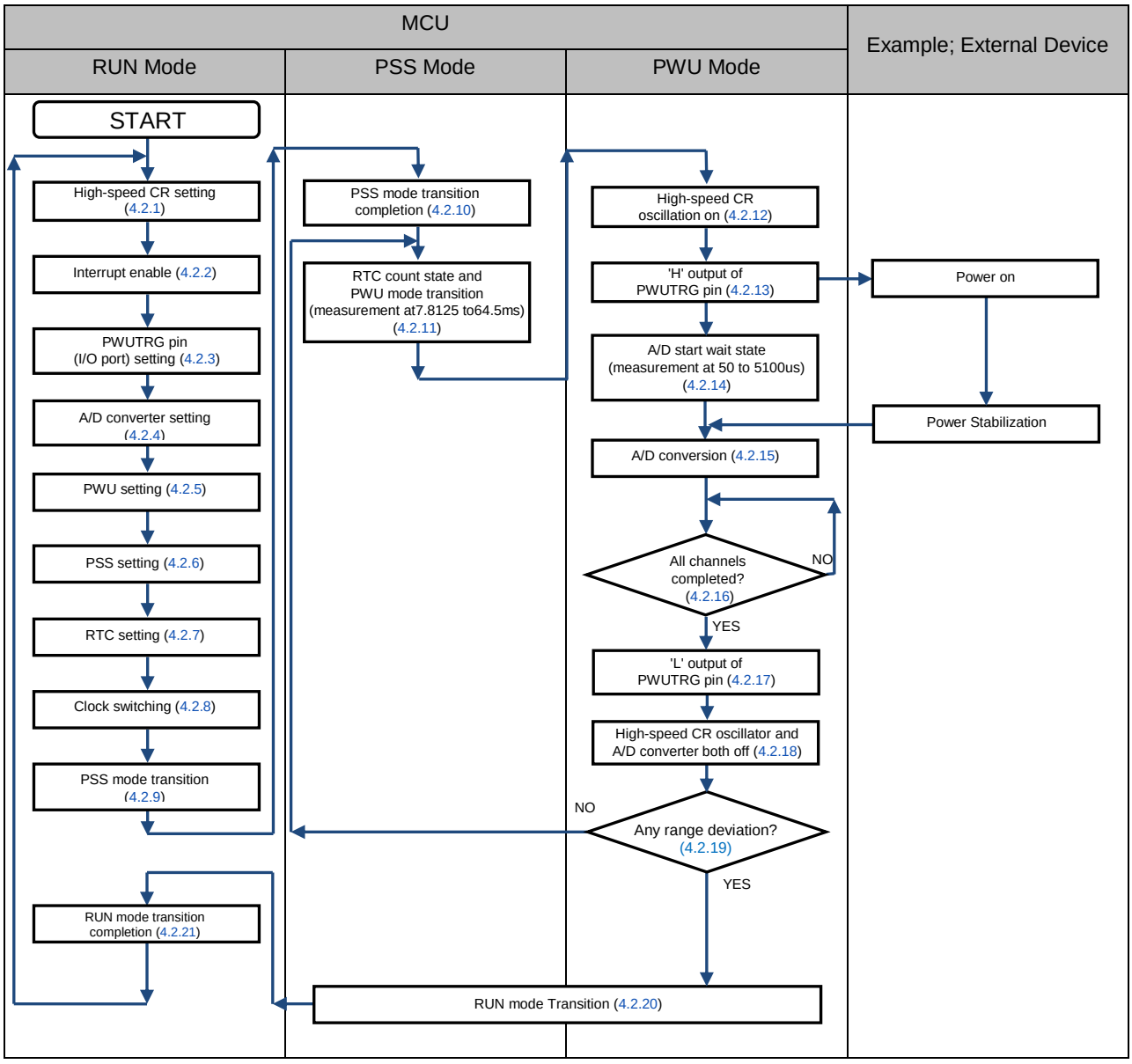
Figure 3. Partial Wakeup Mode Transition Diagram



4.2 Flowchart

The following flowchart explains the partial wakeup function in detail. Steps and states numbered in this flowchart are referenced in the corresponding description. The "RUN mode" is in a state that is executing the user program.

Figure 4. Partial Wakeup Function Flowchart



4.2.1 High-Speed CR Setting (Processing by Software)

4.2.1.1 Calibration

Software calibrates the high-speed CR oscillator and corrects any deviation in the A/D conversion time and the period from the PWUTRG pin output to A/D conversion start (external device stabilization wait time). Such deviations are due to process variations and variations depending on the use conditions.

For more information on these settings, see the “CR CALIBRATION" chapter in the Related Documents.

4.2.1.2 Stabilization Wait Time

Set the PSCL bit and CMPR bit in the SYSC_FCRCTCPR register to the initial (default) value.

These settings are applied to the settings described in the 4.2.12 High-Speed CR Oscillator ON (Processing by Hardware) section. If the stabilization wait time is set to a large value and the PWU mode time exceeds the PWU transition cycle, the device enters an illegal state. In this state, the transition to RUN mode cannot occur by an A/D converter range deviation.

For details on setting the stabilization wait time, see the “SOURCE CLOCK TIMER" chapter in the Related Documents.

4.2.2 Interrupt Enable (Processing by Software)

You can treat enabled interrupt factors as return factors from the PSS mode and PWU mode. If the MCU returns to the RUN mode due to an interrupt, a transition occurs as described in the 4.2.20 RUN Mode Transition (Processing by Hardware) section.

You can specify the following parameters: interrupt of a resource not in the Power Down state, even in PSS mode. Examples include external interrupt, RTC, NMI, and low-voltage detection. For information on the method of enabling interrupts, see the chapters on the respective resources in the Hardware Manual.

For information on ADC-related settings, see the 4.2.4 A/D Converter Setting (Processing by Software) section.

4.2.3 PWUTRG Pin (I/O port) Setting (Processing by Software)

Here, software makes the port output setting for the output of the PWUTRG function and the analog I/O settings of the A/DC.

You can set the PWUTRG by writing an appropriate value to the Port Output Function (POF) bit in the corresponding PPC_PCFGRijj (i=0 to 4, jj=00 to 31) register.

The target port is used as analog input of A/DC by writing appropriate value to the corresponding PPC_PCFGRijj (i=0 to 4, jj=00 to 31) register and GPIO_DDR register.

For a corresponding register and setting,

If you use S6J3310 or S6J3400 series, see the "APPENDIX: VARIOUS SETTINGS OF I/O PORTS" section in the Hardware Manual.

If you use S6J3360 or S6J3370 series, see the chapter of "Port Configuration" section in the Hardware Manual.

For information on the settings related to retaining the pin state in PSS mode, see the 4.2.6 PSS Setting (Processing by Software) section.

4.2.4 A/D Converter Setting (Processing by Software)

Table1-1 (for S6J3110 & S6J3400 series) and Table 1-2(for S6J3360 & S6J3370 series) lists the setting values for the writeable registers related to A/D converter unit 1 corresponding to PWU mode.

The following numbered limitations correspond to the entry in column 3 of Table 1-1 and Table 1-2:

1. Set a value appropriate to the use conditions.
2. The recommended setting is based on the "setting value." It can be changed to match the use conditions.
3. Always set values according to the "setting value."

For a detailed explanation of the registers and the setting method, see the “12-BIT A/DCONVERTER" chapter in the Hardware Manual.

Note:
When you use PWU mode with S6J3110 or S6J3400 series, you can use up to eight activation channels [AN40 to AN47].

When you use PWU mode with S6J3360 or S6J3370 series the A/D converter can be used only with the eight channels from AN6-8 and AN12-16.

Table 1-1. A/D Converter Settings (for S6J3110 or S6J3400 Series)

Register Name	Setting Value	Limitation
KEYCDR	Before writing to the ADER1 register, write to this register by using the prescribed method and then release write protection.	3
ADER1	Set the bit corresponding to the pin used for the analog input to '1', and set the other pins to '0'. Except for AN40 to AN47, rest of the analog inputs are not supported, so set the ADEn (n=32 to 39, 48 to 63) bits to "0".	3
ADTSS1	Do not write.	3
ADTSE1	Set all bits to '0'. (Software start is prohibited.)	3
ADCOMPB32 to ADCOMPB63	There is no effect on operation.	1
ADTCS32 to ADTCS63 * Select only the registers corresponding to the numbers assigned as activation channels.	INTE=1'b0	3
	{STS1,STS0}=2'b10	3
	RPT=1'b1	3
	PRT=1'b0	3
	PRTS = Do not use with the PWU mode. (There is no effect on operation.)	1
	{SEL1, SEL0} = Do not use with the PWU mode. (There is no effect on operation.)	1
	BUFX = Do not use with the PWU mode. (There is no effect on operation.)	1
	BTS = Do not use with the PWU mode. (There is no effect on operation.)	1
ADTECS32 to ADTECS63 * Select only the registers corresponding to the numbers assigned as activation channels.	STS2=1'b0	3
	Value of {CHSEL4, CHSEL3, CHSEL2, CHSEL1, CHSEL0}= 5'b01000 to5'b01111 Activation channels and analog input pins are associated. Since only analog input pins AN40 to AN47 are associated, the settings must be associated with these pins.	3
ADRCUT4 to ADRCUT7	Set a value appropriate to the use conditions.	1
ADRCLT4 to ADRCLT7	Set a value appropriate to the use conditions.	1
ADRCCS32 to ADRCCS63* Select only the registers corresponding to the numbers assigned as activation channels.	{RCOCD2, RCOCD1, RCOCD0}=3'b001	3
	RCOIRS = Set a value appropriate to the use conditions.	1
	RCOIE=1'b1	3
	RCOE=1'b1	3
	{RCOTS1, RCOTS0} = Set a value appropriate to use conditions.	1
ADSCANS1	SCIE=1'b1	3
	SCMD=1'b1	3

Register Name	Setting Value	Limitation
ADNCS16 to ADNCS31* Select only the registers corresponding to the numbers assigned as activation channels.	CNTEN=1'b1	3
	{CCNT1, CCNT0}=2'b00	3
ADTCSC32 to ADTCSC63 * Select only the registers corresponding to the numbers assigned as activation channels.	Do not use with the PWU mode.	1
ADRCIFC1	Write '1' to clear the range comparison interrupt flag corresponding to the number assigned as the activation channel. (Do not transition to the PWU mode with interrupts left enabled)	3
ADSCANSC1	Write '1' to clear the scan conversion completion interrupt flag. (Do not transition to the PWU mode with interrupts left enabled)	3
ADMD1	STPCEN=1'b0	2
	{CT1, CT0}=2'b00 (Setting 2'b11 is prohibited.) The built-in high-speed CR oscillator clock (4 MHz) is divided according to the setting, and the compare time is measured using the divided clock. For details and notes on the settings, see the 12-BIT A/D CONVERTER" chapter in the Hardware Manual.	2
	{ST1, ST0}=2'b00 (Setting 2'b11 is prohibited.) The built-in high-speed CR oscillator clock (4 MHz) is divided according to the setting, and the sampling time is measured using the divided clock. For details and notes on the settings, see the "12-BIT A/D CONVERTER" chapter in the Hardware Manual.	2
ADSTPCS8 to ADSTPCS15 * Select only the registers corresponding to the numbers assigned as activation channels.	{STCH1, STCH0}=2'b00 (Setting 2'b11 is prohibited.) The built-in high-speed CR oscillator clock (4 MHz) is divided according to the setting, and the sampling time is measured using the divided clock. For details and notes on the settings, see the "12-BIT A/D CONVERTER" chapter in the Hardware Manual.	2

Table 1-2. A/D Converter Settings (for S6J3360 or S6J3370 Series)

Register Name	Setting Value	Limitation
ADC12B1_CHCTRLi (i = 0~63)	TRGCL=1'b0	3
	SWTRG=1'b0	3
	Value of RCEN is set to the following value. RCEN bits corresponding to activation channels are set to 1'b1 (Range comparator enabled), and other bits are set to 1'b0 (Range comparator disabled).	3
	RCINVSEL=Set a value appropriate to use conditions.	1
	RCSEL[2:0]=Set a value appropriate to use conditions. Set the register value "i" (i.e. ADC12B1_FRCOHi, ADC12B1_FRCOLi) selected as the upper/lower threshold values.	1
	SMTIME[1:0]=Set a value appropriate to use conditions. Set the register value "i" (i.e. ADC12B1_STi) selected as channel sampling time.	2
	DP=1'b0	3
	RSMRST[1:0]=2'b00	1
	Value of CHPRI[3:0] are set to three kinds of priority. CHPRI[3:0]=4'b0000 (Highest priority) Set the first channel (e.g. corresponding to AN6) of the group to the above value. CHPRI[3:0]=4'b0001 Set the following channels (e.g. corresponding to AN7 - AN8,AN12-AN16) to the above value. CHPRI[3:0]=4'b0010 or more Set the unnecessary channels for PWU mode to the above value. For details and notes on the settings, see the chapter “12/10/8-Bit Analog To Digital Converter" in S6J3360 or S6J3370 series manual.	3
	Value of TRGTYP[1:0] are set to two kinds of trigger types. TRGTYP[1:0]=2'b01 (Software or hardware trigger.) Set the first channel (e.g., corresponding to AN6) of the group to the above trigger type. TRGTYP[1:0]=2'b10 (Preceding logical channel conversion completion.) Set the following channels (e.g., corresponding to AN7 - AN8, AN12-AN16) to the above trigger type. No other channel (corresponding to use in PWU mode) must be included in the group which is defined for PWU mode. It is prohibited to set TRGTYP[1:0]=2’b11 (Idle trigger) in PWU mode. For details and notes on the settings, see the chapter “12/10/8-Bit Analog To Digital Converter" in S6J3360 or S6J3370 series manual.	3
	Value of ANIN[5:0]=6'b000110 to 6'b001000 or 6’b001100 to 6’b010000 Activation channels and analog input pins are associated. Only analog input pins AN6 to AN8 or AN12 to AN16 are enabled with PWU mode.	3
ADC12B1_PCCTRL i (i = 0~63)	Do not use with the PWU function.	1

Register Name	Setting Value	Limitation
ADC12B1_CDONEIRQE0/1	Value of {CDONEIRQE63 to CDONEIRQE0} is set to the following value. Interrupt enable bit (CDONEIRQEx) of the last channel in the group is set to 1'b1 (Conversion done interrupt enabled), and other bits are set to 1'b0 (Conversion done interrupt are disabled). (Do not transition to PWU mode with interrupts left enabled.) The channel set at this register will be the last channel of the group procedure.	3
ADC12B1_CDONEIRQC0/1	Write "0xFFFF_FFFF" to clear all A/D conversion done interrupt flags.	3
ADC12B1_GRPIRQE0/1	Value of {GRPIRQE63 to GRPIRQE0}="0x0000_0000_0000_0000" (Group interrupted interrupt disabled.)	3
ADC12B1_GRPIRQC0/1	These bits are not used in PWU mode.	1
ADC12B1_RCIRQE0/1	The value of {RCIRQE63 to RCIRQE0} is set to the following value. Interrupt enable bit (RCIRQEx) of the activation channel for PWU mode is set to 1'b1 (Range comparator interrupt enabled), and other bits are set to 1'b0 (Range comparator interrupt are disabled). (Do not transition to PWU mode with interrupts left enabled.)	3
ADC12B1_RCIRQC0/1	Write "0xFFFF_FFFF" to clear all Range comparator interrupt flags.	3
ADC12B1_PCIRQE0/1	Value of {PCIRQE63 to PCIRQE0}="0x0000_0000_0000_0000" (Pulse counter interrupt is disabled.)	3
ADC12B1_PCIRQC0/1	These bits are not used in PWU mode.	1
ADC12B1_TRGCL0/1	Write "0xFFFF_FFFF" to clear all A/D channel trigger status flags	3
ADC12B1_TRGORC0/1	Write "0xFFFF_FFFF" to clear all A/D channel trigger overrun flags	3
ADC12B1_CDDS0~3	CDCHEN=1'b0 (DMA request is disabled.) CDCHNUM[5:0] have no effect with CHCHEN=1'b0.	3
ADC12B1_RT	These bits are not used in PWU mode, when Power down disable mode (ADC12Bn_CTRL.PDDMD = "1"), these bits have no effect.	1
ADC12B1_CT	CT[15:0]="0x0001" ("0x0006" or more is a prohibited setting.) The built-in high-speed CR oscillation clock (4 MHz) is divided according to the setting, and the comparison time is measured using the divided clock. For details and notes on the settings, see the chapter of “12/10/8-Bit Analog To Digital Converter" on S6J3360 or S6J3370 series manual.	2
ADC12B1_STi (i = 0~3) * Select only the registers corresponding to the numbers assigned as the settings for the sampling time	STi[15:0]="0x0007" ("0x0019" or more is a prohibited setting.) The built-in high-speed CR oscillation clock (4 MHz) is divided according to the setting, and the sampling time is measured using the divided clock. For details and notes on the settings, see the chapter “12/10/8-Bit analog To Digital Converter" in S6J3360 or S6J3370 series manual.	2
ADC12B1_OCV	This register specifies the setting for offset compensation value.	2
ADC12B1_GCV	This register specifies the setting for gain compensation value.	2
ADC12B1_CTRL	RES[1:0]=2'b00 (12 bit resolution)	3
	DBGE=1'b0	3
	ACHMD=1'b0	3
	FSMD=1'b0	3
	FRCMD=1'b1 (12 bit range comparator mode)	3
	FSTP=1'b0 (When the "not" forced stop mode (FSMD = "0")	1
	PDDMD=1'b1 (A/D convertor does not go idle state after A/D conversion finished.)	3
ADC12B1_RCOL0~7	Do not use with the PWU function.	1

Register Name	Setting Value	Limitation
ADC12B1_RCOH0~7	Do not use with the PWU function.	1
ADC12B1_FRCOH0~7 * Select only the registers corresponding to the numbers assigned as the upper threshold values	FRCOH[11:0]=Set a value appropriate the use conditions.	1
ADC12B1_FRCOL0~7 * Select only the registers corresponding to the numbers assigned as the lower threshold values	FRCOL[11:0]=Set a value appropriate the use conditions.	1
ADC12B1_MCCTRL0~3	Value of ADC12B1_MCTRL="0x00"	3

4.2.5 PWU Setting (Processing by Software)

1. Enables the PWU function.
2. Sets the external device stabilization wait time, which is the period between the PWUTRG pin output and A/D conversion start.

You can select external circuit or device stabilization wait times from 50 µs to 5100 µs in steps of 50 µs when the high-speed CR oscillator is typically 4 MHz.

If using S6J3360 or S6J3370 series, you can set as follows:

1. Select the PWU A/D conversion trigger (PWU_ADT) as A/D conversion trigger.
2. Set the first logical channel number of the group procedure executing in the PWU mode.

4.2.6 PSS Setting (Processing by Software)

Table 2-1(for S6J3110 or S6J3400 series) and Table 2-2(for S6J3360 or S6J3370 series) lists the setting values for the writeable registers in the PSS profile register group and the writeable registers of the system special setting registers.

The following numbered limitations correspond to the entry column 3 of Table 2-1 and Table 2-2:

1. Set a value appropriate to the use conditions.
2. The recommended setting is based on the "setting value." It can be changed to match the use conditions.
3. Always set values according to the "setting value."

For a detailed explanation of the registers and the setting method, see the "LOW-POWER CONSUMPTION" chapter in the Hardware Manual.

Table 2-1. PSS Profile Register Group Settings (for S6J3110 or S6J3400 series)

Register Name	Setting Value	Limitation
SYSC0_PSSPDCFGR	PD6_0EN=1'b0	3
	PD4_1EN = Set a value appropriate to the Backup RAM use conditions.	1
	PD4_0EN = Set a value appropriate to the Backup RAM use conditions.	1
	PD2EN=1'b0	3

Register Name	Setting Value	Limitation
SYSC0_PSSCKSRER	SSCG0EN=1'b0	3
	PLL0EN=1'b0	3
	MOSCEN=1'b0	3
	SCROSCEN=1'b1	3
	CROSCEN=1'b0	3
SYSC0_PSSCKSELR	CDMCUCCSL=3'b111	3
SYSC0_PSSCKER	ENCLKMCUCP=1'b0	3
	ENCLKMCUCH=1'b0	3
SYSC0_PSSCKDIVR	MCUCPDIV=4'b0000	3
	MCUCHDIV=5'b00000	3
SYSC0_PSSPLLxCNTR	PLLxISEL=1'b0	2
	PLLxDIVN=8'b00001101	2
	PLLxDIVM=4'b0001	2
	PLLxDIVL=2'b00	2
SYSC0_PSSSSCGxCNTR0	SSCGxISEL=1'b0	2
	SSCGxDIVN=8'b00001101	2
	SSCGxDIVM=4'b0001	2
	SSCGxDIVL=2'b00	2
SYSC0_PSSSSCGxCNTR1	SSCGxSSEN=1'b0	2
	SSCGxFREQ=2'b00	2
	SSCGxMODE=1'b0	2
	SSCGxRATE=10'b0000101001	2
SYSC0_PSSLVDCFGR	LVDL1S = Set a value appropriate to the use conditions.	1
	LVDL1V = Set a value appropriate to the use conditions.	1
	LVDL1E = Set a value appropriate to the use conditions.	1
	LVDH1S = Set a value appropriate to the use conditions.	1
	LVDH1V = Set a value appropriate to the use conditions.	1
	LVDH1E = Set a value appropriate to the use conditions.	1
SYSC0_PSSCSVCFGR	SSCG0CSVE=1'b0	3
	PLL0CSVE=1'b0	3
	MOCSVE=1'b0	3
SYSC0_PSSREGCFGR	RMSEL=1'b1	3

Register Name	Setting Value	Limitation
SYSC0_SPECFGR	HOLDIO_PD6_0=1'b0	3
	HOLDIO_PD2=1'b1 The setting by this bit is reflected immediately after writing the register, not after the PSS profile change.	3
	PSSPADCTRL=1'b0	3
	BRAMSC=1'b1 If the setting is PD4_0EN=1 or PD4_1EN=1, exercise Backup RAM sleep control to suppress current dissipation in the PSS mode.	3
SYSC1_PSSCKSELR0	LAPP1ACSL=1'b0	3
	LAPP0ACSL=1'b0	3
	LCP1ACSL=1'b0	3
	LCP0ACSL=1'b0	3
	CD0CSL=3'b111 If this setting is not made, a PSS profile error occurs at a PSS mode transition.	3

Table 2-2. PSS Profile Register Group Settings (for S6J3360 or S6J3370 series)

Register Name	Setting Value	Limitation
SYSC0_PSSPDCFGR	PD4_1EN = Set a value appropriate to the Backup RAM use conditions.	1
	PD4_0EN = Set a value appropriate to the Backup RAM use conditions.	1
	PD2EN=1'b0	3
SYSC0_PSSCKSRER	SSCG0EN=1'b0	3
	PLL0EN=1'b0	3
	MOSCEN=1'b0	3
	SCROSCEN=1'b1	3
	CROSCEN=1'b0	3
	SOSCEN=1'b0	3
SYSC0_PSSCKSELR	CDMCUCCSL=3'b111	3
SYSC0_PSSCKER	ENCLKMCUCP=1'b0	3
	ENCLKMCUCH=1'b0	3
SYSC0_PSSCKDIVR	MCUCHDIV=5'b00000	3
SYSC0_PSSPLLxCNTR	PLLxISEL=1'b0	2
	PLLxDIVN=8'b00001101	2
	PLLxDIVM=4'b0001	2
	PLLxDIVL=2'b00	2
SYSC0_PSSSSCGxCNTR0	SSCGxISEL=1'b0	2
	SSCGxDIVN=8'b00001101	2
	SSCGxDIVM=4'b0001	2
	SSCGxDIVL=2'b00	2

Register Name	Setting Value	Limitation
SYSC0_PSSSSCGxCNTR1	SSCGxSSEN=1'b0	2
	SSCGxFREQ=2'b00	2
	SSCGxMODE=1'b0	2
	SSCGxRATE=10'b0000101001	2
SYSC0_PSSLVDCFGR	LVDL1S = Set a value appropriate to the use conditions.	1
	LVDL1V = Set a value appropriate to the use conditions.	1
	LVDL1E = Set a value appropriate to the use conditions.	1
	LVDH1S = Set a value appropriate to the use conditions.	1
	LVDH1V = Set a value appropriate to the use conditions.	1
	LVDH1E = Set a value appropriate to the use conditions.	1
SYSC0_PSSCSVCFGR	SSCG0CSVE=1'b0	3
	PLL0CSVE=1'b0	3
	SCRCSVE=1’b0	3
	CRCSVE=1’b0	3
	SOCSVE=1’b0	3
	MOCSVE=1'b0	3
SYSC0_PSSREGCFGR	RMSEL=1'b1	3
SYSC0_SPECFGR	HOLDIO_PD2=1'b1 The setting by this bit is reflected immediately after writing register, it is not after PSS profile change.	3
	PSSPADCTRL=1'b0	3
	EXVRSTCNT=1'b1 If the setting is EXVRSTRCNT=1’b0, the RAM data of Backup area in System SRAM are not guaranteed after LVDH1 reset.	3
SYSC1_PSSCKSELR0	LAPP1ACSL=1’b0	3
	LAPP0ACSL=1’b0	3
	LCP1ACSL=1’b0	3
	LCP0ACSL=1’b0	3
	CD0CSL=3’b111 If this setting is not made, a PSS profile error occurs at a PSS mode transition.	3

4.2.7 RTC Setting (Processing by Software)

Table 1 through Table 5 show examples of RTC settings. For details on the setting method, see the "REAL-TIME CLOCK" chapter in the Hardware Manual.

Initialization Settings

Table 1. RTC Initialization Settings

Sequence	Set Contents *1	Set Timing
1-1	Write ‘1’ to the ST bit in the RTC_WTCR register.	Setting needs to be done only after the POR.
1-2	Write ‘0’ to the ST bit in the RTC_WTCR register.	Setting needs to be done only after the POR.
1-3.	Write ‘"2'b10’ to the RCKSEL bit in the RTC_WTCR register, write ‘1’ to the CSM bit, and select the low-speed CR clock.	Setting needs to be done only after the POR. (RTC Clock = typical 100 kHz)
1-4.	Set each bit in the RTC_WRT register.	Setting needs to be done only after the POR

*1 Do not write to the registers at the bit level.

There is a possibility that the bit that the hardware automatically changes will be rewritten unintentionally by the program (e.g.; "UPCAL" bit in RTC_WTCR register). In this case, the bit with a difference function between read and write is changed to the other setting. Therefore, unrelated bits might get affected.

Calibration setting to correct deviations in count values due to variations in low-speed oscillator

Table 2. RTC Calibration Setting

Sequence	Set Contents *1	Set Timing
2-1.	Write a value to the DURMW bit in the RTC_DURMW register, and set the calibration period. Normally, set the calibration period to 0.25 s. To set a time 0.25 s or shorter, a value of 0.25 s divided by 1, 2, 4, 8, or 16 can be selected for the period. However, the lower the value set, the lower the accuracy becomes. (Related to the SCAL[2:0] bit) When the main clock is 4 MHz and the calibration period is set to 0.25 s, set the DURMW bit value="0xF4240" (1'000'000 as a decimal).	First setting only after POR
2-2.	Set the following related bits in the RTC_WTCR register.	
	Set the SCAL [2:0] bit according to the RTC_DURMW value. If the calibration period is set to 0.25 s, set ‘'3'b000’.	First setting only after POR
	Set the CCKSEL bit to ‘1'b1’, and select the low-speed CR oscillator.	First setting only after POR (RTC Clock = typical 100 kHz)
	Set the ENUP bit according to the use conditions. To update the calibration result automatically with hardware, set ‘1'b1’. To update it with software, set ‘1'b0’.	First setting only after POR
	Set the ACAL bit to ‘1'b0’, and disable auto calibration.	First setting only after POR
2-3.	Write ‘1'b1’ to the CALDC bit in the RTC_WINC register, and clear the calibration interrupt.	Clear the interrupt flag after an interrupt occurs.
2-4.	Write ‘1'b1’ to the MTRG bit in the RTC_WTCR register, and start calibration.	Set in the timing that you want to calibrate.(e.g. Post-PWU) The calibration is available on real time count.
2-5.	Wait until the CALD bit in the RTC_WINS register becomes ‘1'b1’.	

*1 Do not write to the registers at the bit level..

Partial Wakeup Setting

Case 1: When the ENUP bit in the '2-2' entry in Table 4 is set to ‘1'b1’"

Table 3. RTC Initialization – Case 1

Sequence	Set Contents *1	Set Timing
3-1.	Set the following related bits in the RTC_PWUTRGCR register.	
	Set the MD bit to ‘1'b1’.	First setting only after POR
	For the SEL bit, set the cycles for transitioning to the PWU mode in accordance with the purpose. Values ranging from 7.8125 ms to 62.5 ms can be selected in units of 7.8125 ms. (When Low-speed CR oscillator is typically 100 kHz)	The period of PWU can be switched.
3-2.	Wait until the BUSY bit in the RTC_PWUTRGSR register becomes ‘1'b0’.	Set if RTC_PWUTRGCR register is changed.

*1 Do not write to the registers at the bit level.

Case 2: When the ENUP bit in the '2-2' entry in Table 4 is set to ’1'b0’.

Table 4. RTC Initialization – Case 2

Sequence	Set Contents *1	Set Timing
3-1.	Read the value of RTC_CNTCAL, subtract 1, and then divide it by 32. The RTC_CNTCAL includes the counter value of 0.25 s. By dividing by 32, it generates a count value of approximately 8 ms.	Set if the calibration (setting of “2-3”-”2-5”) sequences in Table 2 is completed.
3-2.	Read the value of RTC_CNTCAL, and subtract 1. Write the post processing value to the WTBR bit in the RTC_WTBR register.	
3-3.	Set the related bits in the RTC_PWUTRGCR register as described below.	
	- Set the C8MRL bit to the value calculated in "3-1" in this table.	Set if the calibration (the setting of “2-3”-”2-5”) is completed.
	- Set the MD bit to ‘1'b0’.	1st setting only after POR
	- For the SEL bit, set the cycles for transitioning to the PWU mode in accordance with the purpose. Values ranging from 8 to 64 ms can be selected in units of 8 ms.	The period of PWU can be switched.
3-4.	Wait until the BUSY bit in the RTC_PWUTRGSR register becomes ‘1'b0’.	Set if RTC_PWUTRGCR register is changed.

*1 Do not write to the registers at the bit level. .

RTC Count Start

Table 5. RTC Initialization – RTC Start

Sequence	Set Contents *1	Set Timing
4-1.	Set the RTC_WINE register, and enable the required interrupts.	First setting only after POR
4-2.	Write a ‘1’ to each bit in the RTC_WINC register, and clear the interrupt flag.	Clear the interrupt flags after interrupts occur
4-3.	Write a ‘1’ to the ST bit in the RTC_WTCR register, and start counting.	First setting only after POR (RTC Clock = 100 kHz)

*1 Do not write to the registers at the bit level.

4.2.8 Clock Switching (Processing by Software)

1. Clock Gear Down Operation

If the PLL clock is being used for operating the internal circuit, use the clock gear down function to set the clock frequency lower in stages to reduce the fluctuations due to clock switching.

For details on how to use the clock gear down function, see the "Clock Gear" section in the “CLOCK SYSTEM" chapter in the Hardware Manual.

2. Clock Adjustment

To transition to PSS, establish a 1:1 relationship among the CPU clocks, memory configuration clock, SCU clock, and MCUCH clock. The absence of this relationship among these clocks may cause a malfunction. Additionally, PLL and SSCG-PLL must be disabled before PSS mode transition.

Example of Settings

Because the SCU clock operates with the high-speed CR oscillator clock, switch the CPU clock (CLK_CPU), memory configuration clock (CLK_MEMC), and MCUCH clock (CLK_SYSC0H) so that they all operate with the high-speed CR oscillator clock.

a. Set the CD0CSL bit in the SYSC1_RUNCKSELR0 register to zero.
b. Set the HPMDIV bit and the SYSDIV bit in the SYSC1_RUNCKDIVR0 register to zero.
c. Set the CDMCUCCSL bit in the SYSC0_RUNCKSELR register to zero.
d. Set the MCUCHDIV bit in the SYSC0_RUNCKDIVR register to zero.
e. Set the PLL0EN and SSCG0EN bit in the SYSC0_RUNCKSRER register to zero. (PLL and SSCG-PLL are disabled.)
f. Set the SYSC0_RUNPLL0CNTR, SYSC0_RUNSSCG0CNTR0 and SYSC0_RUNSSCG0CNTR1 register to the appropriate value to avoid a profile error.

   For details on the combination of violation settings, see "Profile" in the "LOW-POWER CONSUMPTION" chapter in the Hardware Manual.
g. Set the SYSC1_RUNENR register to ‘0xAB’.
h. Set the SYSC0_TRGRUNCNTR register to ‘0xAB’. (The RUN profile update starts.)
i. Wait until the RUNDF0 bit in the SYSC0_SYSSTSR register becomes ‘1’

4.2.9 PSS Mode Transition (Processing by Software)

See "Operation Procedure" in the “LOW-POWER CONSUMPTION" chapter in the hardware manual and transition to PSS mode.

4.2.10 PSS Mode Transition Completion (Processing by Hardware)

There has been a transition to PSS mode according to the PSS profile register settings as described in Section 4.2.6 PSS Setting (Processing by Software).

4.2.11 RTC Count State and PWU Mode Transition (Processing by Hardware)

Hardware waits until the RTC count value reaches the cycles set in the step described in Section 4.2.7 RTC Setting (Processing by Software). After the cycles are reached, the MCU transitions to the PWU mode. For a transition from RUN mode to PSS mode, the RTC is not initialized because PWU mode is executed at the same periodic interval.

4.2.12 High-Speed CR Oscillator ON (Processing by Hardware)

Hardware turns on the high-speed CR oscillator. A stabilization wait time is activated to turn on the high-speed CR oscillator. This wait time is set by the steps described in Section 4.2.1 High-Speed CR Setting (Processing by Software). The PWU mode operates with the output clock of the high-speed CR oscillator.

4.2.13 "H" Output of the PWUTRG Pin (Processing by Hardware)

Hardware changes PWUTRG from ‘L’ to ‘H’.

4.2.14 A/D Start Wait State (Processing by Hardware)

Hardware waits until it arrives at the time (Until the external circuit is stabilized) set by the steps described in Section 4.2.5 PWU Setting (Processing by Software). The power supply of external devices is assumed to be stable during this wait period.

When using S6J3110 or S6J3400 series, A/D conversion starts after the set time has elapsed.

When using S6J3360 or S6J3370 series, A/D conversion request (PWU_ADT)is issued and A/D conversion is started.

4.2.15 A/D Conversion (Processing by Hardware)

A/D conversion is executed according to the settings described in Section 4.2.4 A/D Converter Setting (Processing by Software).

4.2.16 A/D Conversion Judgment (Processing by Hardware)

Hardware waits until the conversion of all selected channels (up to eight channels) completes.

4.2.17 'L' Output of the PWUTRG Pin (Processing by Hardware)

Hardware switches the PWUTRG output from 'H' to 'L'.

4.2.18 High-Speed CR Oscillator and A/D Converter Both Off (Processing by Hardware)

Hardware turns off the high-speed CR oscillator and A/D converter.

4.2.19 Range Comparison Judgment (Processing by Hardware)

Hardware determines whether a range deviation has arisen as a result of the A/D conversion at the step described in Section 4.2.15 A/D Conversion (Processing by Hardware). If no deviation has arisen, the MCU transits to the PSS mode again. If a deviation has arisen, a WAKEUP signal is issued, followed by a transition to RUN mode to wake up the CPU.

4.2.20 RUN Mode Transition (Processing by Hardware)

For details on the operation, see "Operation Procedure" in the "LOW-POWER CONSUMPTION" chapter in the Platform Hardware Manual.

4.2.21 RUN Mode Transition Completion (Processing by Hardware)

1. PSS enable setting: Set the PSSEN0 bit in the SYSC0_PSSENR register to '1'b0'. Otherwise, written data to registers in SYSC0 is invalid and a bus error will occur. However, setting the PSSEN1 bit in the SYSC1_PSSENR register is not required because of initialization with power down.
2. Determination of the wakeup factor: If the following bits are all '0' before the step described in 4.2.9 PSS Mode Transition (Processing by Software) and '1' after the RUN mode transition, you are able to determine whether the RUN mode transition occurred by A/DC range deviation.

   When you using S6J3110 or S6J3400 series:

   a. Any bits among RCINT32 to RCINT63 in ADRCIF1 register
   b. SCINT bit in ADSCANS1 register

   When you using S6J3360 or S6J3370 series:

   a. RCIRQ0 to RCIRQ63 in ADC12B1_RCIRQ0/1 register
   b. CDONEIRQ0 to CDONEIRQ63 in ADC12B1_CDONEIRQ0/1 register

   Moreover, if you have made the settings described in Section 4.2.2 Interrupt Enable (Processing by Software), a RUN mode transition might occur by the factor you set. You need to check the interrupt flag.

3. A/D Converter use after RUN mode transition:

   a. When using S6J3110 or S6J3400 series:

   When the A/D conversion is executed in the PWU mode, the A/D Converter enters the "Pause state". *1

   If the ADC enters the Pause state, the BUSY flag is activated. It is not possible to change the ADC setting when the BUSY flag is activated. For example, when the CNTEN bit in registers from ADNCS16 to ADNCS31 is changed, A/D Conversion starts unexpectedly. When you change A/D Converter setting after the run mode transition, clear the BUSY flag before changing the setting.

Example of settings

Write ‘1’ to the BUSYC bit in registers from ADTCSC32 to ADTCSC63.

*1. See the explanation of “Pause scan conversion when the conversion count is specified for each channel” in “5.2.12. About the Scan Conversion Mode” in the “12-BIT A/D CONVERTER” chapter in the Hardware Manual.

b. When using S6J3360 or S6J3370 series:

The corresponding A/D Channel Trigger Status flag (ADC12B1_TRGST0/1.TRGST and ADC12B1_CHSTAT0～63.TRGST) is set if A/D conversion request (PWU_ADT) occurs in PWU mode.

Updating the A/D converter setting during A/D conversion operation (ADC12B1_TRGST0/1.TRGST and ADC12B1_CHSTAT0～63.TRGST=”1”) is not allowed. After run mode transition, clear all trigger status flags in case of changing A/D converter setting.

Example of settings

Write "1" to TRGCL0 to TRGCL63 bits in ADC12B1_TRGCL0/1 register.

For a detailed explanation of the A/D Channel Trigger Status flags, see the chapter "12/10/8-Bit Analog To Digital Converter” in the Hardware manual..

When using hardware trigger as the active trigger for A/D Converter Unit1 in RUN mode, write “0” to ADHWTS bit in PWU_ADTC register to make the other activation factor available.

For a detailed description of the A/D conversion hardware trigger select, refer to “Section 4 Registers” of “CHAPTER 23: Partial Wakeup Control” in the Hardware manual.

5 Summary

Normally, when A/D conversion is performed from the low power consumption mode, the CPU is interrupted and the system returns to normal operation. Afterwards, it is necessary to start the A/D converter from the CPU. However, when using partial wakeup, power except RTC is disconnected. Once the RTC performs a specified count, the A/D converter is started and conversion begins without passing through the CPU. If conversion results are not within the scope of the set values, it is possible to start the CPU through interrupts. Partial wakeup makes it possible for a lower power consumption even when periodically checking for sensor malfunctions.

6 Related Documents

- S6J311E/D/C/B Series Datasheet (Doc. No.002-05681)
- S6J311A/9/8 Series Datasheet (Doc. No.002-04632)
- S6J3360/70 Series Datasheet (Doc.No.002-03359)
- S6J3400 Series Datasheet (Doc.No.001-97829)
- S6J3110 Series Hardware Manual (Doc.No.002-10667)
- S6J3360 / S6J3370 Series Hardware Manual (Contact Technical Support)
- S6J3400 Series Hardware Manual (Doc.No.002-09919)
- Traveo Family HardwareManual Platform Part for S6J3360/3370 Series (Doc.No.002-07884)

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*A	5759007	YODE	06/19/2017	Added S6J3360 and S6J3370 series to target products.

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