AN212061

Programming and Erasing Flash Memory by User Program for Traveo™ Family

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Associated Part Family: S6J3110/S6J3120/S6J3200/S6J3300/S6J3350/S6J3360/S6J3370/ S6J3400 Series

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This application note describes how to program and erase the flash memory by user program for the Traveo family. Major topics include the operation explanation of TCFLASH, the explanation of TCFLASH command and the explanation of an example of TCFLASH reprogramming.

Contents

1 Introduction

This application note describes how to program and erase the flash memory of the Traveo family. In this document, Traveo family refers to S6J3110/S6J3120/S6J3200/S6J3300/S6J3350/S6J3360/S6J3370/S6J3400 series.

2 Overview of Flash Memory

The Traveo family includes two types of flash memories: TCM flash (TCFLASH) and work flash (WorkFlash). TCFLASH is a flash memory to mainly store programs for Traveo family. WorkFLASH is rewritable, non-volatile data memory for Traveo Family. Please refer to the TRM (Technical Reference Manual) of Traveo family for details of TCFLASH and WorkFlash.

2.1 TCFLASH memory

TCFLASH is a flash memory that is used mainly to store programs. If the Traveo microcontroller is in user mode, it will be mapped to two regions: the TCM and the AXI region. TCM is the abbreviation of the Tightly Coupled Memory, it is memory that can be accessed at high speed and is directly coupled to the processor core. TCM is one of the ARM architecture. AXI is the abbreviation of the Advanced eXtensible Interface, and AXI is the most widespread AMBA interface. Please refer to a document of ARM® architecture for details of TCM and AXI. If the TCFLASH is accessed via the TCM region, it will be treated as an L1 memory on the ARM® architecture. Therefore, non-cacheable and low-latency access is possible. However, if it is accessed via the AXI region, it is treated as an L2 memory in the context of the ARM architecture.

Programming or erasing of TCFLASH can be performed, if it is accessed via the AXI region by sending a program sequence. However, programming or erasing cannot be performed when it is accessed via the TCM region.

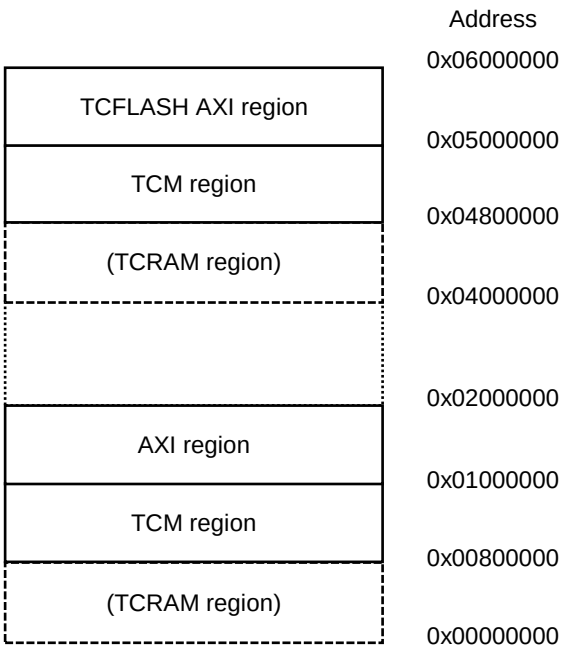
- Programming with access via the AXI region has the highest priority in TCFLASH. With the default setting, reading priority is toggled between accesses via the AXI region and accesses via the TCM region every 16 clock cycle.
- In TCFLASH, set the priority to allow reading with access via the TCM region. However, reading has a lower priority than programming.

It is possible to read 8-bit/16-bit/32-bit/64-bit data from CPU.

ECC (Error Check and Correct) is supported only in AXI with the same calculation formula as that for the ARM Cortex-R5F core, with 1-bit error correction and 2-bit error detection. If ECC is enabled, programming from the CPU is possible only in 16- or 32-bit mode. If ECC is disabled, programming from the CPU is possible in 8-, 16-, or 32-bit mode.

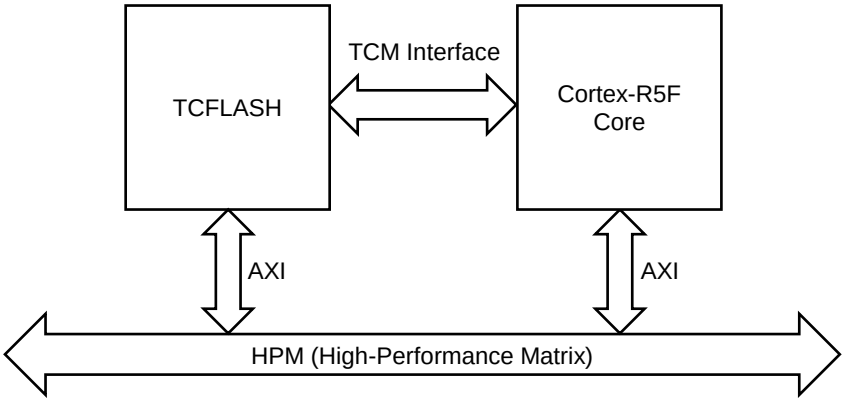
A TCFLASH memory is available only for the CPU core and is placed on the memory map by the program, as shown in Figure 1.

Figure 1. Position of TCFLASH on Memory Map



A block diagram of the TCFLASH is shown in Figure 2.

Figure 2. Block Diagram for TCFLASH and Cortex-R5F



2.2 WorkFlash Memory

The WorkFlash memory does the following:

- Enables reading in units of 8, 16, 32, or 64 bits.
- Provides an ECC function, with 1-bit error correction and 2-bit error detection.
- Enables switching between the enabled and disabled states of the ECC function through a register setting.
- Enables switching between ECC-enabled access and ECC-disabled access using two mirror areas.
- Writes the data and the ECC generated from the 64 bits.

3 TCFLASH Operation

3.1 TCFLASH Operation Mode

Traveo family when in user mode, the CPU or other bus masters can access the TCFLASH. A Cortex-R5F core can access the TCFLASH that is connected to itself via the TCM or AXI interface.

3.2 Programming and Erasing TCFLASH

Traveo family when in user mode, programming/erasing of TCFLASH is done by writing the programming access sequence in the flash memory via the AXI region.

Programming and erasing can be performed by sending the program access sequence to flash memory to start an automatic algorithm. The available commands in the automatic algorithm include reset, read, program, macro erase, and sector erase. For the sector erase command, it is possible to control the suspension and resumption of its execution.

3.3 Command Sequence for S6J3110/S6J3120/S6J3200

To start an automatic algorithm, program the given data to a given address one to seven times consecutively, depending on the command type.

- Specify the values shown in Table 1 for CA1 and in Table 2 for CA0.
- Specify the value of the lower 32 bits of the 64-bit program data for PD64_0 in Table 1. Specify the value of the upper 32 bits of the 64-bit program data for PD64_1.
- Except for the program data that is represented as PD, PD64_0, PD64_1 in Table 1, the upper 24 bits (bit 31 to bit 8) of data to be programmed to start an automatic algorithm are ignored.
- In Table 2, ***** is an arbitrary value that specifies the address range used by the flash memory for which the command is executed. For the memory map, see Figure 1.
- The address, PA, given in the 4th write cycle is the address in to which the program data, PD, is written.
- The programming address, PA, for programming must be a value that is aligned to the programming-size.

- The address SA given in the 6th program cycle of the sector erase command indicates the address of the sector to be erased. SA is specified in the same format as PA.
- The flash memory is reset and transitions to read mode if an invalid address or data set is programmed as a command or if commands are programmed in the wrong order.
- The read operation from flash memory is possible even when the command sequence is being programmed. The automatic algorithm starts upon completion of the last cycle of the program sequence.
- Do not specify the sector address for which sector protection is enabled for CA0, CA1, SA, SA0, SA1, and PA.
- Do not change the setting of the sector protection register for TCFLASH (TCFCFG0_C*SWP) while writing the command sequence.
- Flash memory must not be read-accessed until the status register READ changes to “1” after the sector erase suspend command is issued.

Table 1. Command Sequence List

Command	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle		7th Cycle	
	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Reset	CA0	0xF0	–	–	–	–	–	–	–	–	–	–	–	–
Read	RA	RD	–	–	–	–	–	–	–	–	–	–	–	–
Program	CA0	0xAA	CA1	0x55	CA0	0xA0	PA	PD	–	–	–	–	–	–
Program (64 bit)	CA0	0xAA	CA1	0x55	CA0	0xAC	PA	PD64_0	any	PD64_1	–	–	–	–
Macro Erase (Chip Erase)	CA0	0xAA	CA1	0x55	CA0	0x80	CA0	0xAA	CA1	0x55	CA0	0x10	–	–
Sector Erase	CA0	0xAA	CA1	0x55	CA0	0x80	CA0	0xAA	CA1	0x55	SA0	0x30	–	–
Multiple Sectors Erase	CA0	0xAA	CA1	0x55	CA0	0x80	CA0	0xAA	CA1	0x55	SA0	0xE0	SA1	0x30
Sector Erase Suspend	SA	0xB0	–	–	–	–	–	–	–	–	–	–	–	–
Sector Erase Resume	SA	0x30	–	–	–	–	–	–	–	–	–	–	–	–

CAx: Refer to Table 2. RA: Read Address, RD: Read Data, SAx: Sector Address, PA: Program Address, PD: Program Data, PD64_0: Program Data (lower 32 bits of 64-bit program data), PD64_1: Program Data (upper 32 bits of 64-bit program data).

Table 2. Address in the Command

Operation Mode	Code (Table 1)	Offset in AXI region
User mode	CA0	0x*****AA8
	CA1	0x*****554

3.4 Command Sequence for S6J3300/S6J3350/S6J3360/S6J3370/S6J3400

To start an automatic algorithm, preambles of the command sequence are first sent to the flash memory before sending the data. The preambles determine the modes of the flash programming/erasing. Depending on the modes, the number of the cycles for the preambles as well as for the data varies. Detailed information of different modes is given in Table 4. In the following, explanations are given to Table 4.

- The address PA given at the 4th write cycle is the address in which program data PD is written. The commands before the sending of PA and PD are preamble commands. The preambles have explicit addresses and data values.
- For addresses containing the "any" entry, it means that basically any valid Flash address can be used. However, it must be ensured, that the Flash address used has not a disabled sector write permission (TCFCFG0_CSWPx[n]=0). Otherwise the command is dropped and an error response is returned.
- For the 256bit programming mode, the "nth cycle" is 7th to 11th cycle.
- For the page mode, the "kth cycle" is 12th to 131st cycle.
- In Table 5, ***** is an arbitrary value that specifies the address range used by the flash memory for which the command is executed. The write permission of the given address must be set to "enabled". Therefore, it is recommended that the resulting Flash address should fall into the target sector. For the memory map, see Figure 1.
- To allow the macro erase operation, all sector write permissions must be set to "enabled".

- For the 16bit/32bit programming mode, the size of input data determines whether the programming is 16bit or 32bit mode.
- For the 16bit mode, the bit1 of the address determines which half of the 32bit-word in the flash is programmed. If bit1 is "0", the lower 16 bits of the 32-word are programmed. If bit1 is "1", the higher 16 bits are programmed.
- For the 64bit/256bit/page programming mode, the PDs are written to the flash memory at addresses in an increasing sequence.
- For the 64bit/256bit/page programming mode, only the address of the first 32bit-word at cycle 4 is accepted by the flash memory. The addresses starting from cycle 5 are ignored by the flash memory.
- 8-bit programming mode does not exist.
- The allowed data types for the user to program the flash must be of 16 bits or 32 bits. This rule applies not only to the programming data, but also to the preambles.
- Programming the flash using burst mode is prohibited.
- The programming address PA for programming must be a value which is programming size aligned.
- The address SA given upon the 6th program cycle of the sector erase command indicates the address of the sector to be erased. SA is specified in the same format as PA.
- Flash memory is reset and transitions to read mode if an invalid address or data set is programmed as a command or if commands are programmed in the wrong order.
- The read operation from flash memory is possible even when the command sequence is being programmed. The automatic algorithm starts upon completion of the last cycle of the program sequence.
- Do not change the setting of the sector write permission register for TCFLASH (TCFCFG0_CSWP*) while writing the command sequence.
- Two modes of sector erase suspend exist described in the following table.

Table 3. Two Modes of Sector Erase Suspend

Command	Maximum time from suspend command to suspend state	Minimum time from resume till next suspend	Erase progress
Sector Erase Suspend 1	Short	Long	Guaranteed by user
Sector Erase Suspend 2	Long	Short	Guaranteed by flash

- Flash memory must not be read-accessed until the status register READ changes to "1" after the sector erase suspend command is issued.
- The embedded algorithm operation reset command is one type of hardware reset, which terminates the Automatic Algorithm state (Program/Macro Erase/Sector Erase) of flash and changes to Normal Command state. In the Normal Command state, this macro accepts automatic algorithm execution commands (write) for executing program/erase operations and read commands (read).
- The "Command Reset" command resets the execution commands before the flash enters the Automatic Algorithm state, and enables re-write the command from the beginning.

Table 4. Command Sequence List for S6J3300/S6J3350/S6J3360/S6J3370/S6J3400

Command	1st Cycle		2nd Cycle		3rd Cycle		4th Cycle		5th Cycle		6th Cycle		nth Cycle		kth Cycle	
	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data	Address	Data
Program (16bit/32bit)	CA0	0xAA	CA1	0x55	CA0	0xA0	PA	PD	–	–	–	–	–	–	–	–
Program (64 bit)	CA0	0xAA	CA1	0x55	CA0	0xAC	PA	PD	any	PD	–	–	–	–	–	–
Program (256 bit)	CA0	0xAA	CA1	0x55	CA0	0xA4	PA	PD	any	PD	any	PD	any	PD	–	–
Page Program	CA0	0xAA	CA1	0x55	CA0	0xA8	PA	PD	any	PD	any	PD	any	PD	any	PD
Macro Erase (Chip Erase)	CA0	0xAA	CA1	0x55	CA0	0x80	CA0	0xAA	CA1	0x55	CA0	0x10	–	–	–	–
Sector Erase	CA0	0xAA	CA1	0x55	CA0	0x80	CA0	0xAA	CA1	0x55	SA	0x30	–	–	–	–
Multiple Sector Erase	CA0	0xAA	CA1	0x55	CA0	0x80	CA0	0xAA	CA1	0x55	SA	0xE0	SA	0xE0	SA	0x30
Sector Erase suspend 1	any	0xB0	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Sector Erase suspend 2	any	0xBC	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Erase resume	any	0x30	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Embedded Algorithm Operation Reset	any	0xF4	–	–	–	–	–	–	–	–	–	–	–	–	–	–
Command Reset	any	0xF0	–	–	–	–	–	–	–	–	–	–	–	–	–	–

CAx: Refer to Table 5. RA: Read Address, RD: Read Data, SAx: Sector Address, PA: Program Address, PD: Program Data

Table 5. Address in the Command

Operation Mode	Code (Table 4)	Offset in AXI region
User mode	CA0	0x*****AA8
	CA1	0x*****554

3.5 Automatic Algorithm Execution Status

The detailed status of the flash memory during the execution of an automatic algorithm can be confirmed by reading the TCFCFG_FSTAT: TCFLASH status register to check the value of each bit (refer to Table 6.) Use this status register when you use the TCFLASH. It consists of the following bits: CERS, PGMS, ESPS, ERSEC, SERS, READ, HANG, and RDY. Each bit indicates the status listed in Table 7.

If the flash memory is read during the execution of the automatic algorithm, a bus error response occurs.

Table 6. Bit Assignment of TCFLASH Status Register

Bit No.	7	6	5	4	3	2	1	0
Flag name	CERS	PGMS	ESPS	ERSEC	SERS	READ	HANG	RDY

Table 7. Values of TCFLASH Status Register

State		CERS	PGMS	ESPS	ERSEC	SERS	READ	HANG	RDY
Reset		0	0	0	0	0	0	0	0
Command		0	0	0	0	0	1	0	1
Program		0	1	0	0	0	0	0	0
Macro erase		1	0	0	0	0	0	0	0
Sector erase		0	0	0	0	1	0	0	0
Interruption of sector erasure	Sector read during erasure	0	0	1	1	1	1	0	1
	Not-target sector read during erasure	0	0	1	0	1	1	0	1
Hang-up 1	Program	0	1	0	0	0	0	1	0
	Macro erase	1	0	0	0	0	0	1	0
	Sector erase	0	0	0	0	1	0	1	0

- PGMS (Program Status) bit: This bit indicates the programming status.
- CERS (Chip Erase Status) bit: This bit indicates the macro erase status. Any command can be received until macro erase is completed.
- SERS (Sector Erase Status) bit: This bit indicates the sector erase status. During sector erase, sector erase suspend commands can be received.
- ESPS (Erase Suspend Status) bit: This bit indicates the sector erase suspend status. Reading and programming can be done for sectors other than erase targets. They cannot be done for sectors that are erase targets. The sector erase resume command resumes sector erase.
- ERSEC (Erase Suspend Sector status) bit: This bit indicates the status in which a target sector read is being executed while sector erase is suspended. At this time, the data read from flash memory is not the correct data.
- READ (Read) bit: This bit indicates the readable status of the TCFLASH.
- HANG (Hang-up 1 status) bit: This bit indicates the Hang-up 1 status, which indicates that one of the following events occurred:
  - An attempt has occurred to overwrite with value “1” an address to which the value of “0” has been written.
  - Programming, macro erase, and sector erase are not completed within the time limit.

  In the Hang-up 1 status, the status of the TCFLASH can be recovered by writing a command reset.

- RDY (Ready) bit: This bit indicates the programmable/erasable status of the TCFLASH or WorkFlash memory. When the WorkFlash memory is programmable/erasable, this bit becomes “0”.

The TCFLASH status can be confirmed with the READ and RDY bits.

- READ=0, RDY=0: Reset (TCFLASH: Waiting for ready)
- READ=0, RDY=1: Reading TCFLASH (TCFLASH: Waiting for ready)
- READ=1, RDY=1: NOP (TCFLASH: Readable/programmable/erasable)
- READ=1, RDY=0: WorkFlash memory programming/erasing (TCFLASH: Readable only)

4 Command

This section describes the following commands:

- Reset and read command
- Program command sequence
- Program command sequence (64 bit)
- Macro erase (chip erase) command sequence
- Sector erase command sequence

4.1 Reset and Read Command

This command can be used to abort any flash command and reset it to the default read state. Be careful when using it together with chip or sector erase, because incomplete erase states may result. The read/reset command is issued when writing a 0xXXF0 to any of the flash memory addresses.

4.2 Program Command Sequence

The program command sequence consists of the address/data write accesses described in Table 8.

Table 8. Program Command Sequence

Sequence	Address	Data	Comment
1st	0x****_*AA8	0xXXXX_XXAA	1st sequence write
2nd	0x****_*554	0xXXXX_XX55	2nd sequence write
3rd	0x****_*AA8	0xXXXX_XXA0	3rd sequence write
4th	PA	PD	Programming is carried out

4.3 Program Command Sequence (64-bit)

The program command sequence (64-bit) consists of the address/data write accesses described in Table 9.

Table 9. Program Command Sequence (64-bit)

Sequence	Address	Data	Comment
1st	0x****_*AA8	0xXXXX_XXAA	1st sequence write
2nd	0x****_*554	0xXXXX_XX55	2nd sequence write
3rd	0x****_*AA8	0xXXXX_XXAC	3rd sequence write
4th	PA	PD64_0	The value of the lower 32 bits of the 64-bit program data (PD64_0) is programmed.
5th	Any	PD64_1	The value of the upper 32 bits of the 64-bit program data (PD64_1) is programmed.

4.4 Macro Erase (Chip Erase) Command Sequence

The macro erase (chip erase) command sequence consists of the address/data write accesses described in Table 10.

Table 10. Macro Erase (Chip Erase) Command Sequence

Sequence	Address	Data	Comment
1st	0x****_*AA8	0xXXXX_XXAA	1st sequence write
2nd	0x****_*554	0xXXXX_XX55	2nd sequence write
3rd	0x****_*AA8	0xXXXX_XX80	3rd sequence write
4th	0x****_*AA8	0xXXXX_XXAA	4th sequence write
5th	0x****_*554	0xXXXX_XX55	5th sequence write
6th	0x****_*AA8	0xXXXX_XX10	6th sequence write

4.5 Sector Erase Command Sequence

The sector erase command sequence consists of the address/data write accesses described in Table 11.

Table 11. Sector Erase Command Sequence

Sequence	Address	Data	Comment
1st	0x****_*AA8	0xXXXX_XXAA	1st sequence write
2nd	0x****_*554	0xXXXX_XX55	2nd sequence write
3rd	0x****_*AA8	0xXXXX_XX80	3rd sequence write
4th	0x****_*AA8	0xXXXX_XXAA	4th sequence write
5th	0x****_*554	0xXXXX_XX55	5th sequence write
6th	SA0	0xXXXX_XX30	6th sequence write with SA0 address within sector to be erased

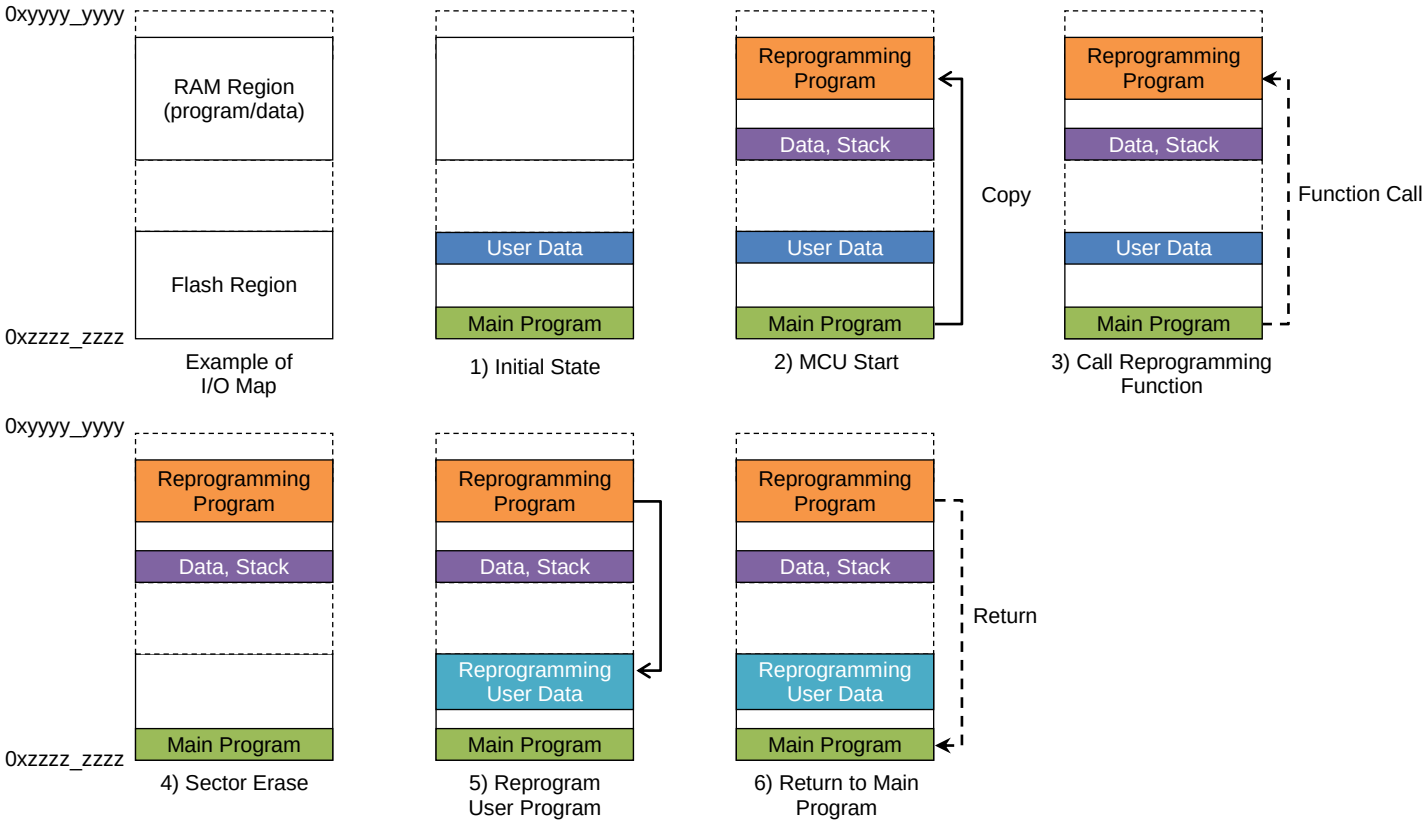
5 TCFLASH Reprogramming Procedure

The TCFLASH cannot be programmed and erased when the user program is getting executed on the TCFLASH. To program the TCFLASH, it is necessary to place the user program onto the RAM and execute it from there.

Figure 3 illustrates the reprogramming procedure as follows,

1. It is necessary to program the main program in the TCFLASH beforehand. The reprogramming program to carry out on the RAM is included in this main program.
2. When the Traveo family MCU starts, the data and stack are assigned to the RAM region and the reprogramming program is copied to the RAM by a main program.
3. The function of the reprogramming program is called from the main program in the TCFLASH.
4. The command is issued to a flash memory by executing the reprogramming program. Sector erase is performed in the sector where user data is programmed.
5. New user data is programmed in the TCFLASH.
6. If data is programmed in the TCFLASH, program execution returns to the main program on the TCFLASH by a return function.

Figure 3. TCFLASH Reprogramming Procedure

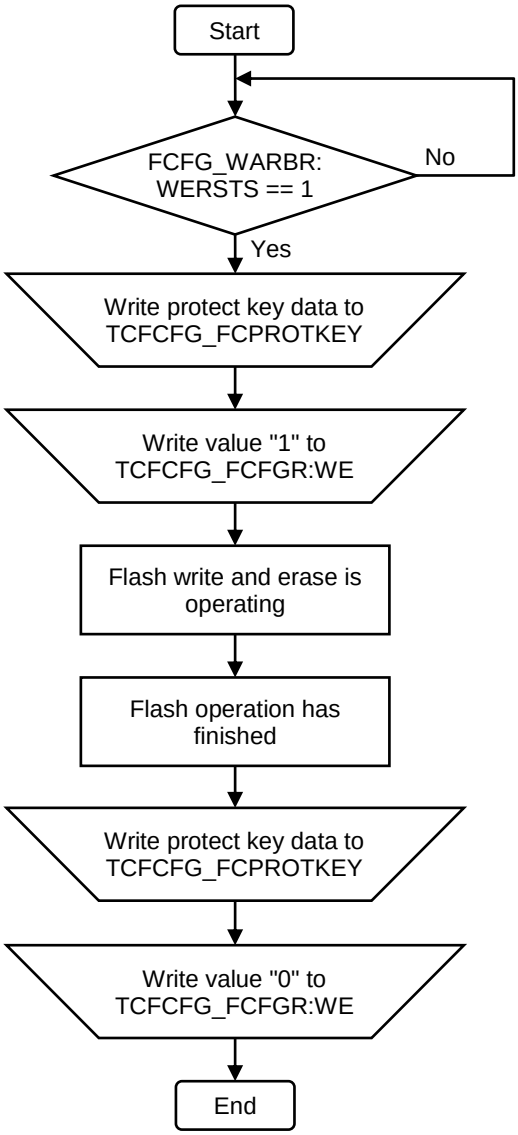


5.1 Enable Programming

To program or erase data in the TCFLASH, the program enable bit of the TCFLASH must be set. In addition, the TCFLASH and WorkFlash cannot be programmed or erased at the same time. Therefore, the flash interface (TCFLASH, WorkFlash) includes the arbitration function.

To program from the TCFLASH, the program enable bit must be enabled using the procedure depicted in Figure 4.

Figure 4. Setting Flash Memory Program Enable Bit Flow Chart



Write enable can be set using the program enable release (FCFG_WARBR:WERINT) interrupt instead of the monitoring program enable release status (FCFG_WARBR:WERSTS) bit.

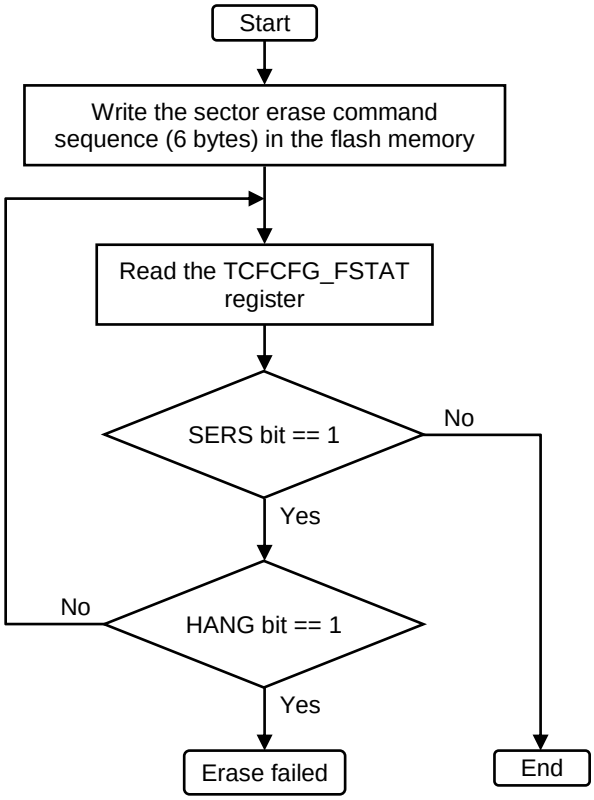
To confirm the completion of the flash program/erase, check that the programming/erasing ready bit (TCFCFG_FSTAT:RDY) has become “1”.

When programming/erasing is not required, to allow programming or erasing to the flash using the WorkFlash interface or Secure Hardware Extension (SHE), set the program enable bit (TCFCFG_FCFGR:WE) to “0”.

5.2 Sector Erase Sequence

The flow of the sector erase sequence is shown in Figure 5.

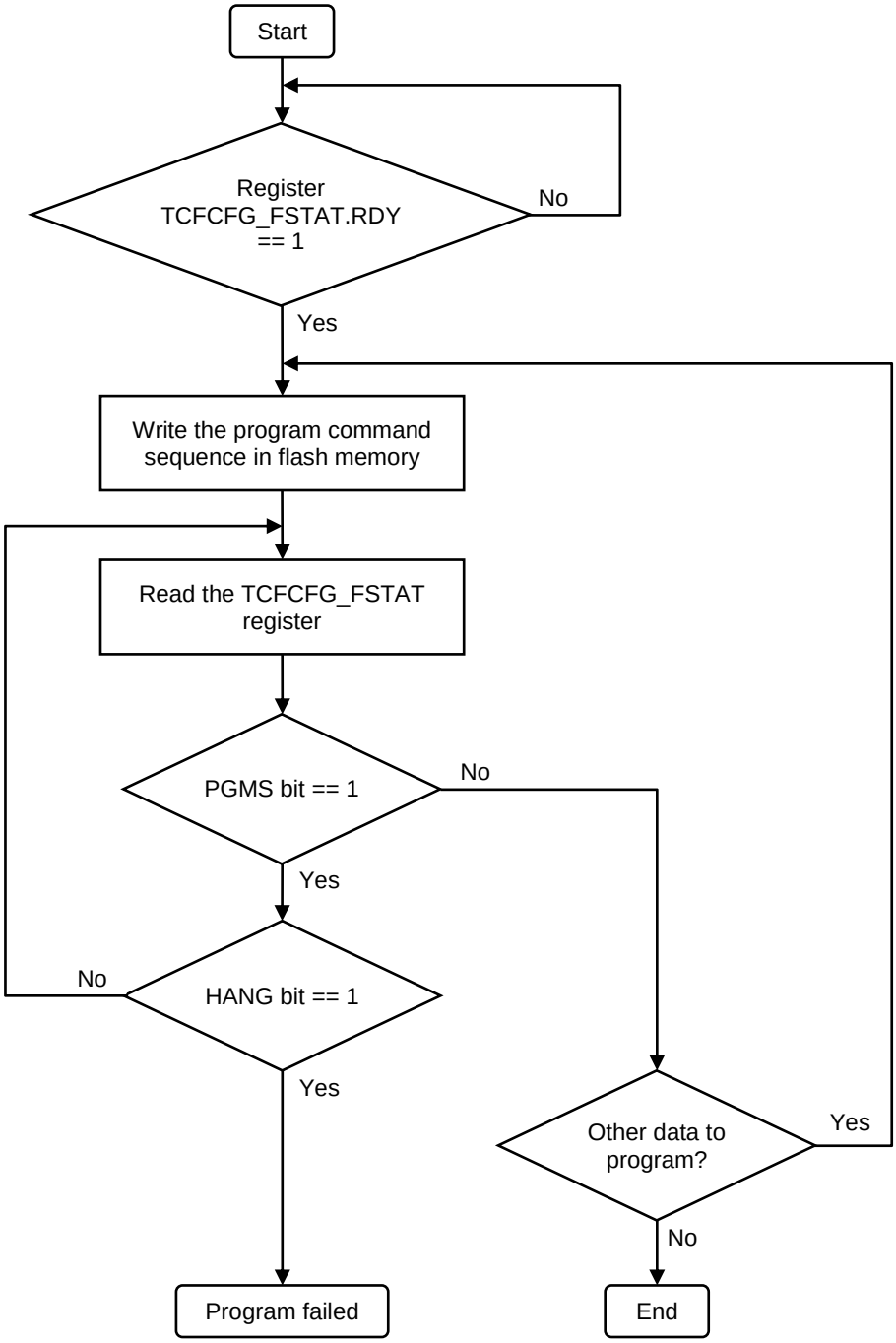
Figure 5. Sector Erase Sequence Flow Chart



5.3 Program Sequence

The flow of the program sequence is shown in Figure 6.

Figure 6. Program Sequence Flow Chart



6 Related Documents

- Technical Reference Manuals
  - S6J3110 Series Hardware Manual (Doc.No.002-10667)
  - S6J3120 Series Hardware Manual (Doc.No.002-04855)
  - S6J3200 Series Hardware Manual (Doc.No.002-04852)
  - S6J32E/F/G Series Hardware Manual (Doc.No.002-12500)
  - Traveo Family Hardware Manual Platform Part for S6J3200 Series (Doc.No.002-04854)
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- Datasheets
  - S6J311E/D/C/B Series Datasheet (Doc. No.002-05681)
  - S6J311A/9/8 Series Datasheet (Doc. No.002-04632)
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  - S6J3360/70 Series Datasheet (Contact Technical Support)
  - S6J3400 Series Datasheet (Doc.No.001-97829)

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5279026	HIAR	05/20/2016	New application note
*A	5317042	HIAR	07/11/2016	Added description of S6J3300/S6J3350/S6J3400 Added "3.4 Command Sequence for S6J3300/S6J3350/S6J3400"
*B	5655998	HIAR	03/28/2017	Added description of S6J3360/S6J3370 Modification of "6. Related Documents" chapter

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Forums | WICED IOT Forums | Projects | Videos | Blogs | Training | Components

Technical Support

cypress.com/support

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