# HYPERFLASH™ and HYPERRAM™ layout guide

## About this document

### Scope and purpose

This application note provides the layout considerations when placing an Infineon HYPERFLASH™ or HYPERRAM™ device on a PCB.

### Intended audience

This document is intended for all technical experts using Infineon HYPERBUS™ memory for a PCB design.

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# 1 Introduction

This document provides the general design recommendations for a PCB designed with Infineon HYPERBUS™ NOR Flash (S26KL/S26KS) and HYPERRAM™ self-refresh DRAM or Pseudo Static RAM (PSRAM) (S27KL/KS, S70KL/KS, and S80KS) products. It includes both the signal integrity and power delivery guidelines.

In general, the PCB design should provide impedance-controlled routing for signals, support a low-impedance power delivery system, and control EMI to achieve the maximum performance.

This document does not eliminate the need to perform signal integrity/power delivery simulations, and it is an initial reference for a PCB design with Infineon HYPERBUS™ memory. You should use the Infineon-provided IBIS models (as well as IBIS models from controller vendors) for signal timing/crosstalk simulations. In addition, it is always recommended to empirically verify the actual signal characteristics on a prototype and validation build units.

If the required design does not meet these recommendations, detailed simulations should be performed to determine whether the exceptions impact the HYPERBUS™ performance.

# 2 Signal descriptions

The following figure and tables describe various pins (and the functions) used in the HYPERBUS™ memory devices.

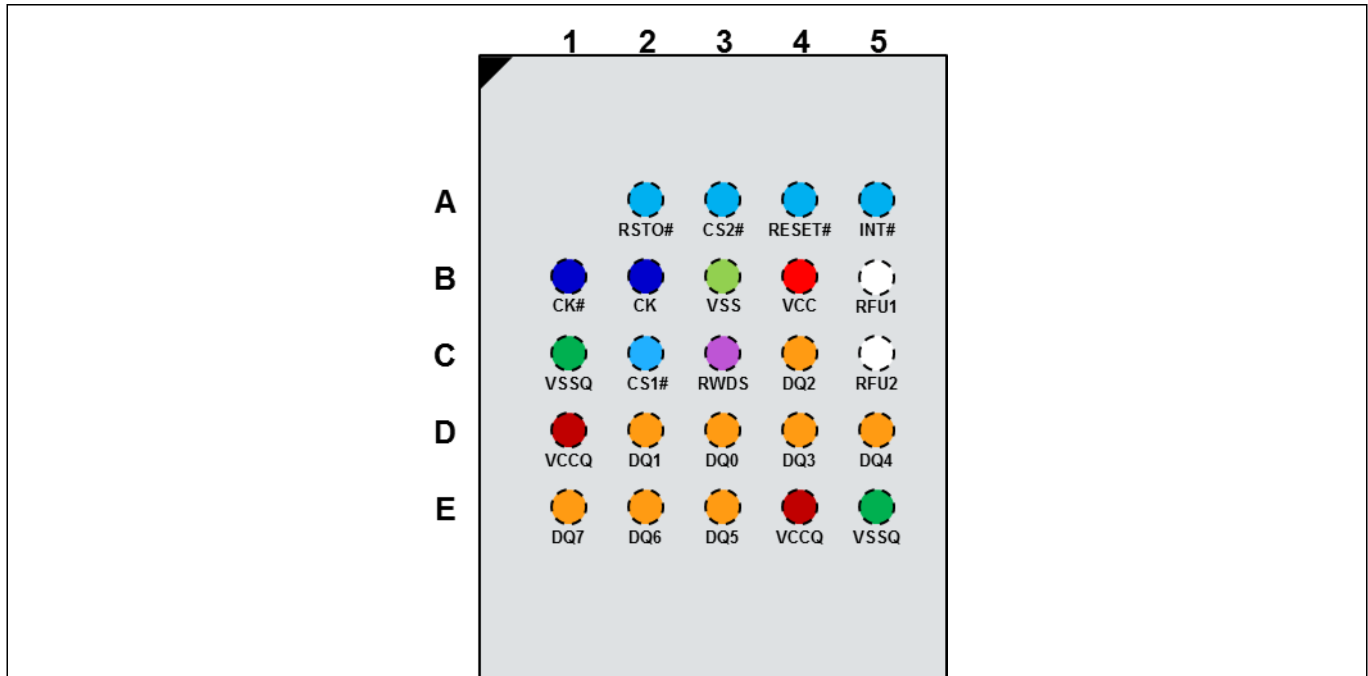


**Figure 1 HYPERBUS™ FAB024 and VAA024 ball map (top view, balls down)**

*Note: RFU1 and RFU2 are grouped together as RFU as shown in Table 3.*

**Table 1 Mandatory I/O summary**

| Symbol | Type | Description |
|---|---|---|
| CS# | Master output, slave input | Chip select. HYPERFLASH™ bus transactions are initiated with a HIGH to LOW transition. HYPERFLASH™ bus transactions are terminated with a LOW to HIGH transition |
| CK, CK# | Master output, slave Input | Differential clock. Command/address/data information is input or output with respect to the crossing of the CK and CK# signals<br>CK# is only used on the 1.8-V devices and may be left open or connected to CK on the 3-V devices. Devices with CK# optional pin (for example, HYPERRAM™ Gen 2) may leave CK# floating or bias it to either VCCQ or VSSQ |
| DQ[7:0] | Input/output | Data input/output. Command/address/data information is transferred on DQs during read and write transactions |
| RWDS | Input/output | Read-write data strobe. Output data during read transactions are edge aligned with RWDS |

**Table 2 Optional I/O summary**

| Symbol | Type | Description |
|---|---|---|
| RESET# | Master output, slave input, internal pull-up | Hardware reset. When LOW, the device will self-initialize and return to the array read state. RWDS and DQ[7:0] are placed into the HI-Z state when RESET# is LOW. RESET# includes a weak pull-up; if RESET# is left unconnected, it will be pulled up to the HIGH state |
| RSTO# | Master input, slave output, open drain | RSTO# output. RSTO# is an open-drain output used to indicate when a POR is occurring within the device and can be used as a system-level reset signal. Upon completion of the internal POR, the RSTO# signal will transition from LOW to HI-Z after a user-defined timeout period has elapsed. Upon transition to the HI-Z state, the external pull-up resistance will pull RSTO# HIGH and the device immediately is placed into the idle state. This pin is not applicable to HYPERRAM™ devices |
| INT# | Master input, slave output, open drain | INT output. When LOW, the device indicates that an internal event has occurred. This signal is intended to be used as a system-level interrupt for the device to indicate that an on-chip event has occurred. INT# is an open-drain output. This pin is not applicable to HYPERRAM™ devices |

*Note: The Extended-IO (x16) HYPERRAM™ has two RWDS signals - RWDS 0 and RWDS1 to control DQ[7:0] and DQ[15:8] respectively.*

**Table 3 Other connectors summary**

| Symbol | Type | Description |
|---|---|---|
| VCC | Power supply | Core power |
| VCCQ | Power supply | Input/output power |
| VSS | Power supply | Core ground |
| VSSQ | Power supply | Input/output ground |
| NC | No connect | Not connected internally. Signal/ball may be used in PCB as part of a routing channel |
| RFU | Reserved | Reserved for future use. May or may not be connected internally, and the signal/ball should be left unconnected and unused on PCB as part of a routing channel for future compatibility. Signal/ball may be used by a signal in the future |
| DNU | No connect | Do not use. Reserved for use by Infineon Technologies. Signal/ball is connected internally, and must be left open on PCB |

# 3 Package breakout recommendations

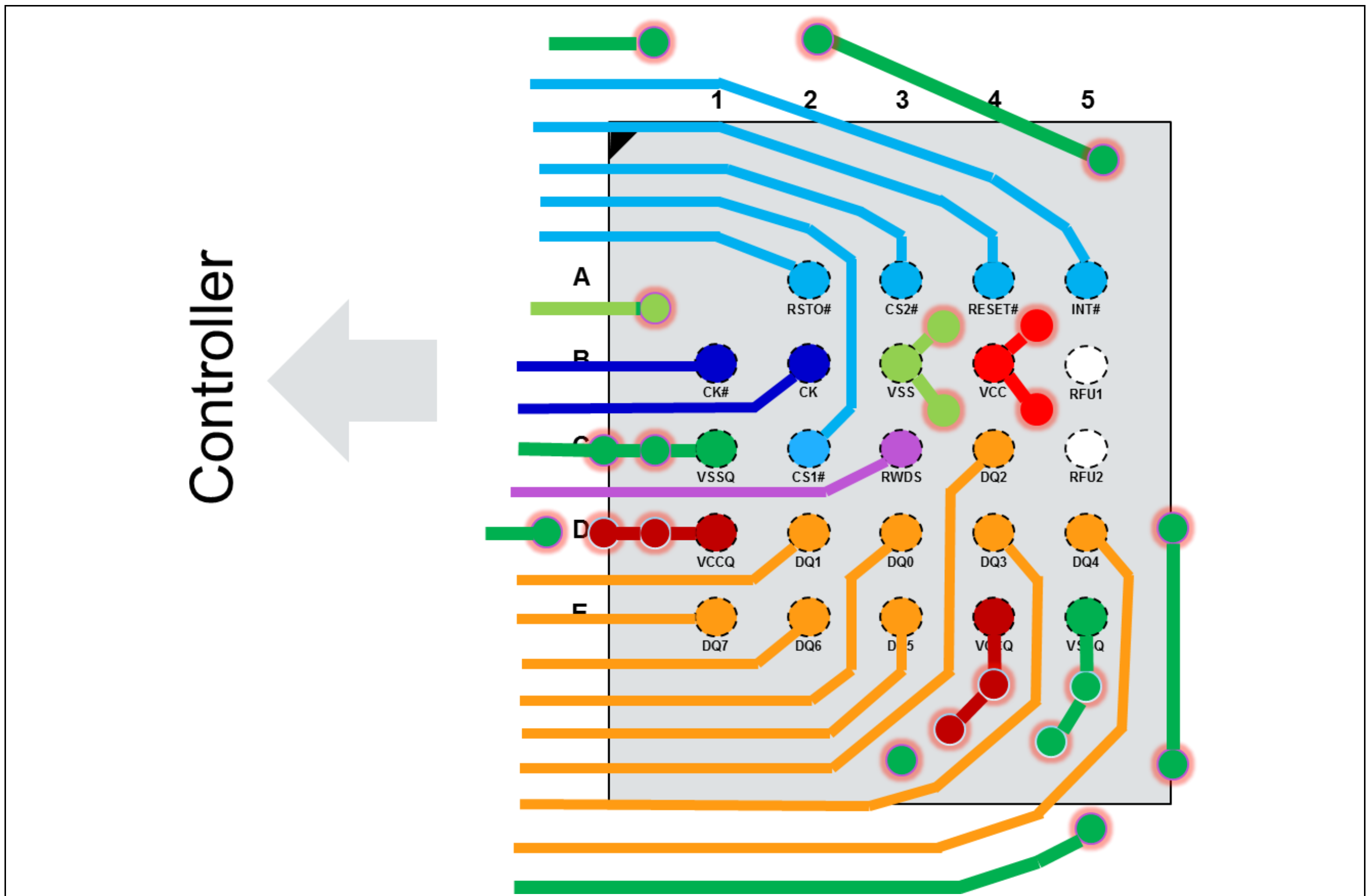


**Figure 2 FAB024 and VAA024 PCB breakout**

*Note: Although both CS1# and CS2# breakouts are shown in the figure above, breakout only the chip selects required for the specific configuration (see the applicable datasheet).*

- As shown in Figure 2, it is possible to breakout all signals on the top layer before redirecting them towards the controller. This is only one of the options for breakout. If multiple layers are available for breakout, different breakout strategies can be used as long as the routing and power delivery guidelines as shown in this section and the **General signal routing guidelines** section are met
- **VSSQ** and **VSS** should be taken to VSS plane layer with at least two vias next to each solder ball. Traces from land pad to via should be as thick as possible
- **VCC** and **VCCQ** should be taken to VCC plane layer with at least two vias next to each solder ball. Traces from land pad to via should be as thick as possible
- As shown in Figure 2, the priority is given to first breakout **DQ (0-7)** as well as **RWDS** in the direction of the controller to allow for the smallest data channel length between HYPERBUS™ memory and controller
- **CK** and **CK#** should be broken out in a coupled fashion, that is, maintain the trace width and trace spacing between these signals identically throughout the breakout region as much as possible (this is true when they exit the breakout area). In addition, shield the clocks with VSS guard traces, if possible
- All signals should be broken out on the top layer while maintaining a solid VSS underneath. This will allow better impedance control and smaller impedance mismatch between breakout traces and traces outside the breakout area

**Package breakout recommendations**

- The VSS guard traces shown in Figure 2 are meant to act as an additional referencing against signals of other interfaces and must be more planar and well stitched with the VSS layer (shown as traces only for pictorial reasons)
- Within the PCB breakout region, use the following SMT recommendations:
  - Ball-to-ball pitch: 1.00 mm
  - Ball pad size: 0.35 mm
  - SR opening size: 0.5 mm
- Minimum trace width and trace spacing: 4 mil or larger spacing between traces (at least 4-mil trace width: 4-mil trace spacing). Once the routing clears the breakout region, it is recommended to follow the general routing guidelines described in this section
- Whenever through-hole vias are used to move breakout traces to inner layers, the potential via coupling effect (from one signal via to another signal via) should be considered at the breakout region. Preferably, no vias should be used for DQ7[7:0] and RWDS signal routes. If they have to be used, minimize the via count and use same number of vias on all DQ[7:0] and RWDS. It is preferred to use µvias or buried vias instead of through-hole vias

# 4 General signal routing guidelines

The following guidelines define the recommended impedance, trace width/spacing, total length limitation, and length-matching requirements to achieve optimal signal integrity and timing margins:

- The exact values of signal trace width and trace spacing should be determined based on the trace impedance requirement
- It is preferred to have a solid VSS as reference for all signal routing layers. Reference planes should avoid any gaps or voids to minimize return current discontinuity
- Isolate the ground return path of analog signals from digital noise whenever applicable
- Infineon recommends that the VSS plane should be used as the primary reference or return path for all signals. Whenever a power layer is used as the reference plane, it is important to ensure that the power layer is low-noise and there is proper stitching at the reference plane transitions to guarantee return path continuity (especially at high frequency). The power layer should only be considered as a secondary signal reference option where a solid continuous ground reference is present
- All the recommended signal routing lengths are defined from package pin (source) to package pin (destination) by considering HYPERBUS™ package length compensation
- Electrical properties of the recommended signal routing are based on dielectric material with FR4
- It is assumed that 1 inch is ~166 ps (assuming FR4 material). The signal integrity tools should be used to ensure the accuracy of this assumption
- Consider performing signal integrity simulations using Infineon-provided IBIS models to determine actual guidelines suitable for the application. The guidelines below should be used as a starting reference
- Normally, signal delay is measured between T***vm*** (timing reference voltage, which is usually VCCQ/2) of the source and T***vm*** of the destination. However, pay attention to the signal polarity in the datasheet to determine the edge the timing is measured at (rising or falling edge)

*Note: The routing principals and guidelines as described for x8 I/O (DQ[7:0]) devices also apply for the Extended-IO (x16) HYPERRAM™.*

## 4.1 Microstrip versus stripline versus coplanar signal routing

**Table 4 Comparison of microstrip, stripline, and coplanar signal routing**

| Microstrip line | Stripline | Coplanar line |
|---|---|---|
| Suffers from dispersion and non-TEM (Transverse Electrical and Magnetic) modes | Pure TEM mode | Suffers from dispersion and non-TEM modes |
| Easy to fabricate | Difficult to fabricate | Fairly difficult to fabricate |
| High-density trace | Mid-density trace | Low-density trace |
| Fair for coupled-line structures | Good for coupled-line structures | Not suitable for coupled-line structures |
| Need through-holes to connect to ground | Need through-holes to connect to ground | No through-hole required to connect to ground |

- Either microstrip or stripline signal routing is allowed as long as the continuous trace impedance of 50 Ω (±10%) is maintained through the entire routing path. Manufacturing tolerances of layer thickness, dielectric constant, and so on should be modeled in the impedance calculation
- In general, whenever through-hole vias are used on the board, they cause impedance discontinuities due to additional capacitive loading as well as possible inductive stubs at a high frequency. Any via that attaches to

a trace will change the delay of that trace. It is therefore preferred to use µvias or buried vias and keep the via count at minimum

- In order to preserve a tight skew relationship, DQ[7:0] and RWDS should have the same number of vias and layer changes. This will help to ensure that the data signals along with the accompanying strobe will experience the same effective delay
- It is recommended to route DQ[7:0] and RWDS on the same signal layer
- CK and CK# should be routed in a coplanar fashion while maintaining the single-ended impedance of 50 Ω and differential impedance of 100 Ω (nominal value)

## 4.2 Signal-routing length constraints

### 4.2.1 Maximum total length

The absolute maximum total length of DQ signals (including RWDS) with respect to its reference plane is defined by the total load capacitance, which directly impacts the signal quality.

- The total load capacitance is preferred to be less than the bus load ($C_L$) specified in the datasheet
- Total load capacitance includes the following:
  - Total line length capacitance (~3.3 pF/inch with FR4 assumption)
  - Maximum package pin capacitance of the controller package
  - Any parasitic capacitance associated with vias and so on

### 4.2.2 Length matching

Length matching refers to trace lengths from the HYPERBUS™ memory package pin to the signal pin of the controller and must include the effective electrical length of the vias.

**Table 5 Length matching**

<table>
<tr><th rowspan="2">Signal group</th><th colspan="3">Length matching tolerance</th></tr>
<tr><th>200 MHz</th><th>166 MHz</th><th>100 MHz</th></tr>
<tr><td>CK to CK#</td><td>±10 mils</td><td>±10 mils</td><td>±20 mils</td></tr>
<tr><td>RWDS to DQ[7:0]</td><td>±15 mils</td><td>±25 mils</td><td>±50 mils</td></tr>
<tr><td>RWDS1 to DQ[15:8] [1]</td><td>±15 mils</td><td>±25 mils</td><td>±50 mils</td></tr>
<tr><td>DQx [7:0] to DQy [7:0]</td><td rowspan="2">±30 mils</td><td rowspan="2">±50 mils</td><td rowspan="2">±100 mils</td></tr>
<tr><td>DQx [15:8] to DQy [15:8] [1]</td></tr>
<tr><td>CK/CK# to DQ[7:0]</td><td rowspan="2">±200 mils</td><td colspan="2" rowspan="2">±500 mils</td></tr>
<tr><td>CK/CK# to DQ[15:0] [1]</td></tr>
<tr><td>CK/CK# to CS#</td><td colspan="3">±1500 mils</td></tr>
<tr><td>CK/CK# to RWDS</td><td colspan="3">±1500 mils</td></tr>
<tr><td>RESET# to RSTO# to CS#</td><td colspan="3">±2000 mils</td></tr>
</table>

*Note: The length matching criteria for "RWDS to DQ[7:0]" and "DQx [7:0] to DQy [7:0]" requires RWDS length to be the mid-point of minimum and maximum length DQx [7:0] , that is, [(min DQx[7:0] )+(max DQx [7:0] )]/2.*

[1] Extended-IO HYPERRAM™

### 4.2.3 Signal spacing constraints from other signals

- CK and CK#: >2H
- RWDS: > 1H
- DQ[7:0] and DQ[15:8] : >1.5H
- CS#, CS2#: >1.5H
- INT#, RESET, RST_N: >1.5H
  - where, H is the height of the dielectric between the signal and VSS (reference layer)

### 4.2.4 Termination

You should review the drive strength/impedance of the controller I/O for CK, CS#, RWDS, and DQ as well as transmission line routing to determine whether the series termination is required on these lines.

### 4.2.5 PCB design consideration

See **AN202751** application note for the pad size and surface mount assembly recommendations for the Infineon FBGA packages.

# 5 Power delivery guidelines

The following power delivery guidelines will help to ensure that there are no power issues in the system:

- Connect the VSS/VSSQ balls to a solid ground plane with its own unique via and, if possible, >1 vias. This will improve the IR drop
- Connect the VCC/VCCQ balls to a single supply plane with its own unique via and, if possible, >1 vias. This will improve the IR drop
- Isolate VCC/VCC of HYPERBUS™ from other noisy supply floods. If the supplies of HYPERBUS™ and non-HYPERBUS™ have to be co-located on the same plane layer, maintain a >40-mil gap. In addition, if possible, add shielding VSS guard traces between the planes for further isolation
- It is recommended to keep the supply trace lengths ≤400 mil and trace width ≥20 mils. This applies to HYPERBUS™ memory, MCU, as well as voltage regulator routing
- Maintain low-impedance routing (traces >20mils) from voltage regulator to HYPERBUS™ supply pins as well as from voltage regulator to controller HYPERBUS™ I/F supply pins

It is recommended to add the VCC/VSS test points as close to the HYPERBUS™ memory package as well as next to the voltage regulator. This will allow the measurement of the VCC-VSS waveform at both VRM as well as HYPERBUS™ memory package.

*Note: Follow the decoupling guidelines provided by the microcontroller and VRM vendors.*

## 5.1 Decoupling capacitor recommendations

- Place the following PCB decoupling capacitors as close to the HYPERBUS™ memory package as possible:
  - At least two 1-µF 0402 ceramic capacitors
  - At least four 0.1-µF 0402 ceramic capacitors
  - Place one 1-µF capacitor closest to D1 (VCCQ) and another closest to E4. Similarly, two 0.1-µF capacitors closest to D1 and another two closest to E4
  - If VCC and VCCCQ are shorted, make sure that the short is as low-impedance as possible. If the short is not low-impedance, it is recommended to add 0.1-µF and 1-uF capacitors close to the VCC pin
  - In Extended-IO HYPERRAM™ (49-ball BGA) place one 1-µF capacitor and one 0.1-µF capacitor closest to each VCC and VCCQ pin.
- The selected capacitor should have low ESL and ESR
- VCC and VSS trace routing from the capacitor should be as wide as possible to avoid the inductive/resistive effects
- X7R or X5R capacitors are recommended with rated voltage ≥6.3 V
- Capacitor placements on either top layer or bottom layer are allowed as long as the capacitor is electrically close to the DQ routing and VCCQ/VSSQ pins (for example, do not place the capacitors at the bottom while using a thicker board)

# 6 Test points and oscilloscope measurements

Signal quality, timing, and power delivery characterization should be performed as per the industry standards, and high-speed digital signal evaluation techniques. Some of these techniques are outlined below:

- Test points should be added as close to the controller for DQ0-7/RWDS and close to the HYPERBUS™ memory package for all signals.
- When the controller is driving, the significant signal to consider is as close to HYPERBUS™ memory as possible, and when the HYPERBUS™ memory is driving, it is vice versa.
- While creating a test pad, the stub (extra inductance and capacitance) resulting from such a pad should be minimized. If you can probe at the breakout via, it is better than creating test pad stubs. In addition, in the case of a 4-layer PCB with through-hole vias, if possible, probe the signals at the bottom of the PCB on these vias.
- While performing the scope measurements, use a 6-GHz or greater bandwidth scope and high-impedance probes. This will show the waveform transition (such as, rising and falling portion of the waveform) more accurately.
- Always measure VCC-VSS at the controller, voltage regulator, next to the connector (either side), and at the HYPERBUS™ memory. This has to be performed before making any signal measurements to ensure that the supply is not noisy. A noisy supply will impact the signal timing. In addition, these measurements establish the IR drop from regulator to controller or regulator to HYPERBUS™ memory.
- While measuring signals, it is a good idea to set the trigger on the most common switching signals, such as clock or RWDS.

## Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| ** | 2016-03-24 | Initial release. |
| *A | 2016-10-12 | • Clarified decoupling recommendation<br>• Updated template |
| *B | 2017-05-19 | Changed low-impedance probes in Section 6 to high-impedance probes |
| *C | 2022-06-08 | Updated to Infineon template.<br>Included high speed, high density HYPERRAM™ Gen 2 and HYPERRAM™ Gen 3 MPNs.<br>Added reference for HYPERRAM™ Gen 3.0 (Extended-IO, x16).<br>Added routing guidelines for 200-MHz access speed.<br>Added section **4.2.5** on PCB design consideration. |

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**Edition 2022-06-08**

**Published by**

**Infineon Technologies AG**

**81726 Munich, Germany**

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**Document reference**

**002-11622 Rev.*C**

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