Supporting HYPERBUS™ and Octal SPI with a common physical layout

About this document

Scope and purpose

This application note describes the key pinout and electrical differences between Infineon HYPERBUS™ NOR Flash and alternate source Octal SPI NOR Flash devices packaged in 24-ball FBGAs. Note these differences when designing an application to enable drop-in ball-to-ball replacement of Octal SPI with HYPERBUS™ devices on the same physical footprint.

Intended audience

This document is intended for all technical experts using the Infineon Technologies serial interface memories.

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1 Introduction

HYPERBUS™ and Octal SPI are both high-performance 8-bit wide serial interfaces used to connect a host system master with one or more slave devices. Both interfaces transmit data and command/address information in Double Data Rate (DDR) fashion over the 8-bit data bus. The clock input signals are used for signal capture by the devices when receiving command/address/data information. Data Strobe (RWDS/DQS/DS), which is an output in both interfaces, indicates when data is being transferred out of the devices to the host. RWDS/DQS/DS is referenced to the rising and falling edges of the clock during the data transfer portion of read operations. Command/address/write-data values are center-aligned with the clock edges, whereas read-data values are edge-aligned with the transitions of RWDS/DQS/DS.

The biggest advantage of serial interface memories is a reduction in the number of signals needed for the memory connection. This in turn frees up host system connections resulting in reduced package and multi-layer PCB cost. However, serial memories historically have lower data throughput or longer random-access time. This is mitigated in HYPERBUS™ and Octal with a high-performance multi I/O DDR architecture where source-synchronous data is captured at twice the clock frequency rate. Thus, a HYPERBUS™ or Octal device operating at a clock frequency of 200 MHz has a peak data transfer rate of 0.4 GB/s. A design where the internal data bus is twice the width of the external data bus and data capture occurs twice per clock cycle is required. To ensure signal integrity at such high-speed data throughputs, a bidirectional data strobe signal is provided.

Figure 1 provides a data throughput comparison across different interfaces.

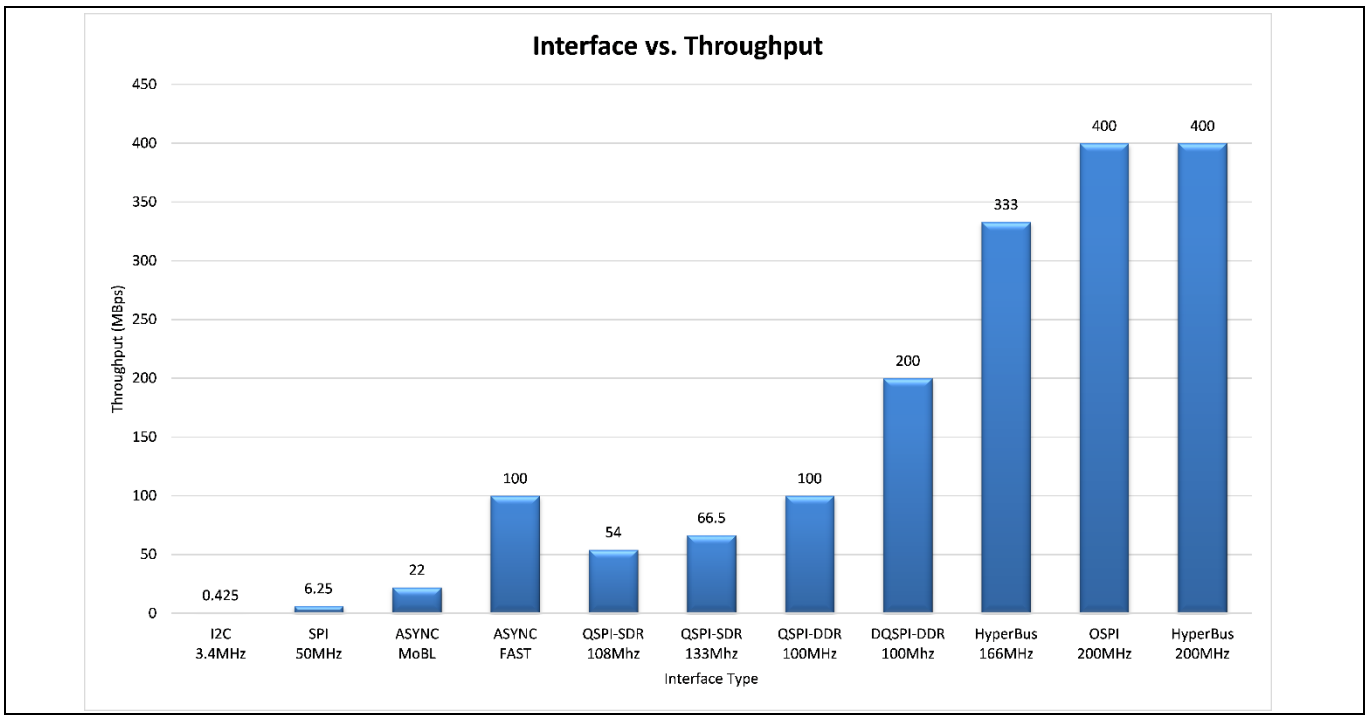

Figure 1 Interface data throughputs

All the HYPERBUS™ and Octal inputs/outputs are LVCMOS-compatible supporting either 1.8 V or 3.0 V (nominal) voltage supplies. Control signals are all single-ended except for the master clock. Octal master clock is single-ended whereas HYPERBUS™ requires the master clock to be differential for the 1.8-V architecture only.

HYPERBUS™ and Octal instruction protocols follow the traditional industry-standard Serial Peripheral Interface (SPI). Every transaction begins with the assertion of Chip Select (CS#). This is followed by the transfer of Command and Address bytes with access latency and either read or write data transfers, until CS# is de-asserted.

2 Supporting HYPERBUS™ and Octal with a common physical layout

This section highlights Infineon HYPERBUS™, Octal interface, and alternate-source Octal products (Micron Xccela, Macronix OctaFlash) in terms of package pinouts, signals, and electrical specifications. It also discusses physical design layout considerations to enable substitution.

2.1 24-Ball FBGA package

The 24-ball FBGA package is shown in **Figure 2**.

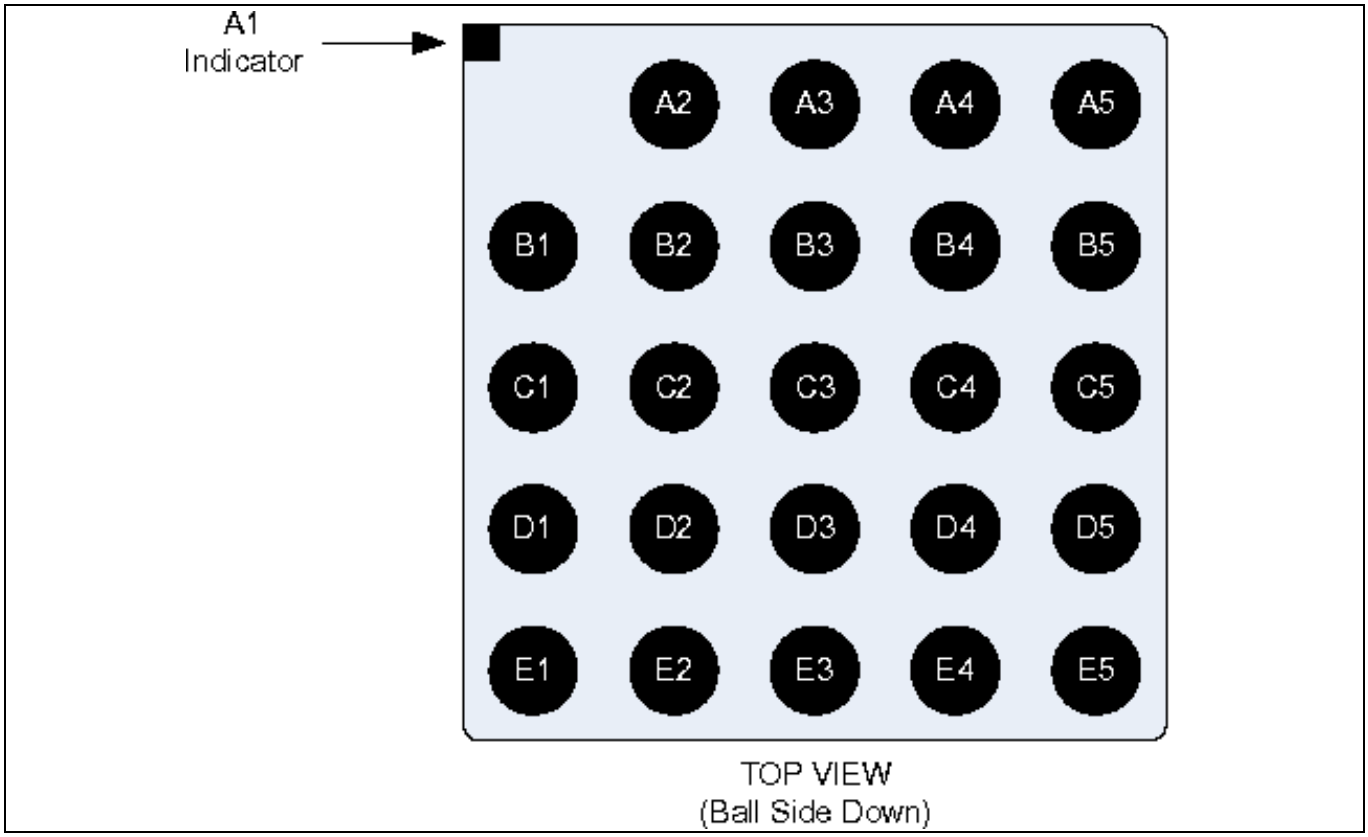

Figure 2 24-Ball FBGA package

2.2 Package compatibility

Infineon HYPERBUS™ products, Octal, and alternate-source Octal products are offered in the 24-ball FBGA packages. The dimensions of the packages are similar and socket compatible, as shown in **Table 1**.

Table 1 24-Ball FBGA package comparison

Package dimensions	Infineon HYPERBUS™, Octal				Micron Xccela Octal		Macronix OctaFlash	
	6 mm × 8 mm package (mm)		8 mm x 8 mm[1] package (mm)		6 mm × 8 mm package (mm)		6 mm × 8 mm package (mm)	
	Min	Max	Min	Max	Max	Maxi	Min	Max
Height (body)		1.00		1.00	**1.00**	1.20		1.20
Length (body)		8.00		8.00	**7.99**	8.01	7.90	8.10
Width (body)		6.00		8.00	**5.99**	6.01	5.90	6.10
Length (max footprint)		4.00		4.00		4.00		4.00
Width (max footprint)		4.00		4.00		4.00		4.00
Ball count		24		24		24		24
Ball pitch		1.00		1.00		1.00		1.00
Ball height	0.20		0.20		**0.25**	0.35	0.25	0.35

2.3 Pinout compatibility

Infineon HYPERBUS™, Octal, and alternate-source Octal mandatory and optional signals description is summarized in Table 2 andTable 3, respectively. Active LOW signal names have a hash symbol (#) suffix.

Table 2 Mandatory I/O summary

Pin name	Type	Description
CS# S#	Input	Chip select. Bus transactions are initiated with a HIGH to LOW transition. Bus transactions are terminated with a LOW to HIGH transition
C CK	Input	Clock. Command, address, and data information is input or output with respect to the crossing of CK. The clock is not required to be free-running
CK# (HYPERBUS™)	Input	Clock#. Command, address, and data information is input or output with respect to the crossing of CK#. The clock is not required to be free-running
DQ[7:0] SIO[7:0]	Input/output	Data input/output. Command, address, and data information is transferred on these signals during read and write transactions
RWDS DQS	Input/output	Read data strobe. Output data during read transactions are edge-aligned with RWDS/DQS

[1]The BGA package 6 mm × 8 mm and 8 mm × 8 mm have the exact same footprint.

Pin name	Type	Description
DQ		
RESET#	Input	Hardware reset. When LOW, the device will self-initialize and return to the array read state. RWDS/QDS and DQ[7:0] are placed into the HI-Z state when RESET# is LOW. RESET# includes a weak pull-up; if RESET# is left unconnected, it will be pulled up to the HIGH state
VCC	Power supply	Core power
VCCQ	Power supply	Input/output power
GND VSS	Power supply	Core ground
VSSQ	Power supply	Input/output ground

Table 3 Optional I/O summary

Pin name	Type	Description
RSTO# *(*Infineon HYPERBUS™*)*	Output (open drain)	RSTO# output. RSTO# is an open-drain output used to indicate when a POR is occurring within the device and can be used as a system-level reset signal. Upon completion of the internal POR, the RSTO# signal will transition from low to high impedance after a user-defined timeout period has elapsed. Upon transition to the high impedance state, the external pull-up resistance will pull RSTO# HIGH and the device immediately is placed into the Idle state
INT# *(*Infineon HYPERBUS™, Octal*)*	Output (open drain)	INT output. When LOW, the device is indicating that an internal event has occurred. This signal is intended to be used as a system-level interrupt for the device to indicate that an on-chip event has occurred. INT# is an open-drain output
V_{PP} (Xccela)	Power supply	Programming power (Micron Xccela)

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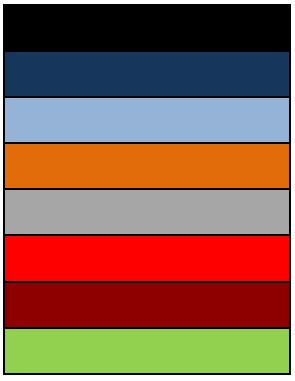
The 24-ball FBGA package pinout compatibility is summarized in **Table 4**.

Table 4 24-Ball FBGA package pinout compatibility

Pin #	Infineon HYPERBUS™	Infineon Octal	Micron Xccela Octal	Macronix OctaFlash
A1	N/A	N/A	N/A	N/A
A2	RSTO#	RFU	RFU	NC
A3	RFU	RFU	RFU	NC
A4	RESET#	RESET#	RESET#	RESET#
A5	INT#	INT#	DNU	DNU
B1	CK#	RFU	RFU	NC
B2	CK	CK	C	SCLK
B3	VSS	VSS	VSS	VSS
B4	VCC	VCC	VCC	VCC
B5	RFU	RFU	DNU	NC
C1	VSSQ	VSS	VSS	VSSQ
C2	CS#	CS#	S#	CS#
C3	RWDS	DS	DQS	DQS
C4	DQ2	DQ2/W#	DQ2/W#	SIO2
C5	RFU	VPP	VPP	NC
D1	VCCQ	VCC	VCC	VCCQ
D2	DQ1	DQ1	DQ1	SIO1
D3	DQ0	DQ0	DQ0	SIO0
D4	DQ3	DQ3	DQ3	SIO3
D5	DQ4	DQ4	DQ4	SIO4
E1	DQ7	DQ7	DQ7	SIO7
E2	DQ6		DQ6	SIO6
E3	DQ5		DQ5	SIO5
E4	VCCQ		VCC	VCCQ
E5	VSSQ		VSS	VSSQ



Not available
Reserved for future use/do not use/not connected
Control pins
Optional functionality pins (programmable)
Data pins
Power
High-voltage power
Ground

2.4 Physical layout guidelines

To optimize substitution, Infineon recommends building the board layout connects as shown in **Figure 3**.

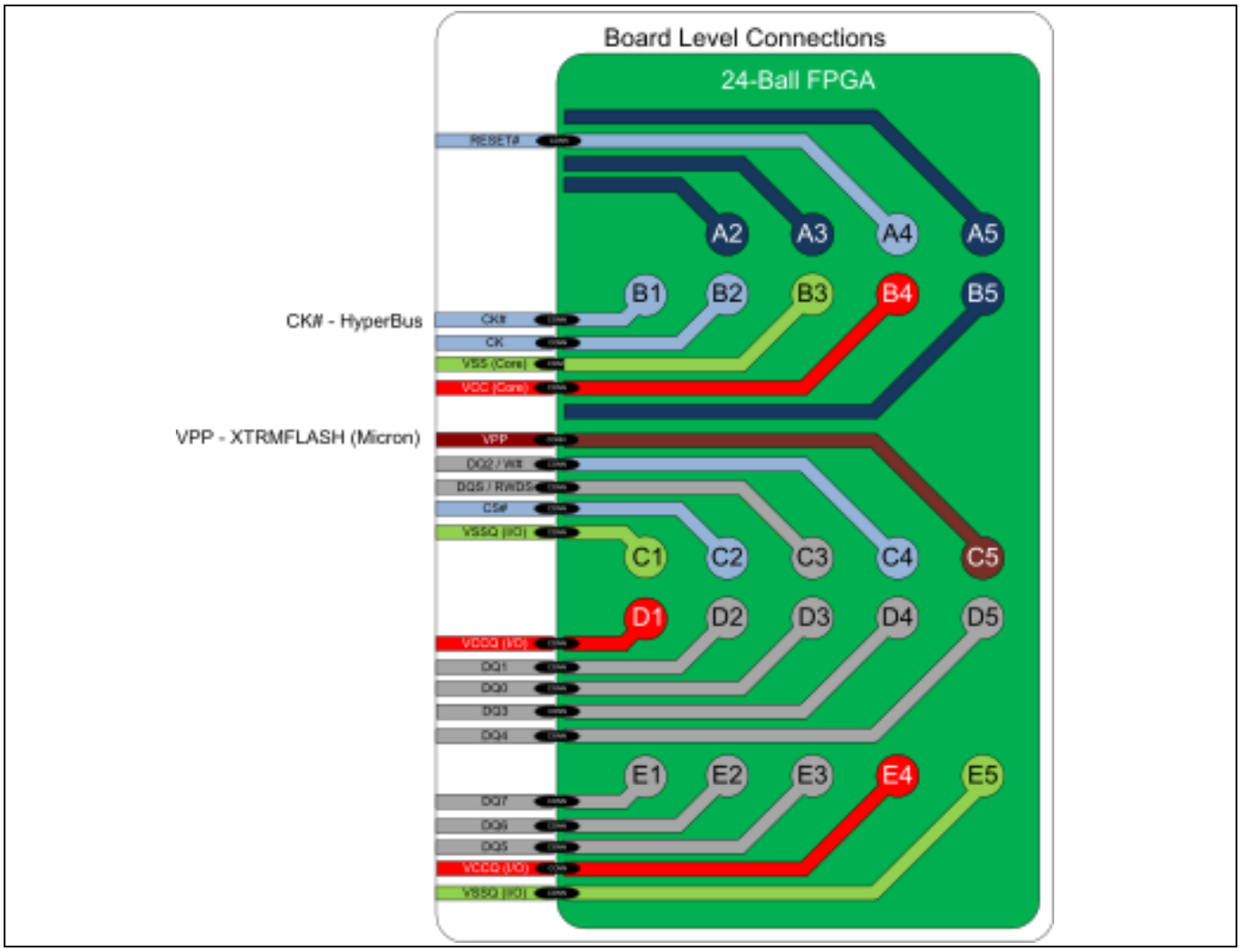


Figure 3 24-Ball FBGA physical board layout

HYPERBUS™ optional pins pose a potential conflict. Infineon recommends avoiding the usage of INT# and RSTO# functionalities because they fall on DO-Not-Use (DNU) and Reserved-for-Future-Use (RFU) pins for Micron Xccela, respectively.

3 Summary

With forethought on PCB layout and care taken to avoid RSTO# and INT# optional pins, Infineon HYPERBUS™ products are pin-compatible with Octal SPI products. Following the instructions in this application note will allow the HYPERBUS™ products to be a ball-to-ball replacement for Octal SPI products.

Revision history

Document version	Date of release	Description of changes
**	2016-04-01	New specification.
*A	2022-05-25	Updated to Infineon template.

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