# AN211139

# FPD-Link PCB Guidelines for the Traveo Family S6J3200 Series MCUs

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**Associated Part Family: Traveo Family S6J3200 Series**

**Related Application Notes: AN213250**

**Related Documents: For a complete list, click here.**

AN211139 provides guidelines for PCB layout for the flat panel display link interface (FPD-Link) for Cypress's Traveo™ Family S6J3200 Series MCUs.

## 1 Introduction

Traveo Family S6J3200 Series MCUs have a flat panel display link interface (FPD-Link, with TxCLK± and TxDOUT[0:3]±), used to connect high-performance video displays. FPD-Link is a high-speed interface (max 350 Mbps/lane) using low-voltage differential signaling (LVDS).

The FPD-Link graphics display port of S6J3200 Series MCUs has the following characteristics:

- High speed: Data rates up to 350 Mbps per lane
- Low voltage swing: Approximately 350 mV
- Five differential signals: TxCLK± and TxDOUT[0:3]±

Because of these characteristics, the PCB for FPD-Link cannot be treated as a simple group of traces. This application note provides guidelines for the layout of the FPD-Link PCB for S6J3200 Series devices.

## 2 Recommended PCB Specifications

The following best practices are recommended for routing the LVDS signals used in an FPD-Link interface:

- Use balanced transmission lines with a characteristic impedance of 100 Ω ±10%.
- Avoid vias by using the programmable inversion and output signal selection[1] abilities of the FPD-Link Controller.
- Ensure that the PCB design conforms to the parameters listed in Table 1.

[1] S6J3200 Series MCUs can select the output signal for FPD-Link. Refer to Chapter 30 in the Hardware Manual for more details.

Table 1. PCB Layout Trace Space, Width, and Length

| Symbol | Description | Recommended Dimensions | As shown in |
|---|---|---|---|
| $S_{DP}$ | Space between differential pair signals (CLK+ [2] and CLK– [3] or DIF+ [4] and DIF– [5]) | Minimum Pair spacing [6] | Figure 1, Figure 2, Figure 3 |
| $S_{DD}$ | Space between differential signals and GND, between differential CLK± and differential DIF±, or between differential DIF± and other differential DIF± | Minimum Pair spacing x 2 | Figure 1, Figure 2, Figure 3 |
| $S_{DC}$ | Space between differential signals and logic signals | Minimum Pair spacing x 4 | Figure 2 |
| $W_{PCB}$ | Width of trace | Trace width [6] | Figure 1, Figure 2, Figure 3 |
| $L_{DP}$ | Length difference between the true (+) and complement (–) signals of a differential pair (CLK+ and CLK–, or DIF+ and DIF–) [7] | Maximum 5 mm | Figure 4 |
| $L_{DD}$ | Length difference between any two differential signals (CLK± and DIF±, or between DIF± and any other DIF±) [7] | Maximum 5 mm | Figure 4 |

# 3 PCB Design Considerations

## 3.1 Layer Layout

Balanced transmission lines for the FPD-Link signals may be implemented as any of the following types: [8]

- Edge-coupled microstrip [9, 10]
- Edge-coupled stripline
- Broadside-coupled stripline

This application note shows edge-coupled microstrip in the examples.

If the PCB has four or more layers, use the structure shown in Figure 1. This places the balanced microstrip traces on one side of the board, and the noisy logic traces on the opposite side of the board. [11]

[2] CLK+ is the true/positive (+) signal of the differential clock

[3] CLK– is the complement/negative (–) signal of the differential clock

[4] DIF+ is the true/positive (+) signal of a differential data line

[5] DIF– is the complement/negative (–) signal of a differential data line

[6] This value is determined by the specifications of the layer thicknesses and dielectric materials used by the board manufacturer. To ensure proper differential impedance in manufacturing, it is recommended to include a test transmission line on a coupon adjacent to each board, and verify the transmission line impedance as part of the test process of the bare board.

[7] For microstrip transmission lines in FR-4 with a dielectric constant of 4.7

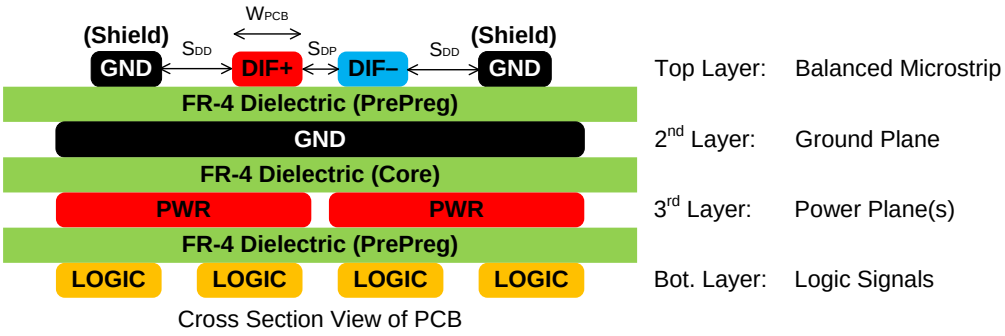
[8] While any of these transmission line constructs can be used, they should not be mixed; i.e., do not use balanced microstrip for some of the signals and balanced stripline for others. The signals propagate at different rates on these transmission lines, which makes it difficult to maintain matched delays.

[9] Most design equations for microstrip and balanced microstrip do not take into account the dielectric impact of the soldermask layer. When selecting a new board manufacturer, a test board allowing evaluation of multiple different spacings is recommended to determine the target values for the board design.

[10] Do not use gold-plated traces as a replacement for soldermask. The nickel diffusion-barrier layer has ferromagnetic properties that distort high-speed signals.

[11] LVDS signals are ground-referenced. When implementing balanced microstrip transmission lines, it is preferred to have them coupled to a ground plane instead of a power plane. When coupled to a power plane, noise on that supply is coupled as common-mode noise to the signals on the transmission lines.

Figure 1. Layout Guidelines for 4-layer PCBs




Cross Section View of PCB

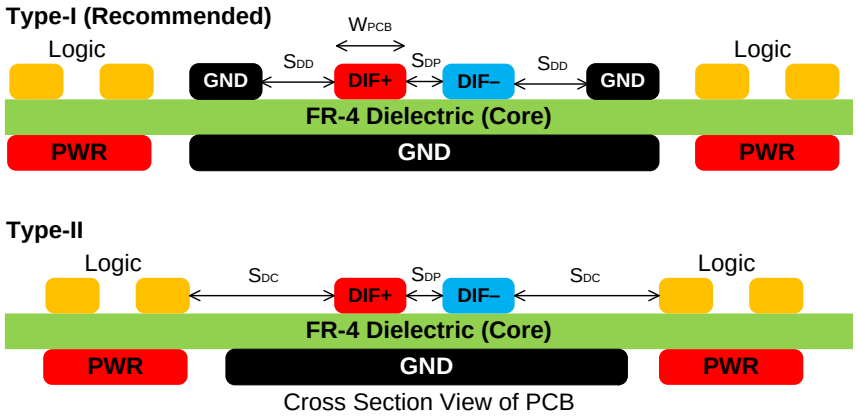
If the PCB has only two layers, or requires both logic and balanced microstrip traces on the same layer, the methods in Figure 2 are often more appropriate.

- Type-I: Use a GND trace between any logic trace and the nearest trace of any balanced transmission line to act as a shield.
- Type-II: Use at least four times the space between the traces of a balanced microstrip transmission line as the space between any logic trace and either trace of that balanced transmission line (see Equation 1).

$$S_{DC} = 4 \times S_{DP} \quad \text{Equation 1}$$

Figure 2 shows examples of Type-I and Type-II recommended layouts.

Figure 2. Recommended Layouts




Cross Section View of PCB

## 3.2 Balanced Transmission Lines Spacing

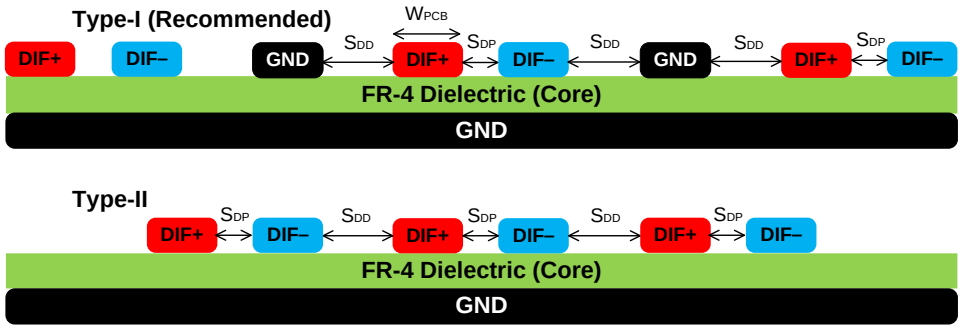
When two or more balanced transmission lines are present in the same layer, do the following:

- Type-I: Use a ground (GND) trace between each balanced transmission line to act as a shield.
- Type-II: Use twice the space between the traces of a balanced microstrip transmission line and other balanced transmission lines (see Equation 2).

$$S_{DD} = 2 \times S_{DP} \quad \text{Equation 2}$$

Figure 3 shows two examples of balanced transmission lines spacing.

Figure 3. Balanced Transmission Lines Spacing



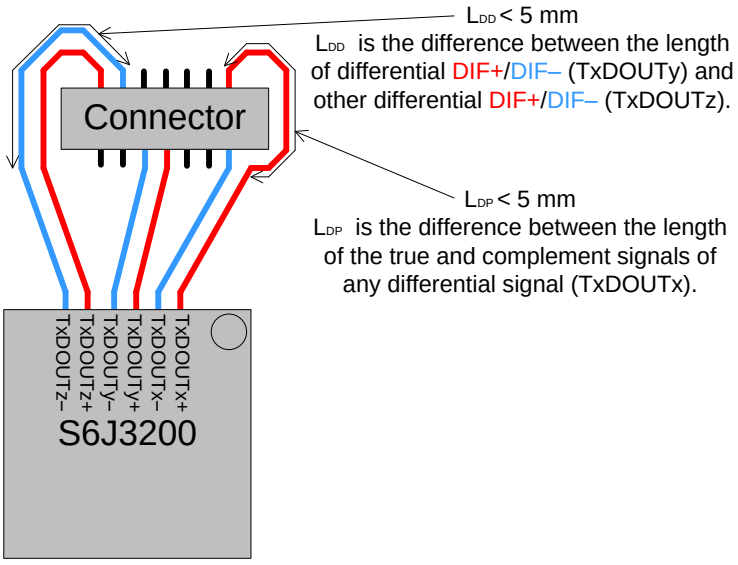

Cross Section View of PCB

## 3.3 Physical Length / Delay Matching

The physical length of the traces that form each balanced transmission line, and how well they are matched, determine much of the signal integrity and timing margin of the interface. Length matching must be managed both between the true and complement traces that form each balanced transmission line ($L_{DP}$) and between different balanced transmission lines ($L_{DD}$). The matching of physical length is used to limit the conversion of a differential signal into common-mode, and the differences in delay of each transmission line between the source and destination.

Figure 4 shows three differential pairs routed between the sending device (S6J3200) and a connector, and how routing can introduce differences in physical length.

Figure 4. Physical Length




Of the three balanced transmission lines shown in Figure 4, the TxDOUTy± signal has the best matching of trace length within the balanced pair ($L_{DP}$). The TxDOUTz± signal has some mismatch, but in most of the cases, this should be acceptable. The TxDOUTy± signal, however, has a large difference in trace length between the TxDOUTx+ and TxDOUTx– signals, and this should be avoided.

When routed as a balanced microstrip on FR4, each millimeter of length equates to approximately 10 ps of delay [12], and every millimeter of length difference between traces equates to a time offset of 10 ps. When there is a difference in length between the true and complement traces of a balanced transmission line, the electromagnetic field between

[12] For microstrip transmission lines in FR-4 with a dielectric constant of 4.7

these two traces becomes unbalanced, and some of the energy in the signal gets converted to common-mode. This conversion should be avoided wherever possible for the following reasons:

- Common-mode energy radiates as EMI
- Common-mode noise couples as crosstalk to nearby signals
- Imbalance causes a reduction in differential signal integrity

As noted in Table 1, Cypress recommends limiting the mismatch between true and complement signals within a balanced pair ($L_{DP}$) to no more than 5 mm or 50 ps. This limitation is based on the rise / fall time of the signals on these transmission lines (typically 400 ps), and remains the same regardless of the signaling rate.

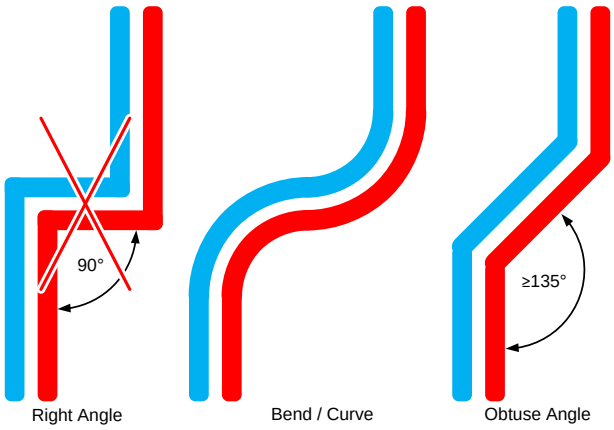
While there appears to be a significant signal length mismatch ($L_{DD}$) between the TxDOUTy± and TxDOUTz± signals, the routing to one connector only shows a part of the transmission line. Because there is often a second connector at the other end of the cable, the exit-routing of that connector may be used to compensate for the entry-routing to a local connector. When measuring $L_{DD}$, the total mismatch in length is between the pins of the sending device (S6J3200) and the pins of the receiving device (normally a display), and not just with the local connector.

The recommendation in Table 1 for $L_{DD}$ is also 5 mm (50 ps), but this is for operation at the 50-MHz clock rate of the FPD-Link interface. The $L_{DD}$ mismatch causes an increase in the transmit pulse position offset (TPPOS) by offsetting the clock and data signals. With a TxCLK± of 50 MHz, each data line carries 350 Mbps of video; the unit interval (UI) of this data is 2.85 ns. At this signaling rate, a 50-ps offset is less than 0.02 UI, and reduces the link timing margin by less than 2%. At slower signaling rates, larger $L_{DD}$ offsets are usually acceptable so long as the interface meets the setup and hold requirements at the display end of the FPD-Link interface.

## 3.4 Trace Routing Limitations

Do not use 90-degree bends when routing traces; instead, use 45-degree angles or curves because Sharp bends have additional capacitance between the traces, which causes a change in the transmission line impedance. Figure 5 shows trace routing recommendations.

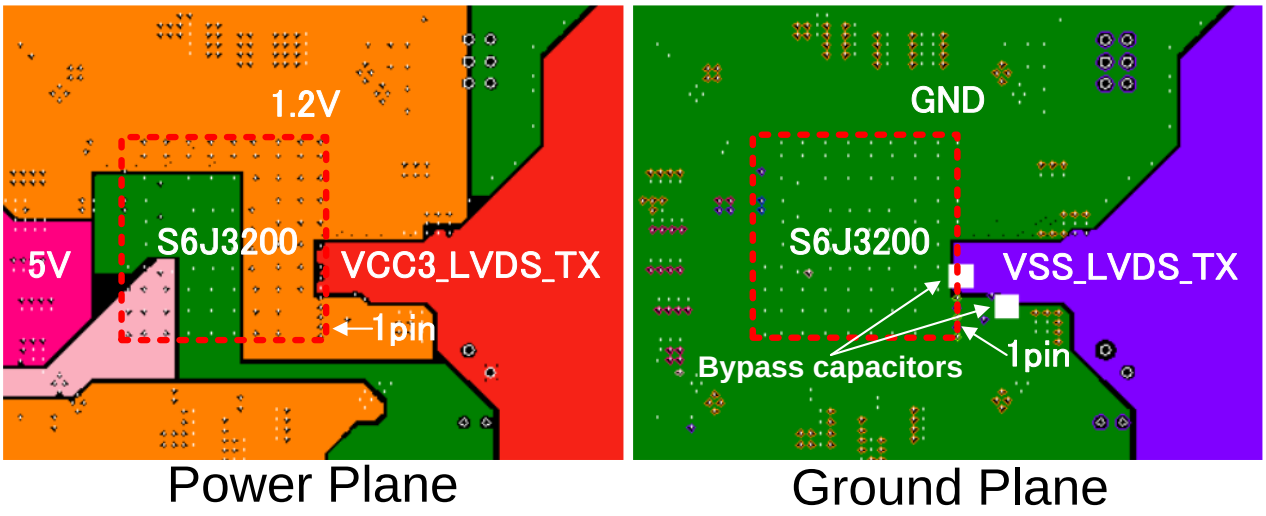
Figure 5. Trace Routing Recommendations




## 3.5 Layout of Power and Ground

Power and ground traces should be as short and wide as reasonably possible. Power for the FPD-Link should be isolated from other power domains of the regulator. Put bypass capacitors near power / ground pins. Figure 6 shows a layout of power and ground.

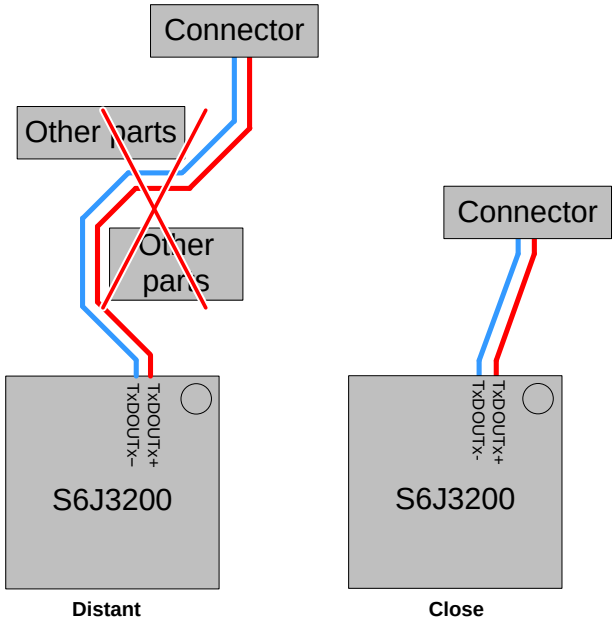
Figure 6. Layout of Power and Ground




## 3.6 Distance Between IC and Connector

Theoretically, the distance between the driver and receiver on a transmission line should have limited impact on the signaling. In reality, the longer and more complex the routing between these points, the larger the imbalance introduced into the signals and the more difficult it becomes to maintain a matched delay for all five balanced pairs. When possible, place the IC as close as possible to the FPD-Link connector. Figure 7 shows the recommended routing between the IC and connector.

Figure 7. Distance Between IC and Connector



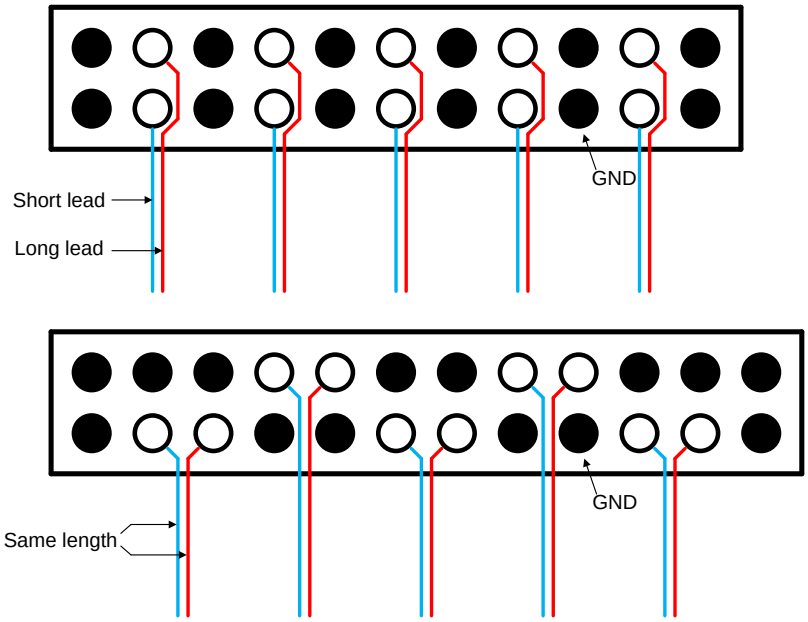
## 3.7 Signal Assignment to the Connector

When assigning signals to the pins of the connecter, consider the following:

- Connectors must have a low skew with matched impedance.
- Select connectors with the same lead lengths for a lower skew and crosstalk.
- Route the true and complement signals of the same differential pair to adjacent pins of the connector.
- If possible, place ground pins between differential pairs.
- End pins of the connectors should preferably be grounded and must not be used for high-speed signals.
- Terminate all unused pins of the connector to ground.

Figure 8 shows two examples of signal assignments of the connector. While the signal assignment on the upper diagram does introduce a mismatch in signal length between the true and complement signals of the differential pair ($L_{DP}$), if the pin spacing between rows of the connector is small (<3 mm), this should remain below the 5-mm target. Signal assignment in the lower diagram introduces a small difference in length between differential signals ($L_{DD}$). This can be compensated by adjusting the lengths of the signals at the other end of the cable exiting from the opposite side of the connector.

Figure 8. Signal Assignment to the Connector




# 4 Related Documents

- S6J3200 Series 32-bit Microcontroller Traveo Family Hardware Manual
- Traveo Family Hardware Manual Platform part
- S6J3200 Series 32-bit Microcontroller Traveo Family Data Sheet

## Document History

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| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | 5131209 | HMIZ | 10/21/2016 | New application note. |
| *A | 6205704 | YSAT | 06/13/2018 | Adapted new Cypress logo |

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