AN209853

HyperRAM™ Refresh Interval Optimization

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Associated Part Family: S27KL0641 S27KS0641

AN209853 discusses how the refresh interval in a Cypress HyperRAM™ device can be changed to optimize the read throughput and standby current when it is operated below the maximum temperature.

1 Introduction

The Cypress HyperRAM family of products are high-speed CMOS, Self-refresh Dynamic RAM (DRAM) devices with a HyperBus interface.

The core DRAM array requires periodic refresh of all bits in the array. This can be done manually by the host system reading or writing a location in each row. This access copies a row of bits to an internal buffer. At the end of the access, the bits in the buffer are written back to the row in memory, thereby recharging (refreshing) the bits in the row of DRAM memory cells. All rows must be accessed within a given time period, the refresh interval, or the data will decay and become corrupted.

However, the host system generally has better things to do than to access every row in memory and ensure that each row in the array is visited within the required refresh interval. The HyperRAM family devices include a self-refresh logic that will refresh all the rows automatically so that the host system is relieved of the need to refresh the memory. The automatic refresh of a row can only be done when the memory is not being actively accessed by the host system. The refresh logic waits for the end of any active access before doing a refresh, if a refresh is needed at that time. If a new read or write begins before the refresh is completed, the memory will drive RWDS HIGH during the Command-Address period to indicate that an additional initial latency time is required at the start of the new access in order to allow the refresh operation to complete before starting the new access.

The required refresh interval for the entire memory array varies with temperature. Table 1 shows the default refresh parameters for the device. The “Array Refresh Interval” is the time within which all rows must be refreshed. The self-refresh logic distributes single-row refresh operations throughout the interval. This ensures that the refresh windows are as short as possible. The host must also leave the device enough time to perform these operations by keeping the length of the accesses it makes to a safe length. The t_{CMS}, CS# LOW maximum time, describes the maximum amount of time the host can access the device and still allow the self-refresh logic to operate. If there are no active host accesses, a single row will be refreshed every t_{CMS}.

Table 1. Default Refresh Parameters

Maximum Device Operating Temperature (°C)	Array Refresh Interval (ms)	Array Rows	Recommended t_{CMS} (µs)
85 (Industrial)	64	8192	4
105 (Industrial Plus)	16	8192	1

2 Refresh Parameters

The default t_{CMS} time is set to ensure that the device will operate at the maximum operating temperature for the device. If the device is not operating at the maximum temperature, the device can be configured for a longer t_{CMS}.

The t_{CMS} value is set by writing to bits 1-0 in Configuration Register 1. Table 2 describes the values in Configuration Register 1.

Table 2. Configuration Register 1 Bit Assignments

CR1 Bits	Function	**Settings** (Binary)
15-2	Reserved	000000h—Reserved (default) Reserved for Future Use. When writing to this register, these bits should be cleared to 0 for future compatibility.
1-0	Distributed Refresh Interval	10b—default 4 µs for Industrial temperature range devices 1 µs for Industrial Plus temperature range devices 11b — 1.5 times default 00b — 2 times the default t_{CMS} 01b — 4 times the default t_{CMS}

3 Optimizing the Refresh Interval

As described in Table 1, Cypress HyperRAM devices come in two temperature grades: Industrial, which are optimized for operation up to 85º C, and Industrial Plus, which are optimized for operation up to 105º C. Table 1 shows what the default value of the Distributed Refresh Interval means. If the device is going to be operated at temperatures below the maximum allowed value for its grade, the Distributed Refresh Interval value in Configuration Register 1 can be changed to allow for a larger t_{CMS}. A larger t_{CMS} will allow the host more throughput to the device with a longer refresh interval; this means that less time needs to be dedicated to refresh so the host can use more time to transfer data. Because of the self-refresh feature, when the device is in the standby state, it alternates between periods of inactivity and periods of refresh activity. During the refresh periods, the device draws more current. By making the time between refresh operations larger, there is more inactive time and the average current draw is lower.

If the device is an Industrial Plus (105º C) device and it is operating at temperatures at or below 85º C, it is safe to change the Distributed Refresh Interval value in Configuration Register 1 to 01b to allow a t_{CMS} of 4 µs. Making this change will decrease the standby current by approximately 30%.

If the device is an Industrial (85º C) device and it is operating at temperatures at or below 25º C, it is safe to change the Default Refresh Interval value in Configuration Register 1 to 00b to allow a t_{CMS} of 8 µs. Making this change will decrease the standby current by approximately 15%.

See the Register Space section of the HyperRAM datasheet for information on how to write to Configuration Register 1.

Table 3 shows the additional bytes that can be transferred before CS# must be deactivated to allow self-refresh.

Table 3. Performance Values

Temperature Grade	Part Number	Operating Temperature	Default t_{CMS}	Max t_{CMS}	Default Bytes per Transfer[1]	Maximum Bytes per Transfer
Industrial Plus	S27KL0641[2]	Less than 85º C	1 µs	4 µs	186	786
	S27KS0641[3]	Less than 85º C	1 µs	4 µs	314	1314
Industrial	S27KL0641	Less than 25º C	4 µs	8 µs	786	1406
	S27KS0641	Less than 25º C	4 µs	8 µs	1314	2648

4 Summary

If the guidelines described in this application note are followed, it is possible to increase the throughput to/from a Cypress HyperRAM device while also lowering its average standby current.

5 Related Documents

HyperRAM datasheet

[1] Transfer bytes = ((t_{CMS} / Max Clock) – (3 Command cycles + wait states)) * 2 bytes per cycle

[2] Max Clock = 10 ns Wait states required at maximum clock = 4

[3] Max Clock = 6 ns Wait states required at maximum clock = 6

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
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*A	5869125	AESATMP8	08/31/2017	Updated logo and Copyright.

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