AN209375

Recommendation for Hardware Setup 32-Bit FR81S Family

This application note describes how to set up a hardware environment for Cypress FR81S MCUs. As an example, the CY91F52x MCU is used.

Contents

1 Introduction

This design guide describes design restrictions and recommendations regarding signal wiring and the electrical power system of the MCU. For more details about the device features and its relevant settings, please refer to the FR81S Hardware Manual and its corresponding Datasheet for electrical characteristics.

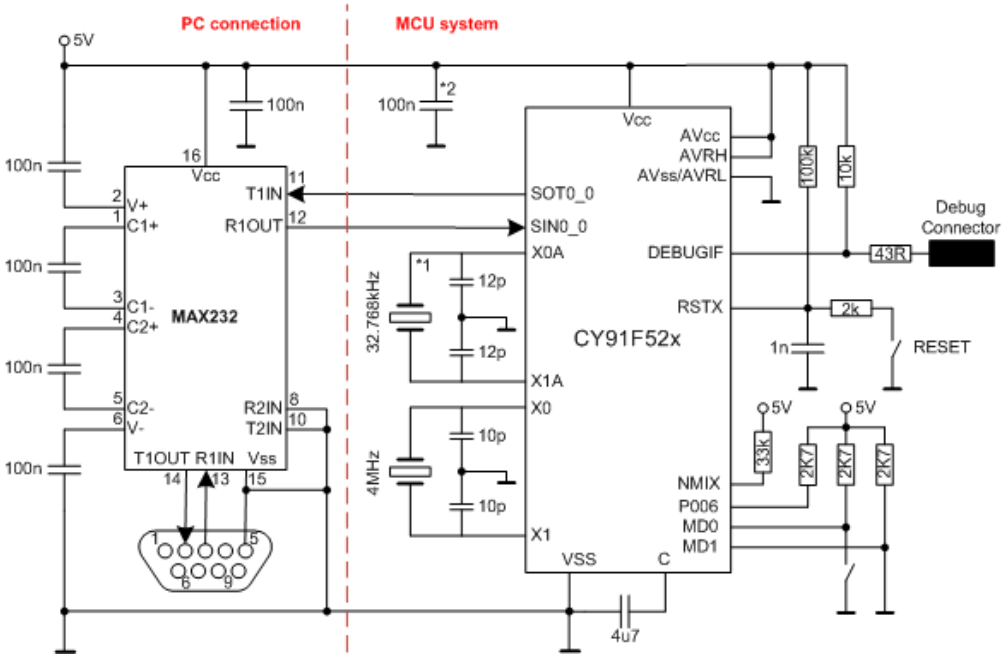
2 Minimal System

This chapter gives an example for a minimum hardware system.

2.1 Schematic

The following graphic shows a schematic of a minimum hardware system. Note that for other MCU families a different pinning is needed.

Figure 1. Principal Schematic for Minimal Requirements



*1 only needed for dual clock devices.

*2 please refer to chapter 3.6 Recommended Power Supply Circuit.

2.2 Serial Interface

The “PC connection” section is only needed, if no 5 V external serial data lines for programming exist. The MAX232 is a standard level shifter, which converts the 5 V levels of the MCU to ±12V RS232V24 levels and vice versa.

If you use a 3.3 V system a MAX3232 is recommended.

Please consider, that the internal charge pumps of the level shifter can produce noise on the +5 Volts line, which can influence the ADC, if AVCCn and AVRHn are directly (unfiltered) connected to it.

2.3 Power supply

The power supply should be from 2.7 Volts to 5.5 Volts for normal usage. If a different supply voltage is used please refer to the corresponding data sheet.

2.4 Analog Digital Converter Supply Pins

The analog converter supply pins (AVCCn, AVRHn / AVRLn, AVSSn) should be connected even if the ADC of the MCU is not used. Please refer to our application note “mcu-an-300215-e-16fx_adc” for using the ADC and pin connection.

2.5 Analog Input Pins

Because the ADC works with an internal sample capacitor (Cadc) you must be aware of the time needed to fully charge this capacitor to the corresponding analog signal source voltage level by the end of the sample time.

When the external impedance is too high, the sampling period for analog voltages may not be sufficient. In this case, it is recommended to connect an external capacitor (Cext, approx. 0.1 µF) to the analog input pin.

An input impedance maximum (Rext) 15k Ohm is recommended. So, an appropriate sample time has to be selected depending on the impedance Rext and the capacitance Cext.

Please refer to Datasheet “A/D Converter” chapter for further information.

Figure 2. Analog Input Circuit Model

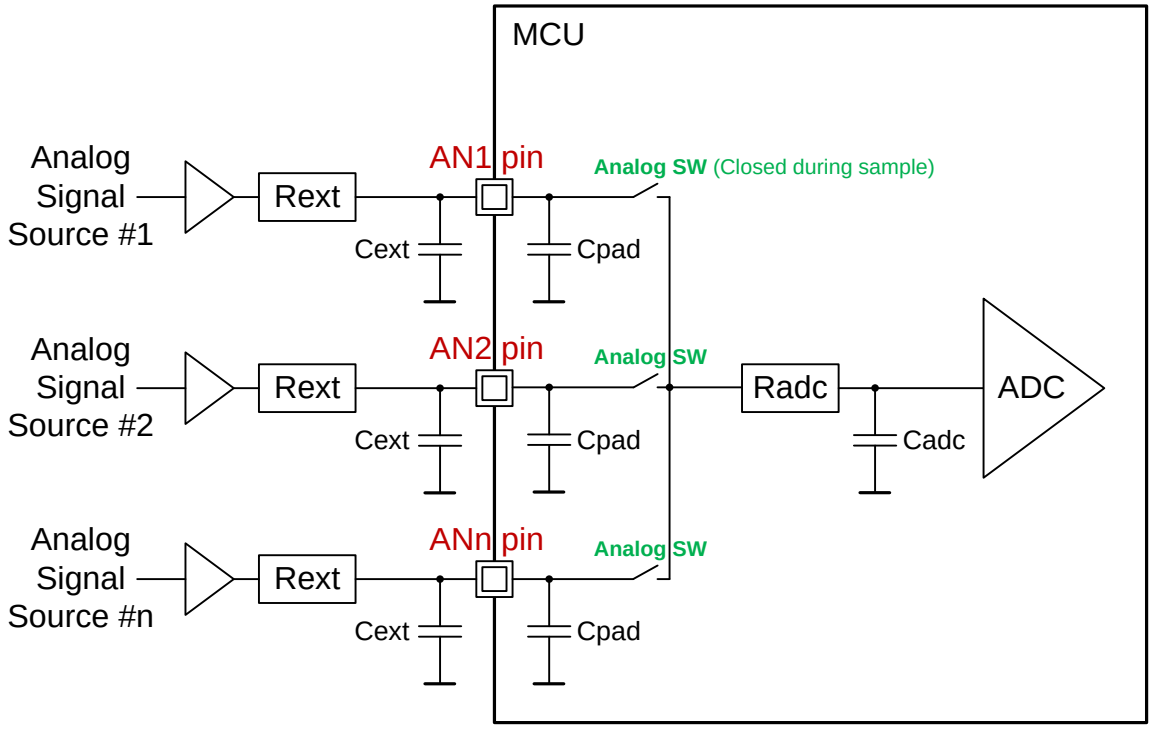


Table 1. Reference Values

Component	Value	AVcc
Cadc	8.30 pF (Max)	4.5 V… 5.5 V
Cadc	8.30 pF (Max)	3 V… 3.6 V
Radc	1.9K (Max)	4.5 V… 5.5 V
Radc	4.3K (Max)	3 V… 3.6 V
Cpin	5pF..15pF	

2.6 Reset Pin (RSTX)

To reset the MCU a switch connects this pin to Vss (Ground). There is internal 50k pull-up resistor, but for high noise requirements an external pull-up resistor with typical 10k is recommended. Additionally, a capacitor has to be connected between Vss and the reset pin for debouncing the switch and for EMI protection. From experience a capacity of not more than 1 nF is recommended. This capacity covers the most common frequency protection in a wide range. Higher capacities and high impedance may cause latch-up effects together with an RSTX-Switch and low EMI protection. The reset level of RSTX pins depends on the logical level on NMIX pin. Please refer to Hardware manual chapter 7 Reset.

Table 2. RSTX and NMIX Function

RSTX	NMIX	Function
1	1	Normal operation
1	0	Non maskable interrupt
0	1	External reset → Reset (RST) → Synchronous reset factor
0	0	Irregular reset → Initialize reset (INIT) → Asynchronous reset factor (not guarantee that memory contents have not been destroyed by the reset)

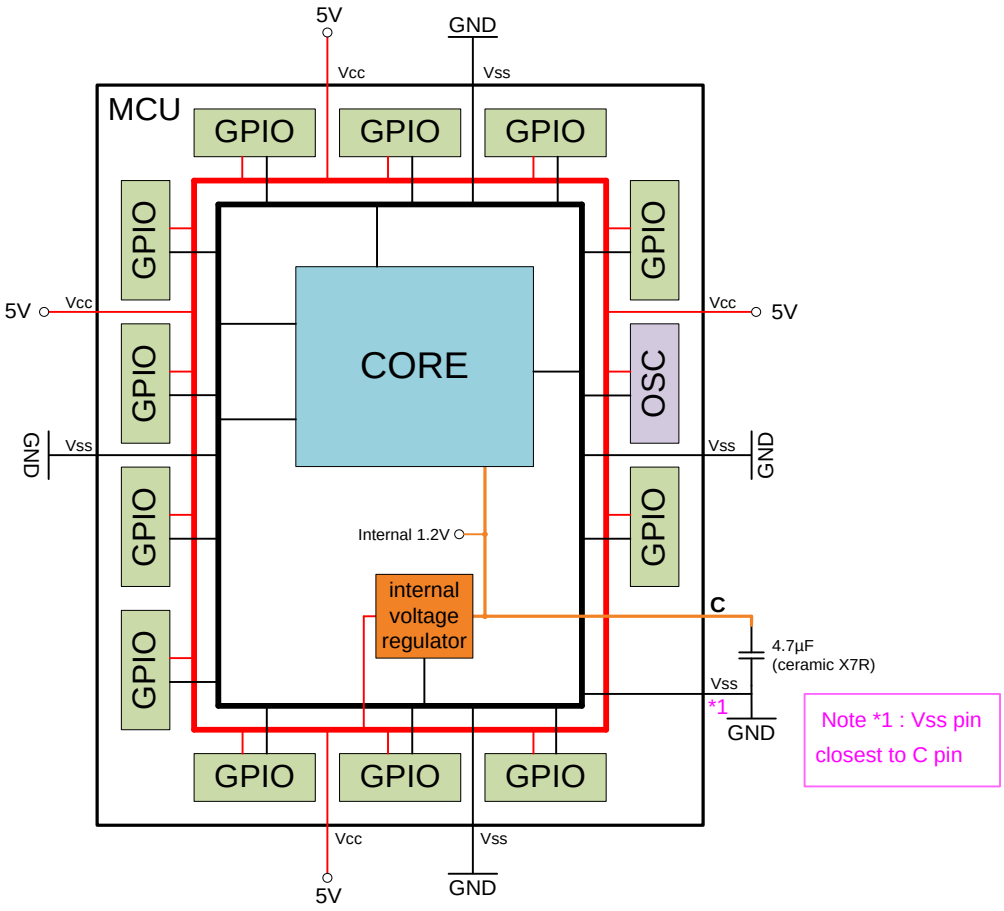
2.7 Non maskable Interrupt Pin (NMIX)

The NMIX supports two several functions, (a) using as NMI input and (b) simultaneous assert of RSTX and NMIX pins to generate an irregular reset. There is internal 50k pull-up resistor, but for high noise requirements an external pull-up resistor with typical 10k is recommended.

2.8 C-Pin

A 4.7 µF ceramic capacitor (dielectric X7R) must be connected very close to the C pin of the MCU. Furthermore, an additional 100 nF (dielectric X7R) for higher noise frequencies is recommended. Otherwise the MCU may not operate correct or will be damaged in worst case. Please refer to Datasheet chapter “Recommended operating conditions” for further information.

Figure 3. Internal Voltage Regulator and C Pin



2.9 Clock Source

A clock source must be provided to the MCU. Therefore, crystals or external clock signals can be used. For external source pin X0 (X0A) is used whereby pin X1 (X1A) is not connected.

There are MCU derivatives for dual clock and single clock devices, the sub clock can be enabled by software. If sub clock X0A pin is neither used as GPIO nor as clock input, the pin can be left open.

If you want to use only CR clock, then you need a MCU version with disabled CSV.

Please also refer to the chapter “Handling the device” in the corresponding hardware manual for details.

2.10 Mode Pins

The mode pins set the current operation mode for the MCU. For a minimal system, only two modes are necessary: Flash-Asynchronous-Serial-Programming-Mode and Run Mode.

In the case, you use the Serial Programming Mode the MD-pins need pull-up/pull-down resistors (typically 2k7 resistors). In order to increase the protection against ESD and EMI effects the PCB tracks should be as short as possible.

If the Serial Programming Mode is not used the MD-pins can be connected directly to Vcc or GND. Please refer to Datasheet chapter “Handling devices” for further information.

The following settings are used for the both modes mentioned above:

Table 3. Mode Pin Settings (x: does not care)

Mode	P006	MD0	MD1
Serial Programming Mode	1	0	1
Run (Internal Vector Mode)	x	1	0

2.11 Not Connected Pins

In default state after power-on reset usually the GPIO pins are in high-z state.

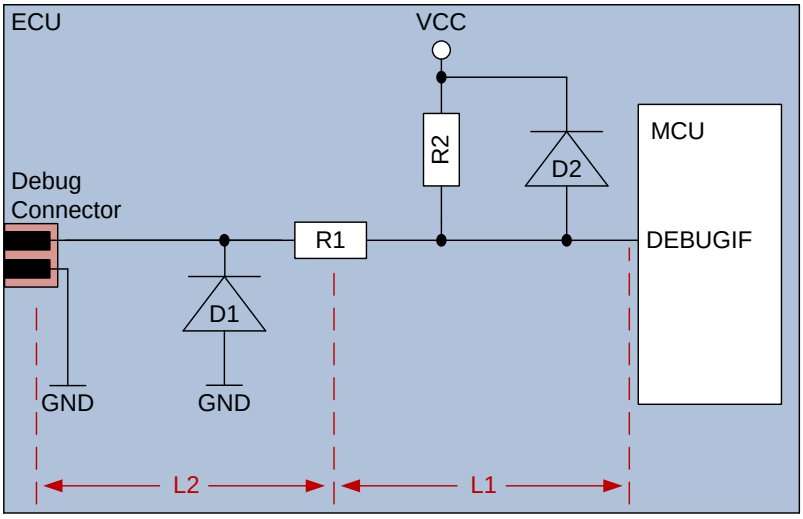
If unused input pins are left open, they may cause a permanent damage to the device due to malfunction or latch-up. Connect at least a 2k resistor to each unused pin in pull-up or pull-down configuration. Also, if I/O pins are not used, they must be set to the output state for releasing or they must be set to the input state and treated in the same way as for the input pins.

Concerning special use cases, it is referred to Port Input / Unused Pins / Latch-up for how to proceed with unused (not connected) pins.

2.12 Debug Interface connection

Debugging is only supported by the 50 Ohm single-wire debug system, which is shared with mode pin ‘DEBUGIF’. Concerning current limitation by an external resistor on programming tool side and maximum clamping current/structure at the ‘DEBUGIF’ pin specified values must be taken out of data sheet.

Figure 4. How to connect Debug System with Programming Connector



(R1 = 43 R, R2 = 10 k, D1 e.g. HZM6.2Z4MFA-E, D2 schottky diode e.g. BAS40, Debug connector: SMA 50R connector for development target boards.)

Table 4. SPEED-BOX General Specifications

Item	Specification
MDI bus maximum communication speed (from MCU to SPEED-BOX)	50 Mbps Does not depend on cable* length. (* cable between SPEED-BOX and ECU)
MDI bus maximum communication speed (from SPEED-BOX to MCU)	Cable* length 2 m or less : 25 Mbps Cable* length 5 m or less : 12.5 Mbps Cable* length 10 m or less : 6.25 Mbps (* cable between SPEED-BOX and ECU)
L1 wiring length	As short as possible, keep less than 5 cm.
L2 wiring length	Less than 15 cm.

Please check for detailed OCDS layout design rules of the MB2100-01-E (see chapter Flash Programming Connection) and the chapter ‘On Chip Debugger: OCD’ of the hardware manual.

3 Layout and Electromagnetic Compatibility

This chapter gives some tips for layout design.

3.1 General

To avoid ESD problems and noise emission of the system some rules for the layout design have to be observed.

The most critical point is the C pin because this is the connection to the internal 1.2 V supply for the MCU core. Thus, two decoupling capacitors have to be placed very near to this pin.

Also, the ground and Vcc routing has to be done carefully. Vcc lines should be routed in star shape. We recommend a Vss ground plane on the mounting side just under the MCU. For both Vcc and Vss only one connection to the rest of the circuit should be done, otherwise noise is carried-over from and to the MCU. This one connection should be used for power supply filtering (PI-Filter with ferrite). Decoupling capacitors (DeCaps) have to be placed as near as possible to the related pins. If they are placed too far away, their functionality becomes useless.

If possible all decoupling capacitors should be placed on the same mounting side as the MCU; otherwise the DeCaps could be placed on bottom layer below the MCU.

PI-Filter prevents EMI from radiating from power supply planes. Keep maximum distance between IN and OUT capacitor to avoid noise coupling at PI-Filter.

If crystals are used, they have to be placed as near as possible to the X1(A) pins, output of the inverter. The feedback resistor of oscillator circuit (typ. 1Mohm) is already implemented internally. The evaluation of crystal/resonator and load capacitor must be tested by the related crystal vendor by crystal matching test.

3.2 Power supply Pins

The following table shows the EMC critical pins and gives short information about how to connect them.

Table 5. Power Supply pins in use

Pin Name	Function
VCC	Dedicated power supply pins for IO buffer and crystal oscillator.
VCC5*	*Only for CY91570/590 series. Dedicated power supply pins for IO buffer and crystal oscillator.
VCC3*	*Only for CY91590 series. Power supply pins for 3V3 IO buffer.
VCCE*	*Only for CY91570 series. Power supply pins for 3V3 IO buffer.
DVCC*, DVSS*	*Only for CY91570/590 series. Power supply pins for high current output buffer pins.
VSS	Dedicated power supply (0 V) pins. (IO buffer, MCU core and crystal oscillator)
AVCCn	Dedicated power supply pins for the AD-converter (unit n).
AVRHn / AVRLn	Dedicated positive/negative reference voltage pin for the AD-converter (unit n).
AVSSn	Dedicated power supply pin (0 V) for the AD-converter (unit n).
C	Dedicated power supply pin for the internal power supply regulator (used to supply the MCU core). External capacitor connected to this pin is required.
C_1*, C_2*, C_3*	*Only for CY91590 series. Dedicated power supply pins for the internal power supply regulator (used to supply the MCU core). External capacitors connected to these pins are required. Please refer to datasheet “C Pin Connection Diagram” reference for further information.

3.3 Oscillator Pins

The following table shows the oscillator pins and gives short information about how to connect them.

Table 6. Oscillator pins in use

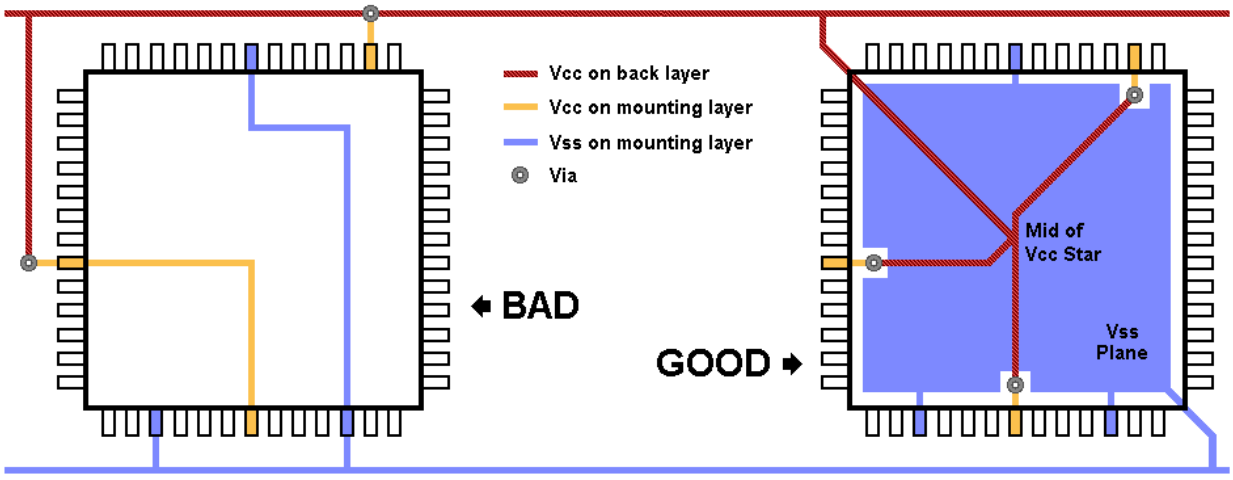
Pin Name	Function
X0, X0A	Oscillator input, if not used so shall be connected with pull-up or pull-down resistor (see please DS)
X1*, X1A*	*Only for devices with subclk. Oscillator output, the crystal and load capacitor must be connected with shortest distance and without any vias. If not used so shall be open

3.4 Power Line Routing

In general, the Vcc and Vss lines should not be routed in “chains”, but in “star shape”. For two layers board the Vss is recommended as ground plane which covers the chip package, and is connected in one point to Vss of the whole circuit to avoid a ground loop.

Below is a principal example of a bad and a good power line routing:

Figure 5. Example of bad vs. good power line routing



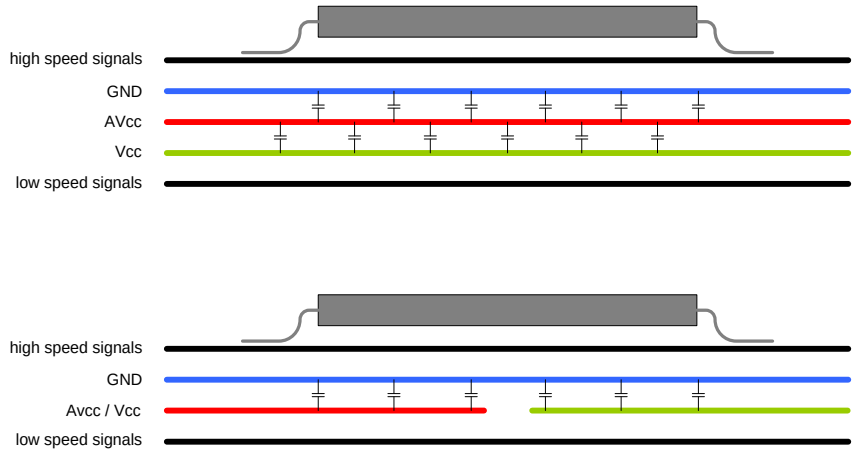
For four and more layers PCB the Vcc and Vss should be routed as a plane in the inner layers of PCB. Concerning the layer stack the several Vdd power supply planes should be not overlapped in parallel layers to avoid noise coupling.

Recommendation for good EMC behaviour:

- Use four layers or six layers PCB
- Use power supply planes (ground and power) in the inner-layer of PCB layer stack
- Reduce the distance between the power planes (low impedance)
- One or two decoupling capacitors close to each VCC pad/pair to adjacent VSS-pad/pair (route under).
- Use capacitor groups to match frequency behaviour of power supply decoupling. The decoupling capacitors can have values between 1 nF and 10 µF.
- Use ferrite filter for each power domain
- Split the used I/O signals in separate layer for low / high speed, and digital / analog signal types

Below is an example for PCB layer stack:

Figure 6. Example of PCB layer stack



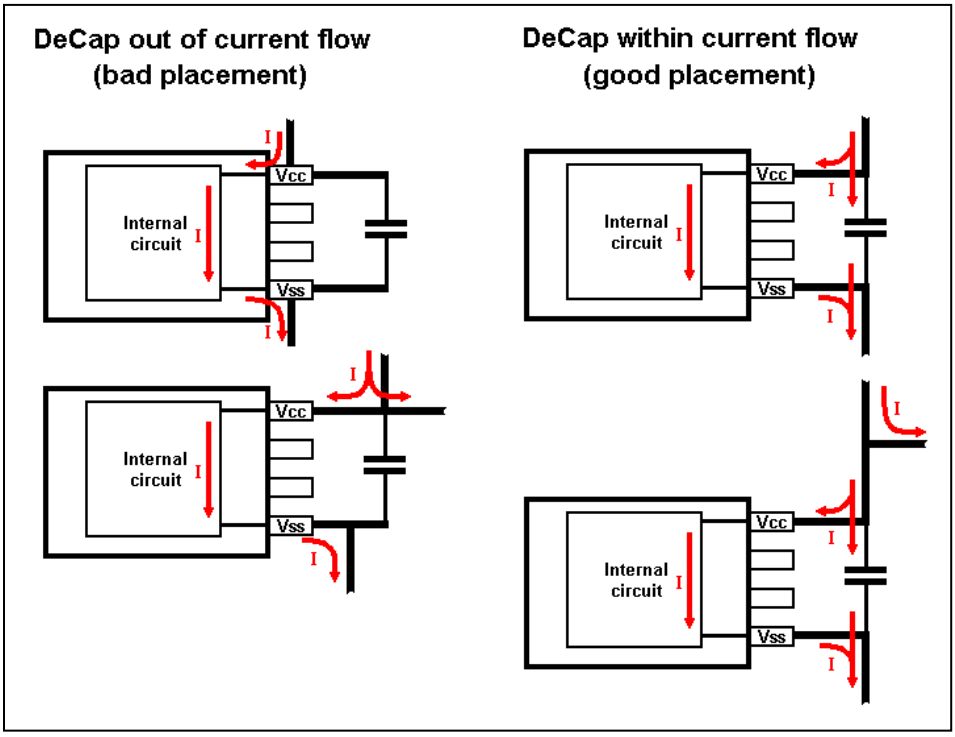
BAD ➔ crosstalk between different power supply planes

GOOD ➔ separation of power supply planes for low EMC requirements

3.5 Power Supply Decoupling

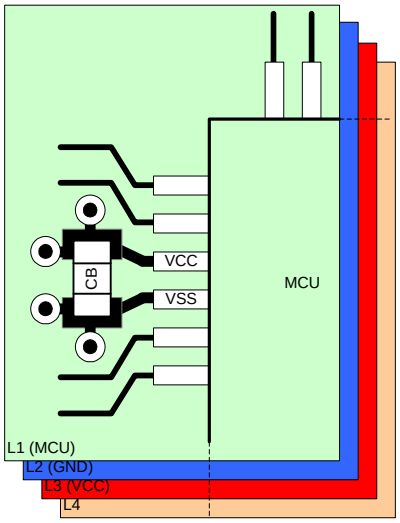
DeCaps for power supply have to be placed within the “current flow”. Otherwise they are senseless, because then their function become inoperable. The following graphic illustrates this:

Figure 7. Power Supply decoupling caps placement



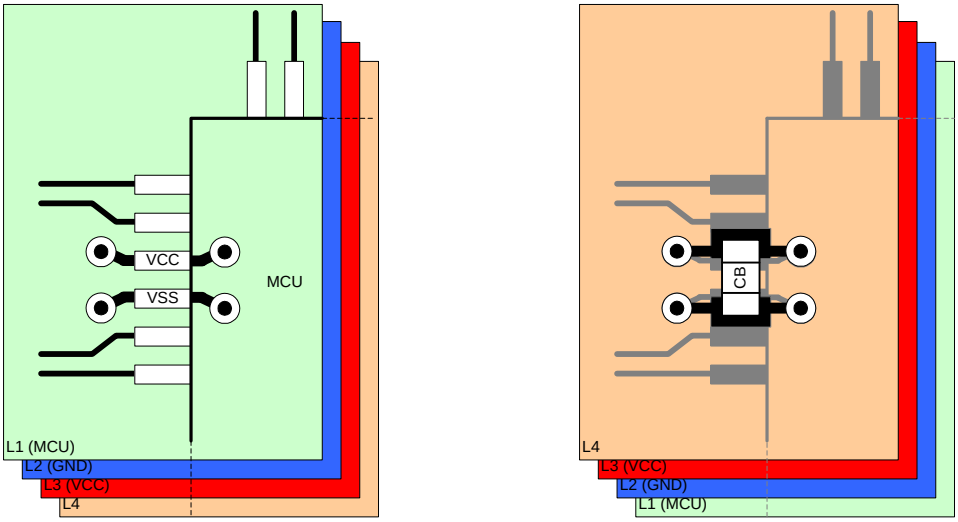
Usually the noise current should flows thought the soldering pad of decoupling capacitor CB. The following routing and placement for single-side assembled boards is recommended:

Figure 8. Power Supply decoupling on single-side assembled boards



The following routing and placement for multi-layer PCB is recommended. Note that despite the capacitor is placed on the opposite side as the MCU, this solution is the best for high-density board assembly.

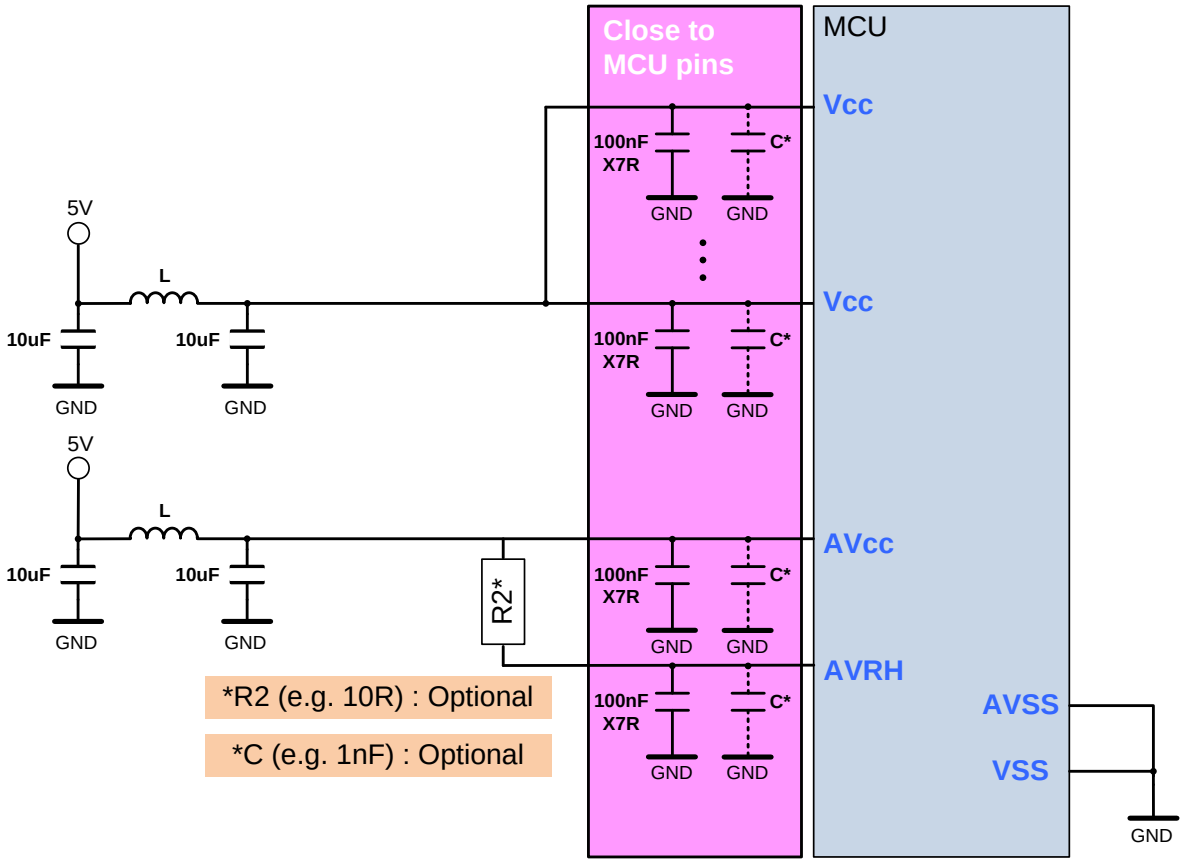
Figure 9. Power Supply decoupling on double-side assembled boards



3.6 Recommended Power Supply Circuit

To meet EMC requirements for the target board, a noiseless supply is necessary. Therefore, the supply should be filtered as shown in Figure 10. Switched IO pins like stepper motor controller or external bus interface can generate spikes on the supplies. These are difficult to filter using capacitors only. A series inductor (ferrite, e.g. WE742792022) is therefore recommended, as shown.

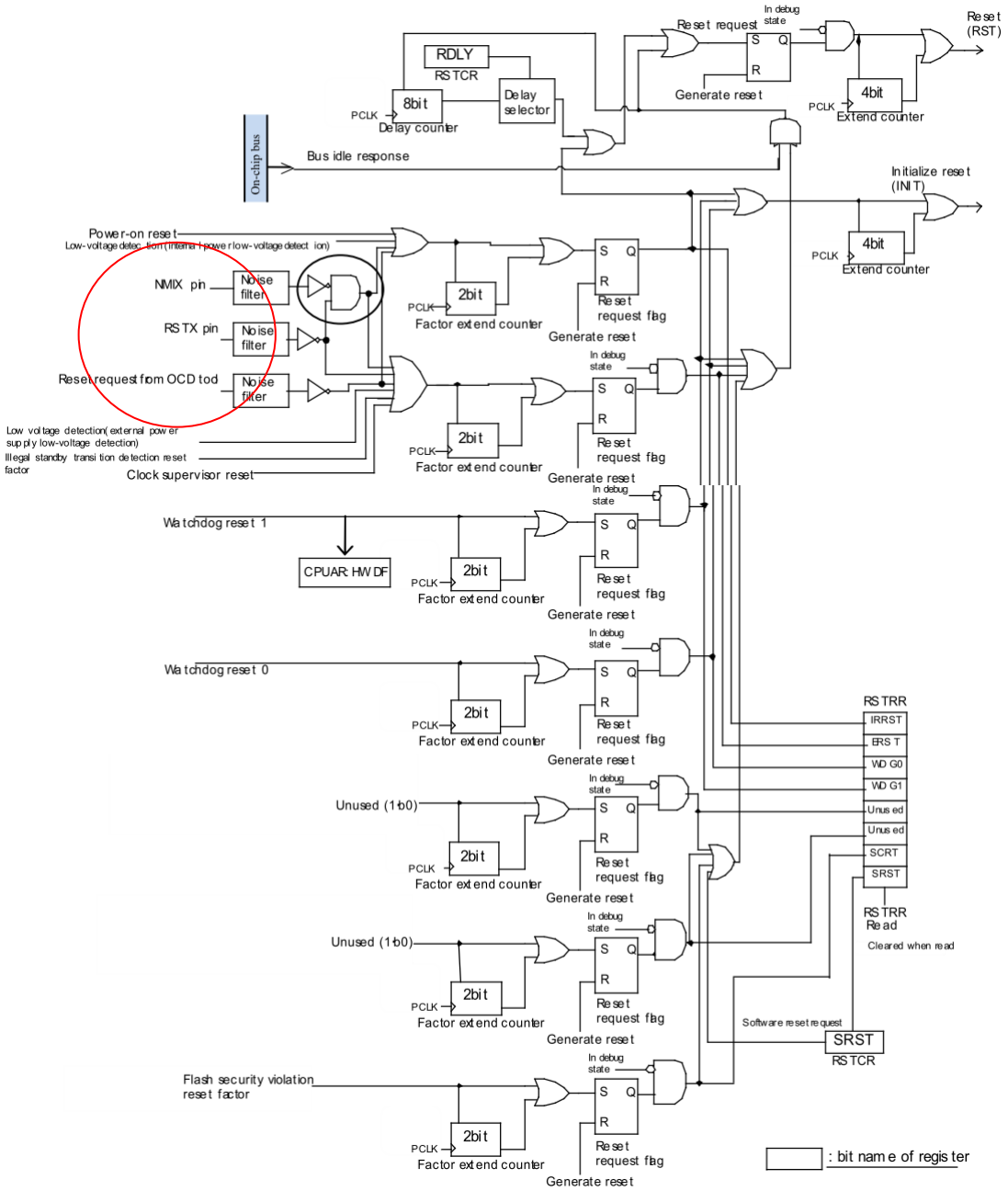
Figure 10. Principal Supply circuit



3.7 Reset circuit

All hard reset events are extended by the hard reset extension circuit to guarantee the stabilization of the Low Voltage Detector (LVD) and complete reset of the device before program execution starts. The reset signal at RSTX pin goes through a noise filter to avoid any spike on the reset input. Please note there are two types of reset level (RST and INIT).

Figure 11. Block Diagram of reset extension circuit



Please see also the datasheet, chapter “External reset timing” of related MCU series.

Table 7. External reset timing

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	RSTX	–	10	–	µs	When normal operation
				Oscillation time of oscillator* +100	–	µs	At Stop mode
				100	–	µs	At Watch mode
Width for reset input removal				1	–	µs	

Figure 12. External reset timing

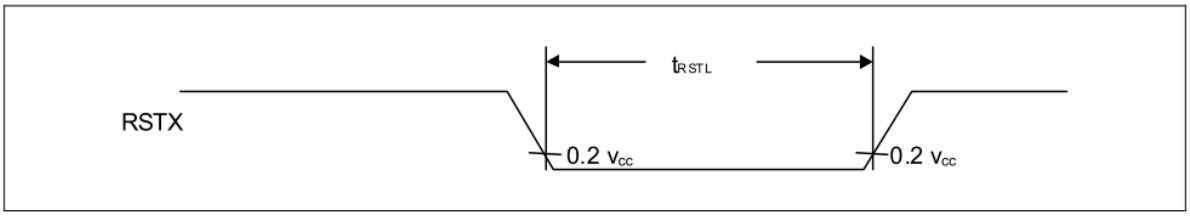
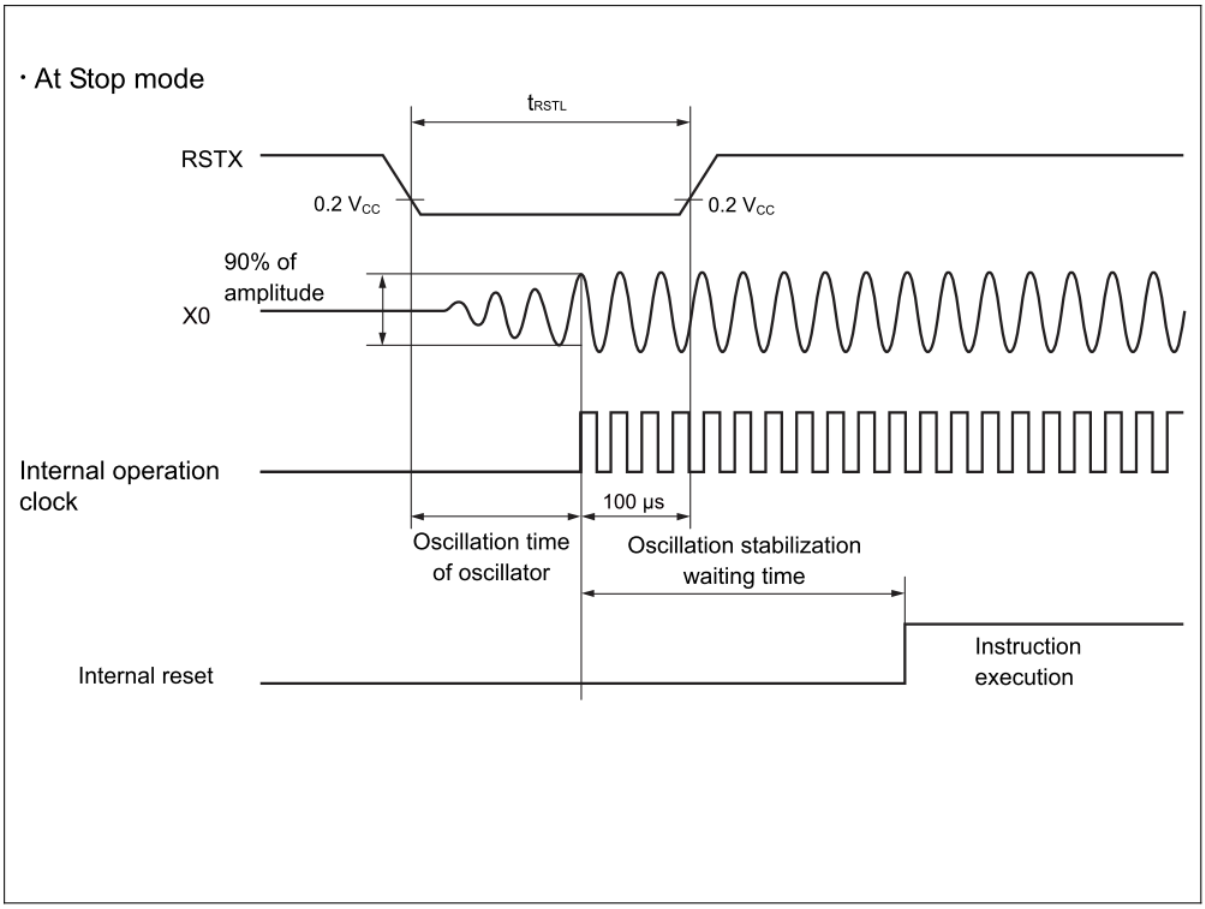


Figure 13. Block Diagram of reset extension circuit



3.8 Quartz Crystal Placement and Signal Routing

The feedback resistor (Rf) of the oscillator circuit is already inside of MCU device. The value of both load capacitors (C1, C2) should be determined with crystal matching test. The crystal matching test must be done by the crystal manufacturer based on the target board. As a result of crystal test maybe will be needed a damping resistor (Rd).

Figure 14. Principal Oscillator Circuit

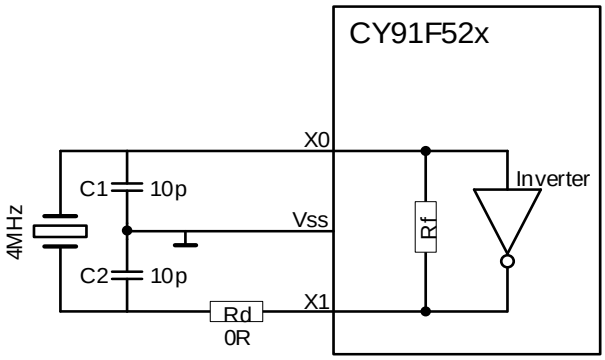
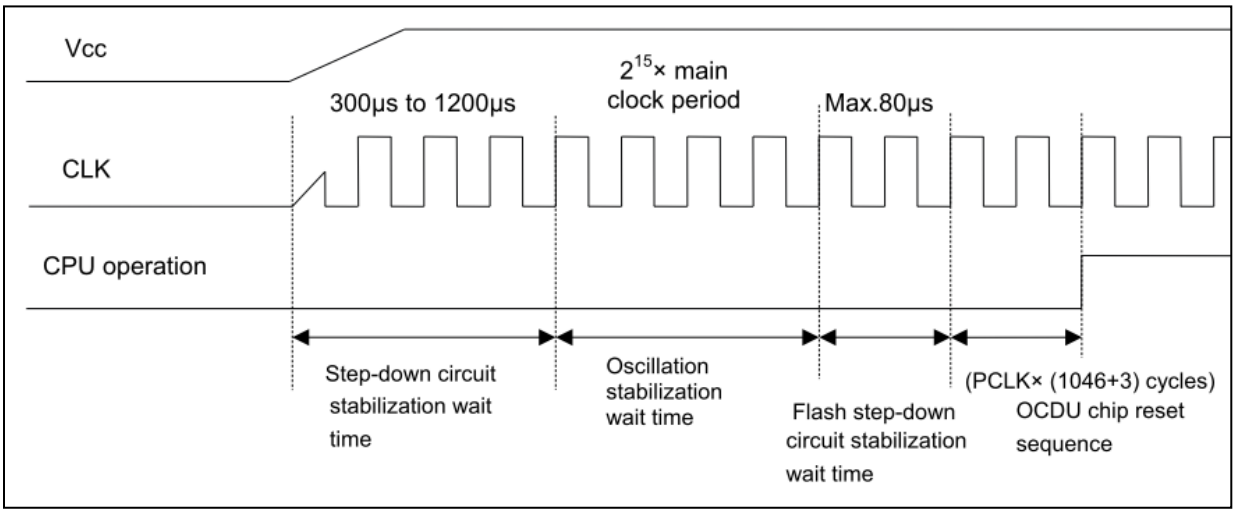


Figure 15. Principal Oscillator Circuit and Startup Sequence



As you can see in Figure 16 the routing of these components is very important in order to reduce EMI effects. These components have to be placed on the same layer as the MCU. The connection of C1 and C2 to the Vss pin must be routed in a star way and so close as possible. The only vias should be placed to connect this ground star routing to the ground plane in other layer, never use vias to connect these components with the corresponding MCU pins.

Figure 16. Layout example for crystal oscillator circuit

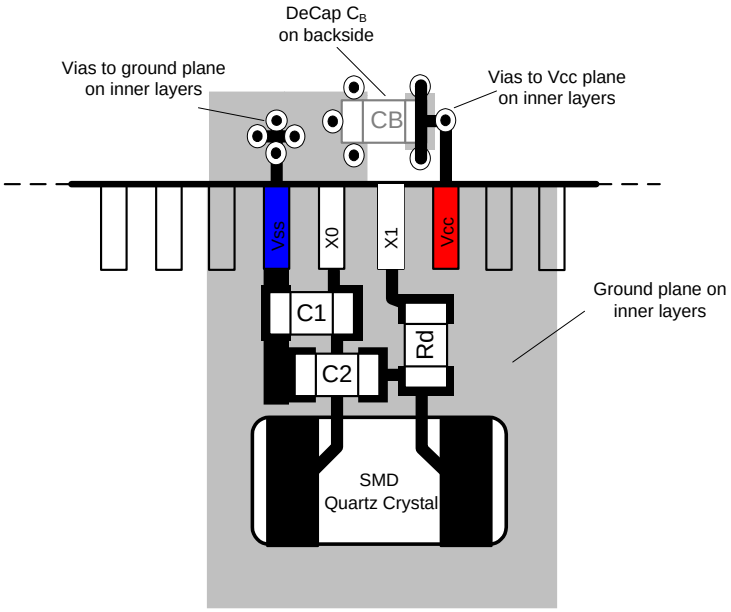
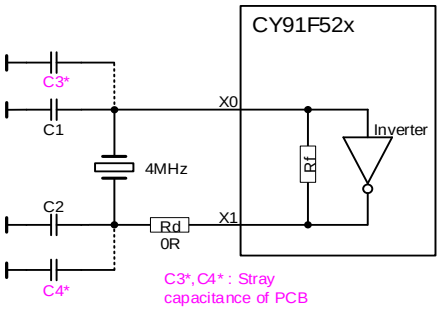


Figure 17. Stray capacitance of PCB



$$C_L = \frac{(C_1 + C_3) \cdot (C_2 + C_4)}{(C_1 + C_3) + (C_2 + C_4)}$$

Equation: C_L calculation with stray capacitance of PCB.

For a proper performance of the oscillator circuit it is necessary to match the load capacitors (C_1, C_2) with the crystal when the MCU, PCB or crystal are replaced for a different one.

As a result of this matching test the value of C_L is provided and then the calculation of C_1 and C_2 can be done using the Equation.

3.9 Test points

The FR81S devices support several clock output functions for failure analysis in development, mass production or in the field. MONCLK out could be used e.g. for clock calibration of main or sub oscillator.

Figure 18. MONCLK internal clock select and prescaler

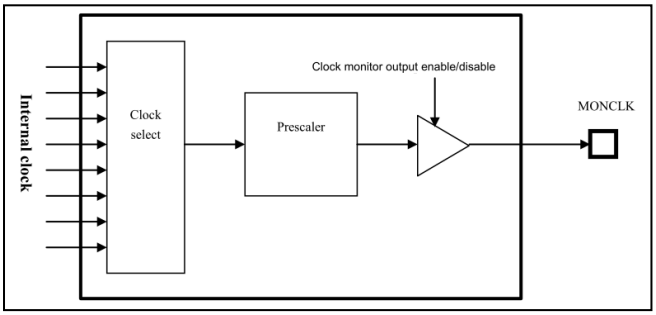


Table 8. Supported output functions for test purposes

CMSEL3	CMSEL2	CMSEL1	CMSEL0	Clock source output to MONCLK pin
0	0	0	0	MONCLK output disabled (high impedance state) (initial value)
0	0	0	1	Main oscillation before CSV input
0	0	1	0	CR oscillation
0	0	1	1	Main oscillation output from CSV
0	1	0	0	Setting Prohibited
0	1	0	1	Setting Prohibited
0	1	1	0	Setting Prohibited
0	1	1	1	Setting Prohibited
1	0	0	0	PLL output
1	0	0	1	SSCG output
1	0	1	0	PLL output after CAN prescaler (CAN system clock)
1	0	1	1	CCLK
1	1	0	0	HCLK
1	1	0	1	PCLK1(Spread peripheral clock)
1	1	1	0	PCLK2 (Peripheral clock after spread/ non spread selection)
1	1	1	1	TCLK

3.10 Other documents

For further detailed information please refer to the application notes on the web page.

4 Port Input / Unused Pins / Latch-up

How to connect input port pins and how to proceed with unused pins

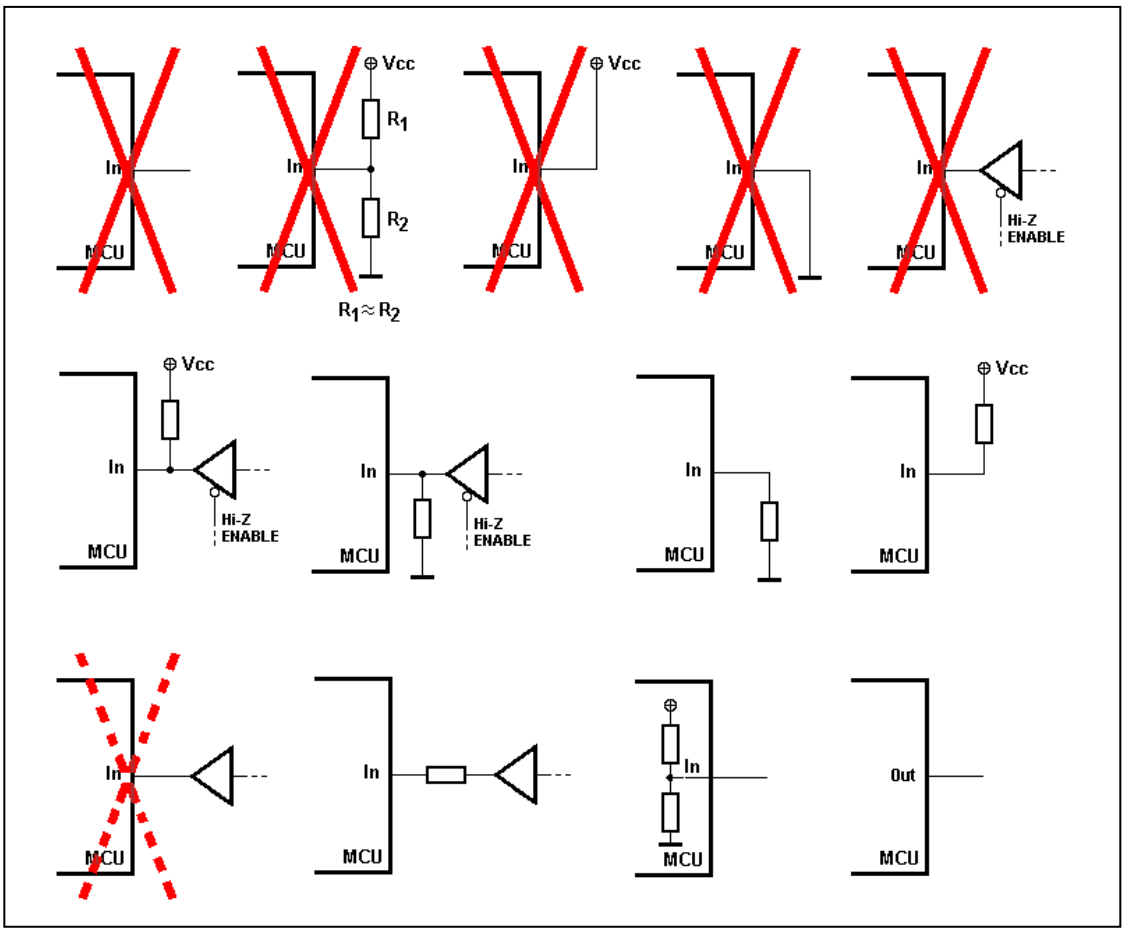
4.1 Port Input / Unused Pins

It is strongly recommended not to leave Input Pins unconnected. In this case those pins can enter a so-called floating state. This can cause a high ICC current, which is adverse to low power modes. Also damage of the MCU can happen.

Use the internal pull-up/down resistors, if the port provides such function. If not, use external pull-up or pull-down resistors to define the input-level. If both solutions are not possible, set the Port Pin to Output.

Never connect a potential divider with almost same resistor values.

Figure 19. Principle using of input circuit to avoid latch-up or leak current



Be careful with connection of input pins to other devices, which can go into High-Z states. Always use pull-up or pull-down resistors in this case.

Outputs from external circuits should always be connected via a serial resistor to a MCU input pin.

Debouncing and decoupling capacitors should always be chosen as smallest as possible. Please refer to Latch-up consideration (switch).

All pins are set to input Hi-Z after its power-on default. Therefore set unused pins to input with internal pull-up/down resistor, or provide them with pull-up or pull-down resistors.

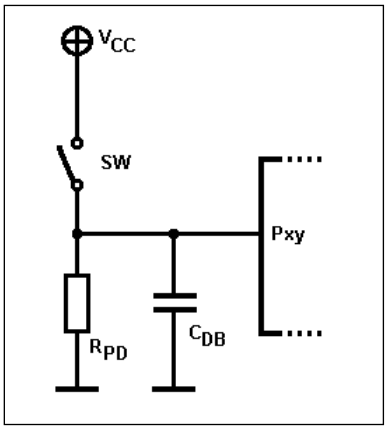
Do not connect any input ports directly to VCC or VSS (GND)! Always use pull up or down resistors (2k … 10k Ohms). If available, it is possible to use the internal pull up or pull down resistors as well. Please note the value internal resistors can be 20k … 100k depends on the device and temperature.

4.2 Latch-up consideration (switch)

Be careful with external switches to VCC or ground together with debouncing capacitors connected to port pins.

A usual configuration is shown in the following schematic:

Figure 20. Usual Configuration Switch

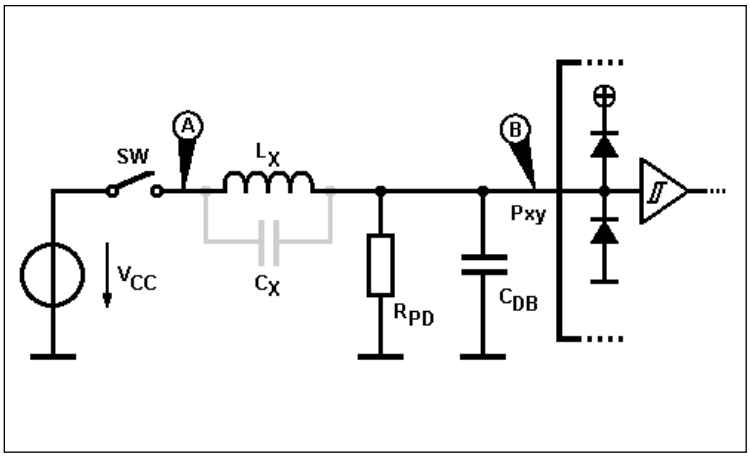


R_{PD} is a pull-down resistor and CBD a debouncing capacitor. If the switch SW is open, a “0” is read from the port pin Pxy. If the switch is closed the input changes to “1”.

From the physical aspect, it has to be considered, that the switch is often placed in distance to the MCU by cable, wire, or circuit path. The longer the circuit path is the higher will be its inductivity LX (and capacity CX).

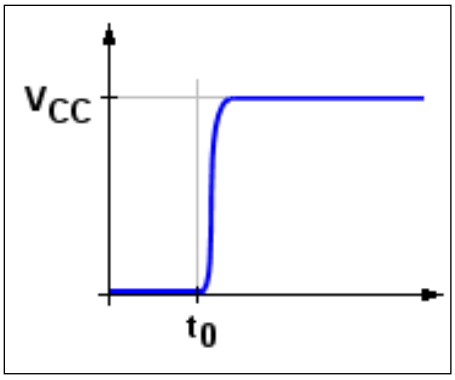
An equivalent circuit diagram looks like the following illustration:

Figure 21. Usual Configuration Switch, equivalent circuit



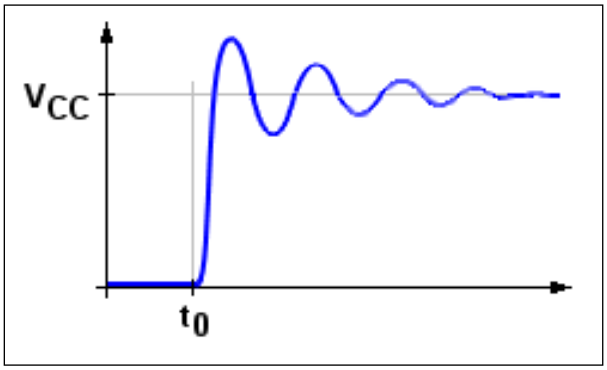
By closing the switch SW at time t_0 the following voltage can be measured at point (A):

Figure 22. Signal rise on switch closing (Point A)



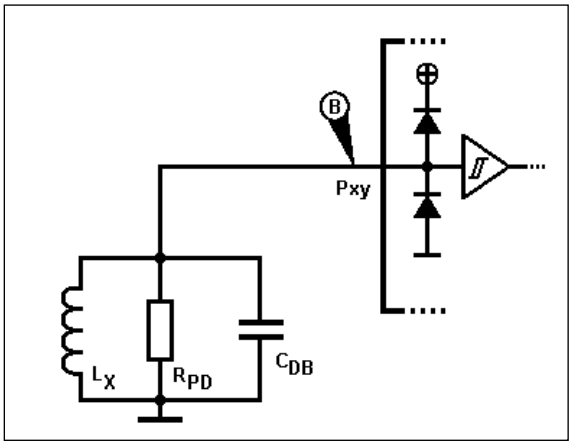
But at the port pin Pxy on point (B) the following voltage can be measured:

Figure 23. Signal rise on switch closing (Point B)



By closing the switch SW the circuit becomes a parallel oscillator with the wire-inductivity LX, the debouncing capacity C_X and the damping RPD of the pull-down resistor (Assume the power supply to be ideal, i.e. it has no internal resistance):

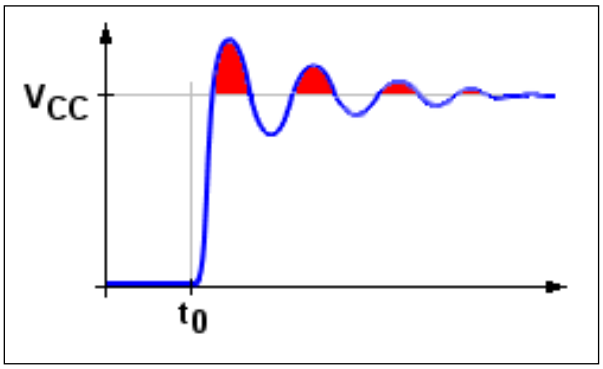
Figure 24. Equivalent circuit on switch closed



Because RPD is often chosen high (> 50 KOhms), its damping effect is weak.

This (weakly) attenuated oscillator causes voltage overshoots on the port pin, drawn in red in the illustration below:

Figure 25. Signal on the pin



These overshoots may cause an internal latch-up on the port pin, because the internal clamping diode connected to VDD becomes conductive. Similar is the effect, if the switch SW is opened. In this case there are under shoots on the port pin.

The frequency of the oscillation can be calculated by

Equation: Oscillation frequency

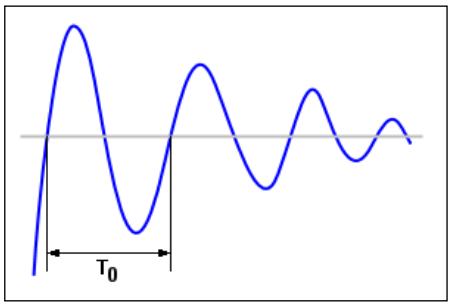
$$f_{OSC} = \frac{1}{2\pi\sqrt{L_X C_{DB}}}$$

The inductivity LX is the unknown value and depends on the PCB, its routing, and the wire lengths.

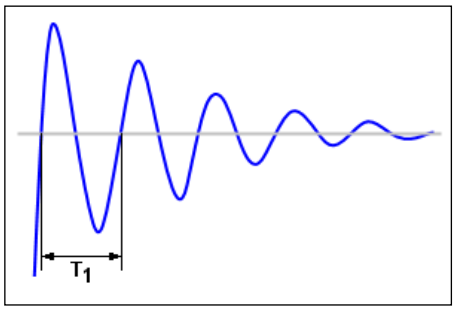
There are two counter measurements to prevent from latch-up.

One solution is to decrease the capacity of the debouncing capacitor. This increases the oscillation frequency, and the over-all energy of the overshoots is smaller.

Figure 26. Signal on the pin with large and small capacities



(a) Signal on the pin with a large capacity.

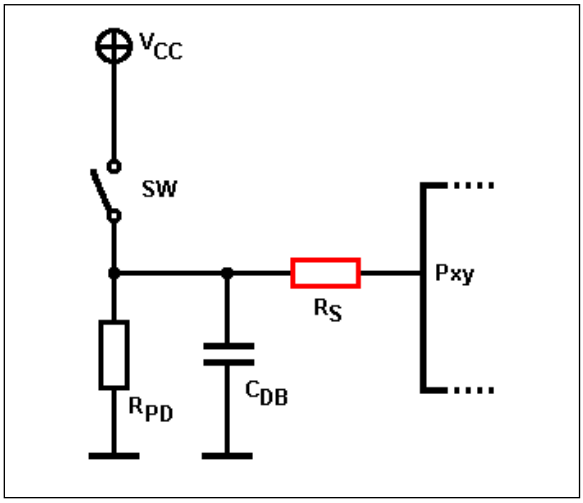


(b) Signal on the pin with a small capacity

This solution has two disadvantages: First the debouncing effect decreases and second, there is no guarantee, that the latch-up condition is eliminated.

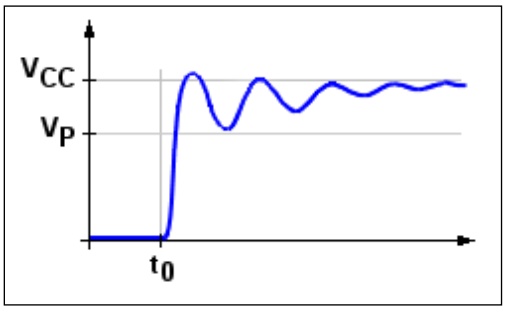
A better solution is to use a series resistor at the port pin like in the following schematic:

Figure 27. Series resistor



The series resistor RS reduces the amplitude of the oscillation and decreases the voltage offset at first. The resistor must not be chosen too high, so that the port pin input voltage VP is within the positive CMOS/TTL/Automotive level.

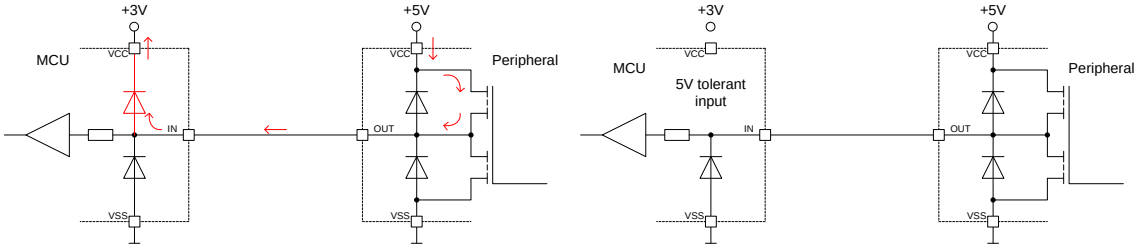
Figure 28. Reduction of the signal on the pin due to the series resistor



4.3 5 V Tolerant Input pins

In case of using of MCU on 3 V level and peripherals on 5 V level of power supply the ESD please note the influence of ESD clamping structure of usual GPIO pin.

Figure 29. Standard IO and 5 V Tolerant IO



(a) Standard IO (b) 5 V Tolerant IO

For 5 V Tolerant IO, the diode is not attached to the Pch side. It is a protection circuit in the parasitic bipolar and the diode to VSS. For the reason, clamp current cannot be specified in the DS for such kind of input pins. 5 V tolerant inputs are e.g. for CY91F52x: P035, P041, P093, P122. Please see also the note *6 in the DS “ELECTRICAL CHARACTERISTICS – Maximum clamp current”. The current limitation with series resistor for + B signal is input is not possible for a 5 V tolerant input.

5 Flash Programming Connection

This chapter shows which connections are needed for programming.

5.1 Overview

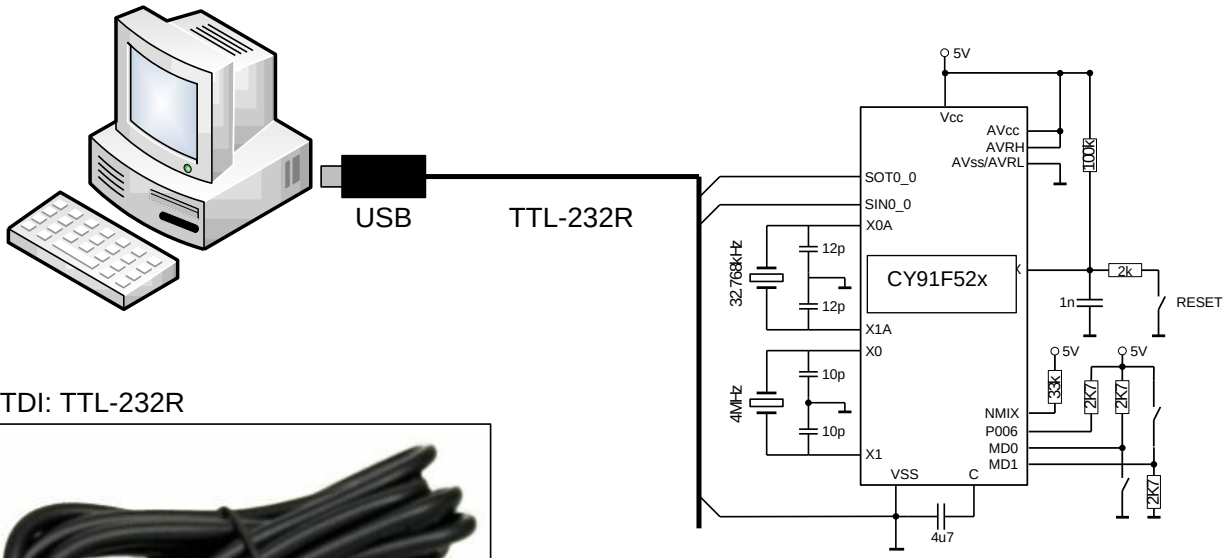
There are three different ways of programming the internal flash memory of this series.

- Serial programming via Uart0
- Serial programming via MDI interface
- Parallel programming interface.

5.2 Serial programming via UART0

In order to program the internal memory flash of the MCU via Uart0, the only needed part is a cable to connect the PC with the MCU Usart0 module, to achieve that nowadays you can do it in different ways; using a regular serial cable if a DB9 serial connector is present in the computer or using a more modern USB cable (i.e. FTDI: TTL-232R http://www.ftdichip.com/Products/Cables/USBTTLSerial.htm). With the USB cable the achieved baud rate is higher due to the higher speed of USB communication.

Figure 30. Principal Schematic for serial programming via Usart0 (with USB Cable)

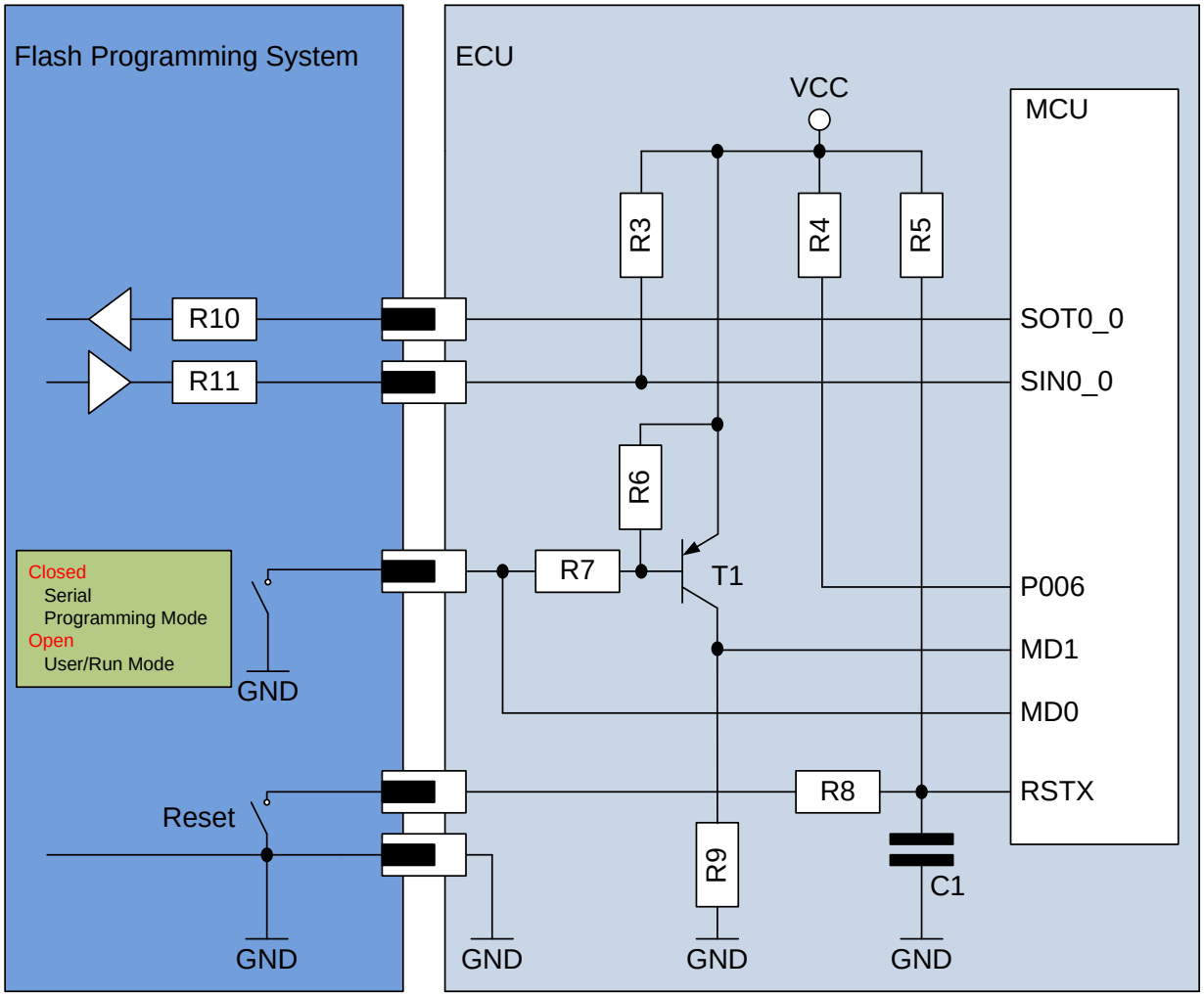


FTDI: TTL-232R

To enable the serial programming using this method, you have to configure the Mode pins in an appropriate way (see Figure 30) according to the Table 3.

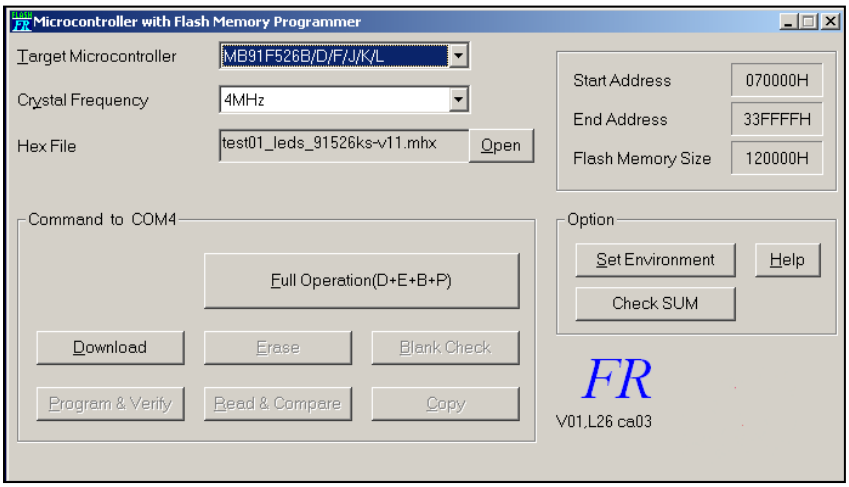
The setting of the Mode pins can be done automatically by the programming system as you can see in the Figure 31, using only one signal connected to pin MD0, inverting MD1 and a pull-up resistor on the pin P006.

Figure 31. Principal Schematic for serial programming via Usart0



The software used for flash programming of this MCU series is FR Cypress Serial Programmer tool. You can see a snapshot in the Figure 32.

Figure 32. Snapshot of the FR program used for flash programming via Usart0



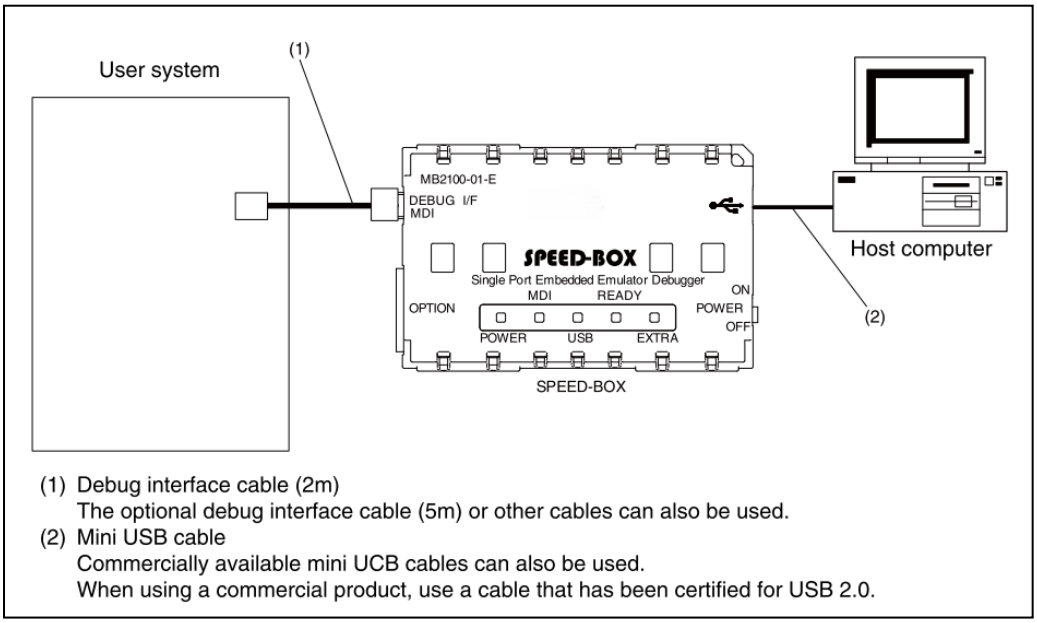
5.3 Serial programming via MDI interface

A suitable way of programming and debugging is the MDI interface using only one signal (pin Debug I/F) through the MB2100-01-E debugger.

The MB2100-01-E debugger is connected to the host computer with an USB cable and to the target PCB with a single wire coaxial.

OCDU is the device built-in debug support unit that provides the on-chip debug function in FR81. OCDU provides the basic debugger functions (CPU execution/break control, CPU register/memory/IO access), small-scale debug support functions (event, execution time measurement, trace, etc.), and security function.

Figure 33. Connection of the MB2100-01-E with the host computer and target board



(1) Debug interface cable (2m)
The optional debug interface cable (5m) or other cables can also be used.
(2) Mini USB cable
Commercially available mini UCB cables can also be used.
When using a commercial product, use a cable that has been certified for USB 2.0.

Figure 34. Picture of the MB2100-01-E

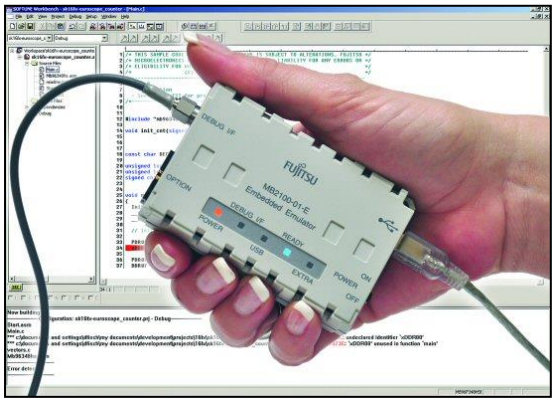
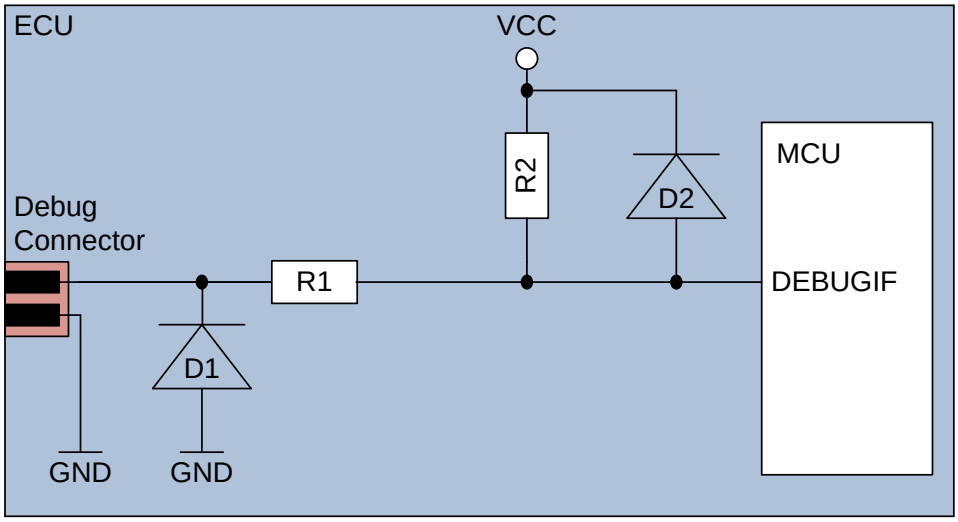


Figure 35. Electronic Components needed to protect the Debug I/F pin



(R1 = 43 R, R2 = 10 k, D1 e.g. HZM6.2Z4MFA-E, D2 Schottky diode e.g. BAS40, Debug connector: SMA 50R connector for development target boards.)

5.4 Parallel programming interface

In case of using Flash security and unknown key or if the OCD interface function is disabled, the Flash may be erased only by the parallel programming mode. The parallel programming is supported by GALEP-5D:

Figure 36. Parallel programming with GALEP-5D

Further information about GALEP-5D can be found on the web page:

http://www.conitec.net/english/galep5d.php

5.5 Security function

This MCU series has a security function to impede improper access to the internal flash. To enable this function, the user has to write in a specific flash memory location a password and a flash security code. From then security is turned on and access restrictions are imposed on subsequent accesses to flash memory.

Once security has been turned on, the security is not turned off unless the entire flash memory area is erased (using serial or parallel programming method).

To avoid not authorized access to memory during debugging the user is forced to enter the same password previously written in flash memory. Once authentication by password of on-chip debugger (OCD) is completed, you can read the content of flash memory from external by using OCD.

The debug security area is allocated at 30 bytes of built-in flash start address +4 to +33. (For further information please go to the Hardware Manual of this series)

6 Reset Behavior of IO port pins

This chapter shows the behavior of IO-Port during and after RESET

During the power-on or RSTX reset state the GPIO port pins are going to HiZ and the inputs are disabled to prevent the leakage by any floating pin. After release of reset the IO-ports will be set to initial value (see also related DS of FR81S series)

Table 9. Power-On/RSTX reset state GPIO initial state

Pin	Function	Initial state
X0/X1	Main oscillator	Running
X0A/X1A	Sub oscillator	Running
Gpio port pins	GPIO	Input disabled HiZ

If some external bus pins should be used as GPIO than do not use any address or bus control lines as input, because these lines are driven as output high.

7 Additional Information

Information about CYPRESS Microcontrollers can be found on the following Internet page:

http://www.cypress.com/cypress-microcontrollers

Related documents for further information are listed in the table below:

Table 10. Related Documents

Ref. #	Document file name	Description
1	CY91520 Series 32-Bit Microcontroller FR Family FR81S Hardware Manual	FR81S CY91520 Series Hardware Manual
2	CY91520 Series 32-Bit FR81S Microcontroller	FR Family FR81S, CY91520 Series datasheet
3	CY91590 Series FR81S Hardware Manual	FR81S CY91590 Series Hardware Manual
4	CY91590 Series FR Family FR81S 32-Bit Microcontroller	FR Family FR81S, CY91590 Series datasheet

Document History

Document Title: AN209375 - Recommendation for Hardware Setup 32-Bit FR81S Family

Document Number: 002-09375

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	-	-	Initial release
			-	RSTX and NMIX input section: correction RSTX and NMIX input
			-	obsolete issue removed
			-	Added new section: 5V-tolerant IOs
			01/06/2014	V1.3: FTo
			02/11/2015	V1.4: FTo Modified Figure 1: Principle schematic for minimal requirements and Figure 30: Principle schematic for serial programming via Usart0 (with USB cable)
*A	6095053	NOFL	03/12/2018	Updated to Cypress template. Completing Sunset Review.
*B	6523608	NOFL	03/27/2019	Replaced “MB” with “CY” in all instances across the document. Completing Sunset Review.

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