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FR Family, 32-bit Microcontroller, MB91F313 HDMI-CEC

This document describes the usage of HDMI-CEC technology used with MB91F313, which begins being adopted in TV and AV devices. Up to now, analog signals have been used to send pictures and voices on signal lines to connect TVs and HD recorders. Generally, cables of the RCA terminal, S terminal, and D terminal have been used for picture transmission and cables of the RCA terminal for voice transmission. Since the analog signals to send pictures and voices are continuous voltage values, there has been the problem that they are subject to noise influences from the outside and inside. To solve the problem, HDMI technology has been developed for home-use electric apparatuses by arranging the personal computer's DVI standard already supporting the digital video signal. In HDMI technology, a single cable can transfer pictures, voices, and device information.

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1 Introduction

This document describes the usage of HDMI-CEC technology used with MB91F313, which begins being adopted in TV and AV devices. Up to now, analog signals have been used to send pictures and voices on signal lines to connect TVs and HD recorders. Generally, cables of the RCA terminal, S terminal, and D terminal have been used for picture transmission and cables of the RCA terminal for voice transmission. Since the analog signals to send pictures and voices are continuous voltage values, there has been the problem that they are subject to noise influences from the outside and inside. To solve the problem, HDMI technology has been developed for home-use electric apparatuses by arranging the personal computer's DVI standard already supporting the digital video signal. In HDMI technology, a single cable can transfer pictures, voices, and device information.

CEC is one function of the HDMI for device control, which has been defined in HDMI ver1.2a and was established in December, 2005. The function controls the relationship among each device mutually; for example, operation for multiple digital apparatuses can be integrated into one remote controller.

This document is written for the purpose of smooth introduction of CEC function when using MB91F313. Note that this document is based on High-Definition Multimedia Interface Specification Version. 1.3a.

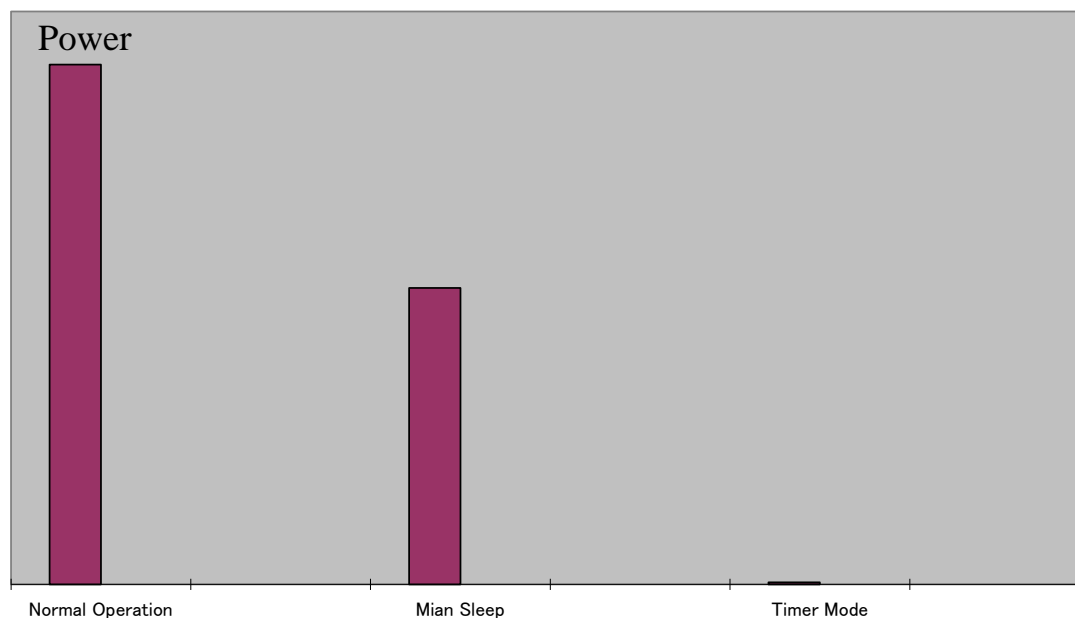
*HDMI, HDMI logo, and High-Definition Multimedia Interface are trademarks and registered trademark of HDMI Licensing LLC.

2 Outline of MB91F313

MB91F313 has the HDMI-CEC reception function, allowing its hardware to receive CEC data without software intervention. Although data reception through software requires the pulse width measuring function such as PWC to process each bit, this function can make batch processing as one set of data since it can receive data in parallel, resulting in reduced loads of software processing.

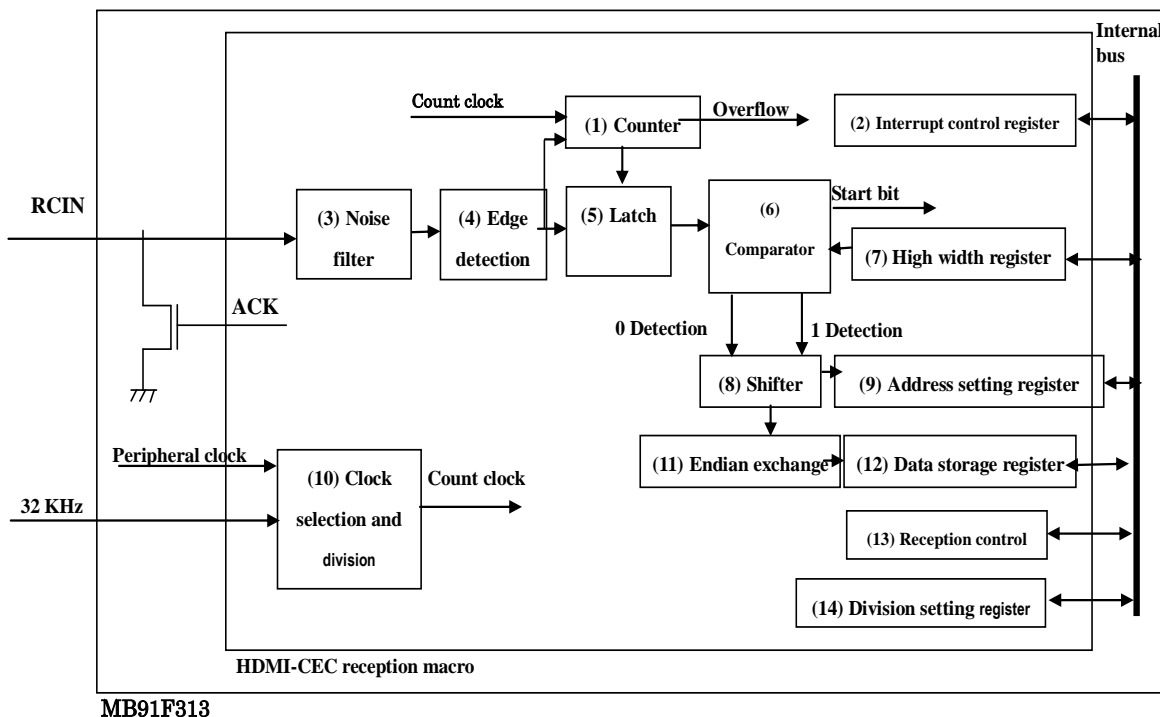
Sub-clock can be input to the HDMI-CEC reception circuit from the external. So, this sub-clock is entered regardless of the clock of CPU or peripheral function and the HDMI-CEC reception circuit can continuously operate even in the timer mode that stops the main clock. Therefore, MB91F313 should receive the sub-clock. In addition, if a transmission destination address is set to the address setting register, an interrupt can occur only when MB91F313 receives a specified transmission destination address, which can greatly reduce power consumption in CEC reception standby state. For the specifications of power consumption, see the datasheet.

	Normal operation	Main sleep	Timer mode
CPU	Operates	Stops	Stops
Peripheral function	Operates	Operates	Stops
HDMI-CEC function	Operates	Operates	Operates
Main clock	Oscillates	Oscillates	Stops
Sub-clock	Oscillates	Oscillates	Oscillates



3 Outline of reception function HDMI-CEC mounted on MB91F313

HDMI-CEC reception function should be used only for reception. This macro has the circuit configuration below, which detects Low width between falling edge and rising edge, compares it with the setting value, and judges 0/1 of the received data. The hardware automatically compares the received address with the specified address, and if the addresses match, then the hardware sets the received data in the data storage register.



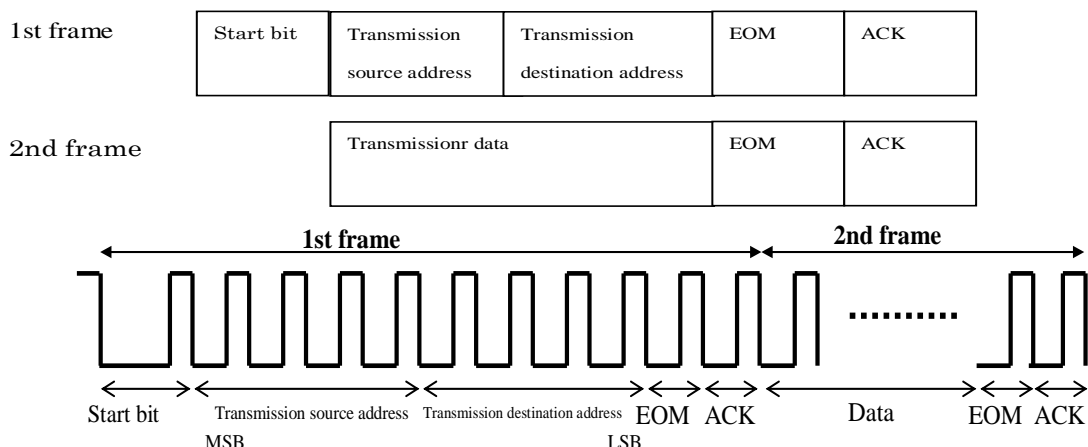
3.1 Operation of HDMI-CEC reception

The signal entered from RCIN pin passes through the noise filter (3) in which noise is removed, and goes into the edge detection circuit (4). Rising and falling signals are entered into the counter (1) and the latch circuit (5). The counter (1) into which the clock selected by the clock selection and division circuit (10) enters, generates the overflow signal if it counts the 128 clock or the 256 clock. The signal entered from the latch circuit (5) into the comparator (6) is compared with the High width register (7). The High width register (7) has the time being set to detect the start bit, data "1", and data "0". The signal is judged by comparing with this time period. The signal generated from the comparator (6) goes into the shifter (8) and when 8-bit data are stored, they are compared with the address setting register (9). If they match, the interrupt should occur. The signal from the comparator above is also entered into the Endian-exchange circuit (11) and stored in the data storage register (12).

4 Input waveform into HDMI-CEC reception function

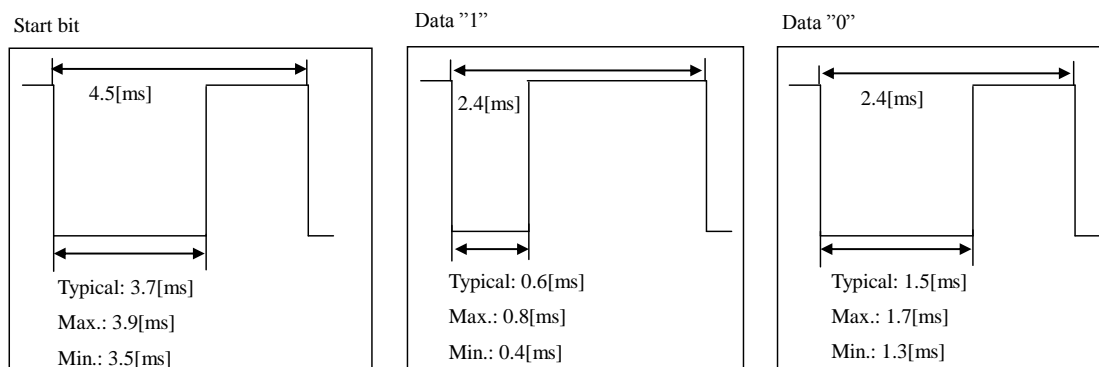
4.1 HDMI-CEC format and its reception operation

CEC communication formats are roughly classified into the format for transmission start and format for reception. The 1st frame consists of the start bit, transmission source address, transmission destination address, EOM, and ACK and the 2nd frame consists of the transmission data, EOM, and ACK.

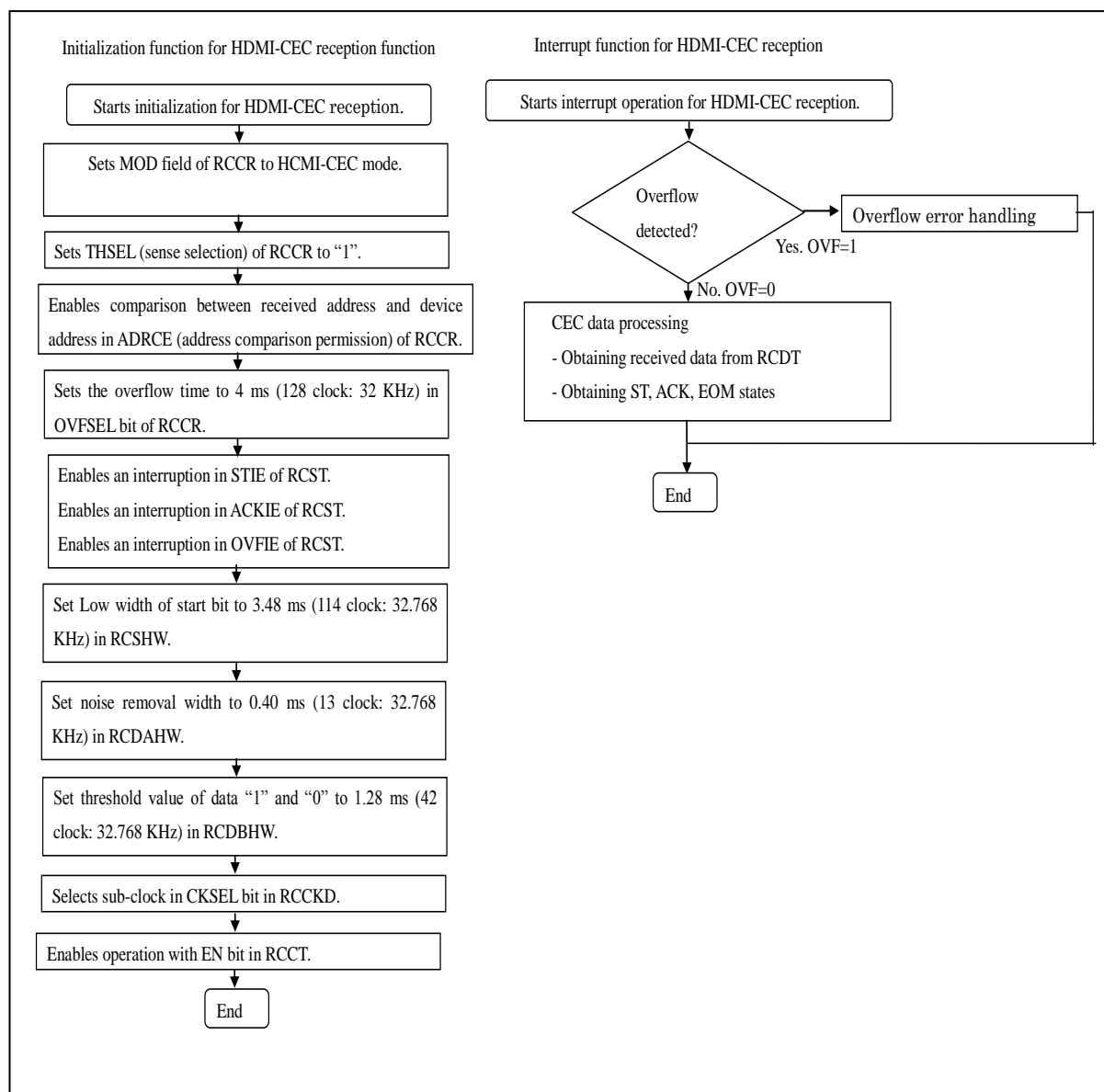


For data transmission, the format of the 1st frame is used to send the transmission source address and the transmission destination address and then the format of the 2nd frame is used to send arbitrary number of data set. Since HDMI-CEC reception function can detect the transmission destination address in the 1st frame, the device address setting register can be used so that it cannot be restored when it receives other than a specified value in it. Data of the 1st frame, the 2nd frame and later is stored as 8-bit parallel data in the data storage register. If overflow occurs after detecting the start bit, the counter overflow detection bit can be set to generate an interrupt. If the received data is normal, the reception side should return ACK for each frame to the source side. In addition, since the source uses EOM to notify the destination of the end of the data, EOM detection bit is used for confirmation.

"1" and "0" of the start bit can be identified by using Low/High width of the pulse. Its cycle should be set by the start bit High width setting register, High width setting register A, and High width setting register B. In HDMI-CEC mode, since the input signal is inverted internally, High width comparison is applied to Low width. A value (ex. 3.48 ms) below the minimum value of 3.5 ms for the start bit Low width should be set in the start bit High width register. Since High width setting register A functions as a noise filter, a value (ex. 0.397 ms) below the minimum value of 0.4 ms for data "1" Low width should be set in the register A. Since High width setting register B is used for the threshold value for data "0" and "1", a value (ex. 0.128 ms) above 0.8 ms and below 1.3 ms should be set in the register B.



5 Example of initialization flow of HDMI-CEC reception function

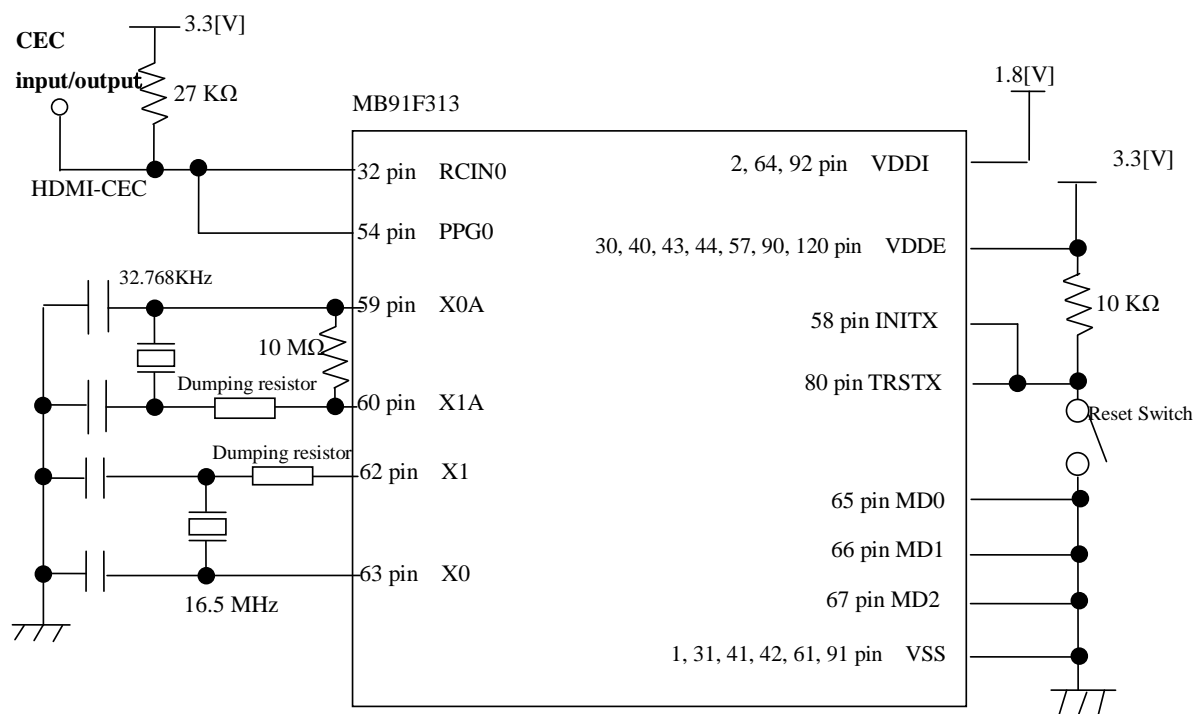


6 Example of HDMI-CEC circuit in MB91F313

6.1 Configuration

HDMI-CEC reception function is used to receive CEC commands. In addition, PPG output having N-ch open/drain function is used to send CEC commands. As shown in the simple circuit example below, CEC input pins connect to CEC signal lines.

6.2 Example of simple MB91F313 circuit



* Select the dumping resistors and the capacitors for the oscillator based on the matching data of the used oscillator.

The matching data is available from the manufacturer of the oscillator

* An additional circuit should be required for on-board debugging and on-board flash writing.

Document History

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Document Number: 002-06371

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	YUIS	03/07/2008	Initial release
*A	5293547	YUIS	06/02/2016	Migrated Spansion Application Note “AN07-00154-1E” to Cypress format.
*B	5876138	AESATMP8	09/07/2017	Updated logo and Copyright.

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