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AN205996

Example of System Configuration And Setup for Three-Phase Motor Control

Target Product: MB9D560 Series Traveo™ Family

This application note describes an example of system configuration and setting for using of the three-phase motor control in the MB9D560 Series.

Contents

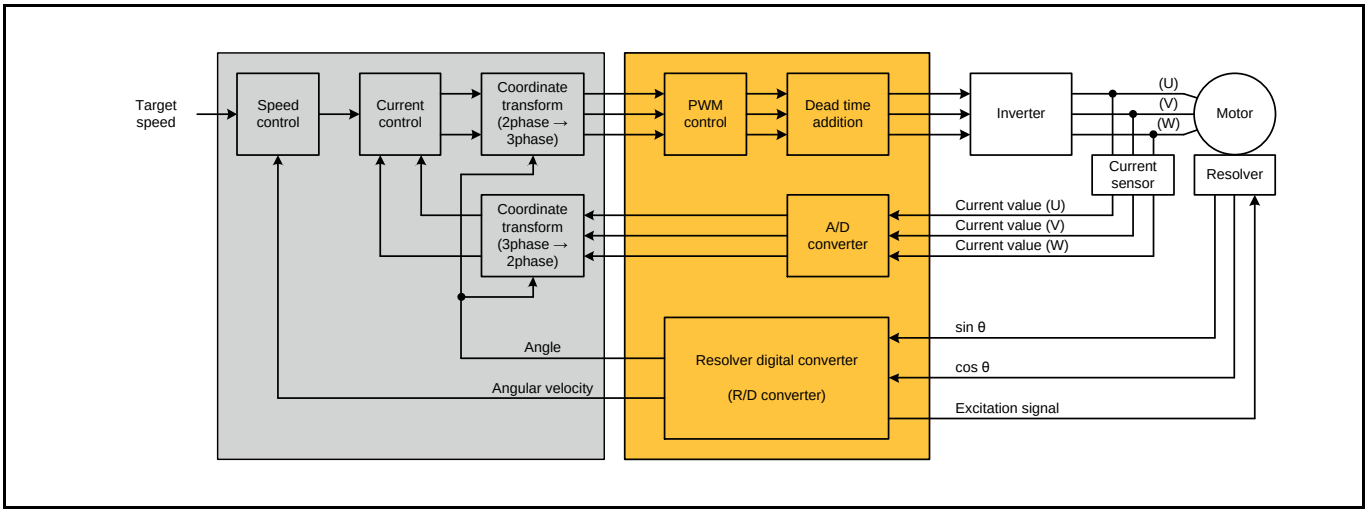
1 Introduction

This application note describes an example of system configuration and setting for using of the three-phase motor control in the MB9D560 Series.

2 Overview

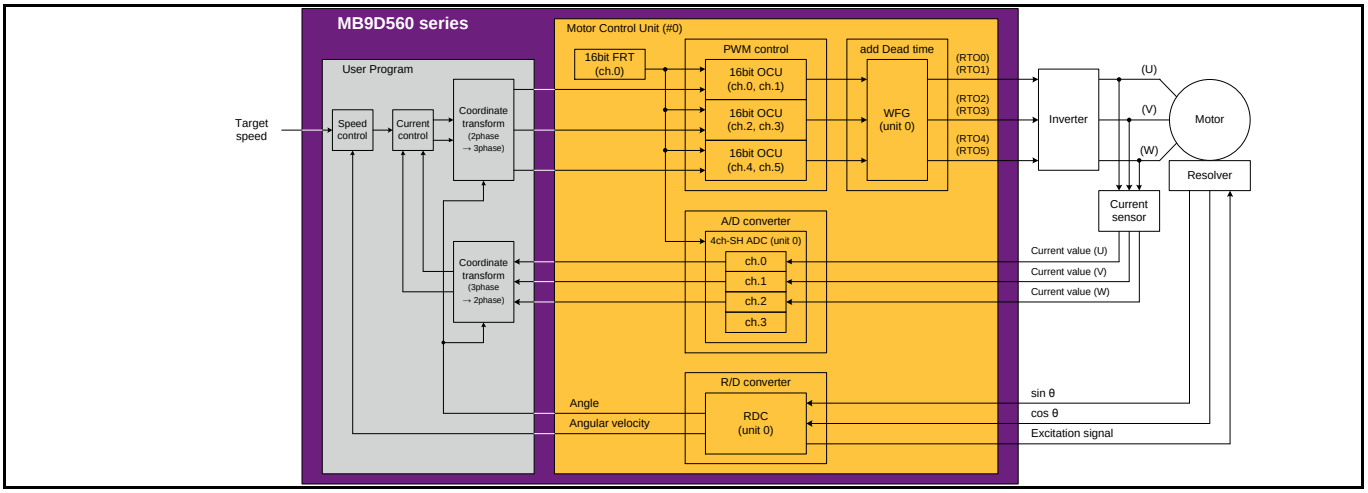
Figure 1 shows a system example of motor control. This system example is vector control by current feedback and the resolver is used for angle detection of the motor.

Figure 1. System Example of Vector Control by Current Feedback



The System Example on Figure 1 can be constructed by MB9D560 Series as Figure 2. The Speed Control, Current Control and Coordinate Transform are controlled by a program, and the Motor Control Unit can be constructed by each unit of the MB9D560 Series. This application note describes a specific example and the setting method of motor control unit.

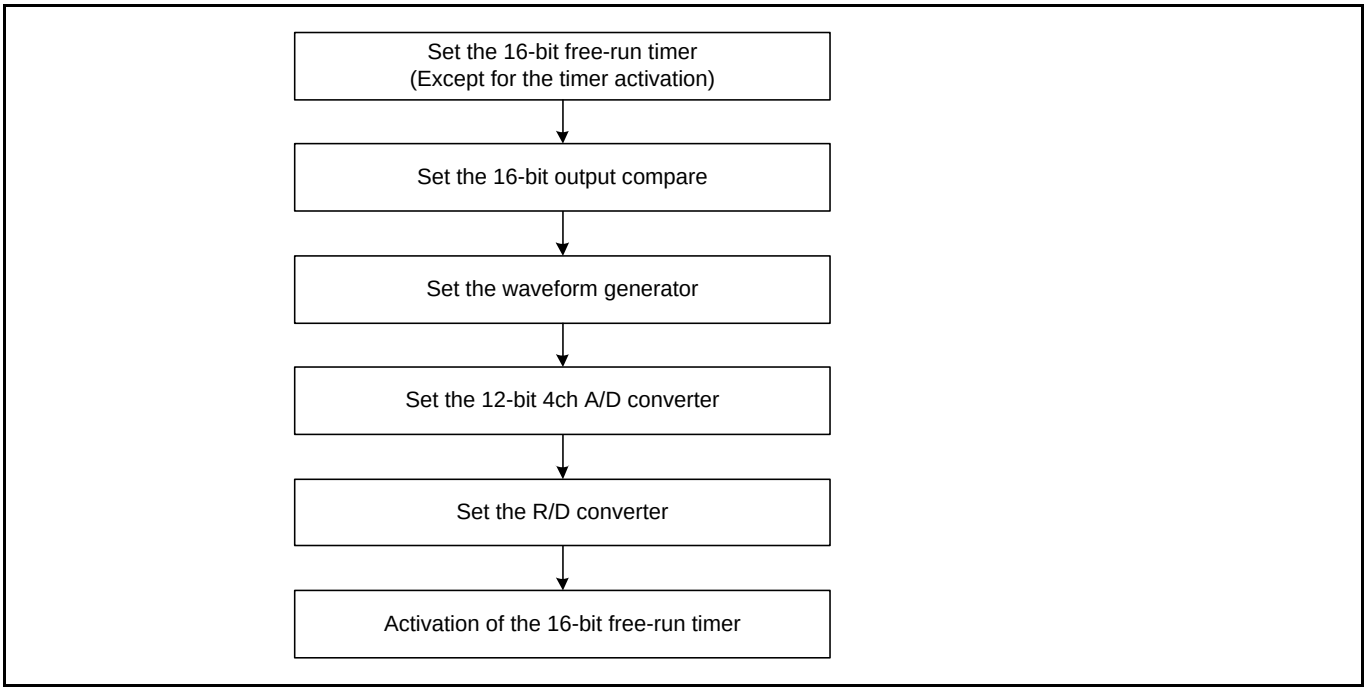
Figure 2. Configuration Example of Vector Control by Current Feedback in the MB9D560 Series



Note: MB9D560 Series has two motor control units (#0, #1). This application note describes only #0. #1 is same as configuration of #0, but a channel and unit number are different. For details on channel and unit number of #0 and #1, see 8.1 Relevant Unit for Three-phase Motor Control

The overall flows of each unit setting are as follows:

Figure 3. Configuration Flow of Motor Control Unit

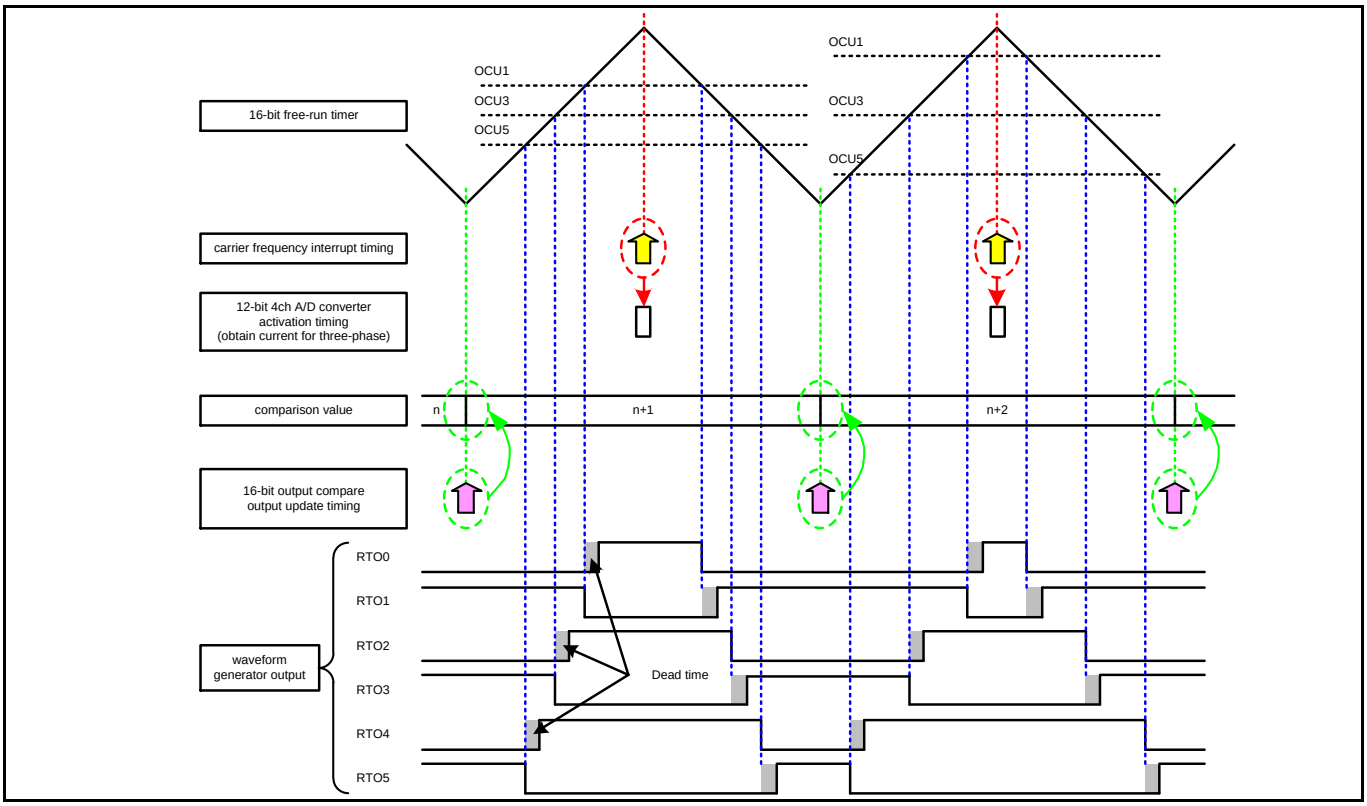


It is necessary to consider a timing of three-phase motor control in using each unit. The timing control conditions are as follows in this application note. The operation clock of each unit is assumed that it is limited to maximum 100 MHz.

Timing Control Conditions

- The carrier frequency (motor control period) is generated by the up/down count mode of (triangle wave) 16-bit free-run timer.
- The compare match detection interrupt of 16-bit free-run timer is the time base for the motor control.
- The current for three-phase is obtained by the 12-bit 4ch A/D converter. It starts conversion in sync with the 16-bit free-run timer.
- The signal for inverter control is generated by the 16-bit output compare unit. The 16-bit OCU is running based on the clock output of 16-bit free-run timer with the compare value given by a user's program. The compare value is updated at zero points of the triangle wave.
- The dead time is added by the waveform generator.

Figure 4. Timing Control



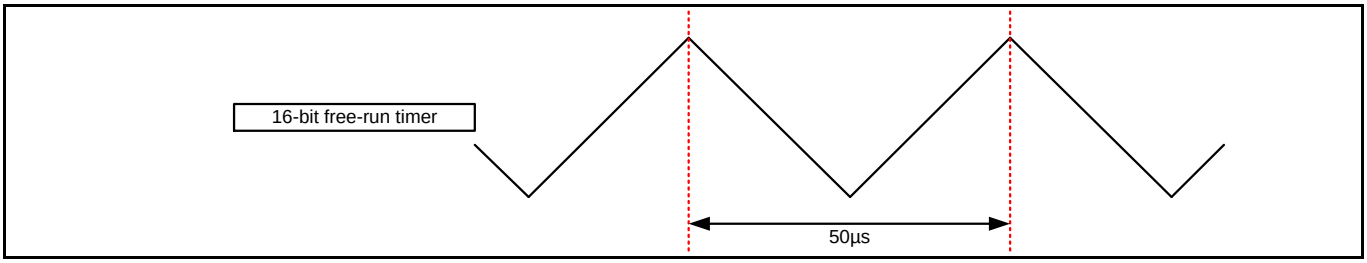
The following explanation is based on mentioned contents in this section.

3 16-bit Free-run Timer (16-bit FRT)

The free-run timer is counted up to the specified counted value with the input clock. When the free-run timer value matches a specified value, the free-run timer is counted down or re-counted up from zero. The free-run timer generates the carrier period in motor control.

This section explains how to generate a carrier period signal with the 16-bit FRT (ch.0).

Figure 5. Output Signal of the 16-bit Free-run Timer (ch.0)



3.1 Overview

Configuration of 16-bit FRT is described below.

3.1.1 Selection of Operation Clock

The clock for a count of operation is chosen from an external clock (FRCK) or an internal clock (CLK_PERI4, CLK_PERI5).

When an internal clock is chosen, the following divider for the operation clocks (ϕ, ϕ/2, ϕ/4,ϕ/8, ϕ/16, ϕ/32, ϕ/64, ϕ/128, ϕ/256) can be selected by internal prescaler.

Note: ϕ The frequency of an internal clock (CLK_PERI4, CLK_PERI5)

3.1.2 Selection of Count Mode

The count mode can choose Up count mode (sawtooth wave) or Up/down count mode (triangle wave).

3.1.3 Interrupts of the 16-bit Free-Run Timer

Comparison clear interrupt is generated when the free-run timer value matches a compare clear register value. Zero detection interrupt is generated when the 16-bit free-run timer value is 0x0000.

The interrupt can be masked between one to eight times by an interrupt mask function. Both of interrupt can be masked in Up/down count mode.

3.1.4 Selector of 16-bit FRT

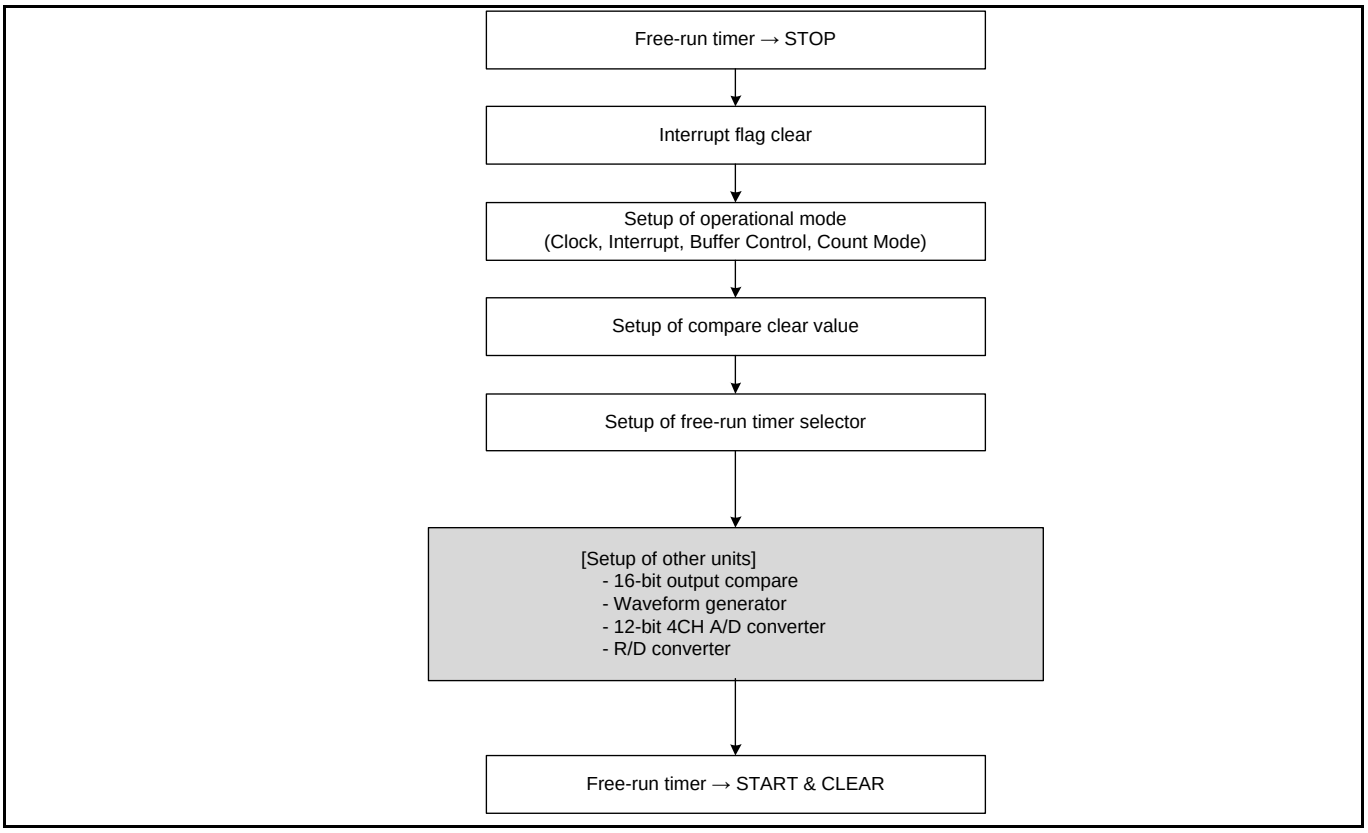
The counted value of a free-run timer can be used as counted value of 16-bit output compare, 16-bit input capture, 12-bit A/D converter, and 12-bit 4CH A/D converter by the Free-run Timer Selection Registers.

3.2 Details of Setup

3.2.1 Setup Procedure Example

The setup flow of the 16-bit FRT is as below.

Figure 6. Setup Flow

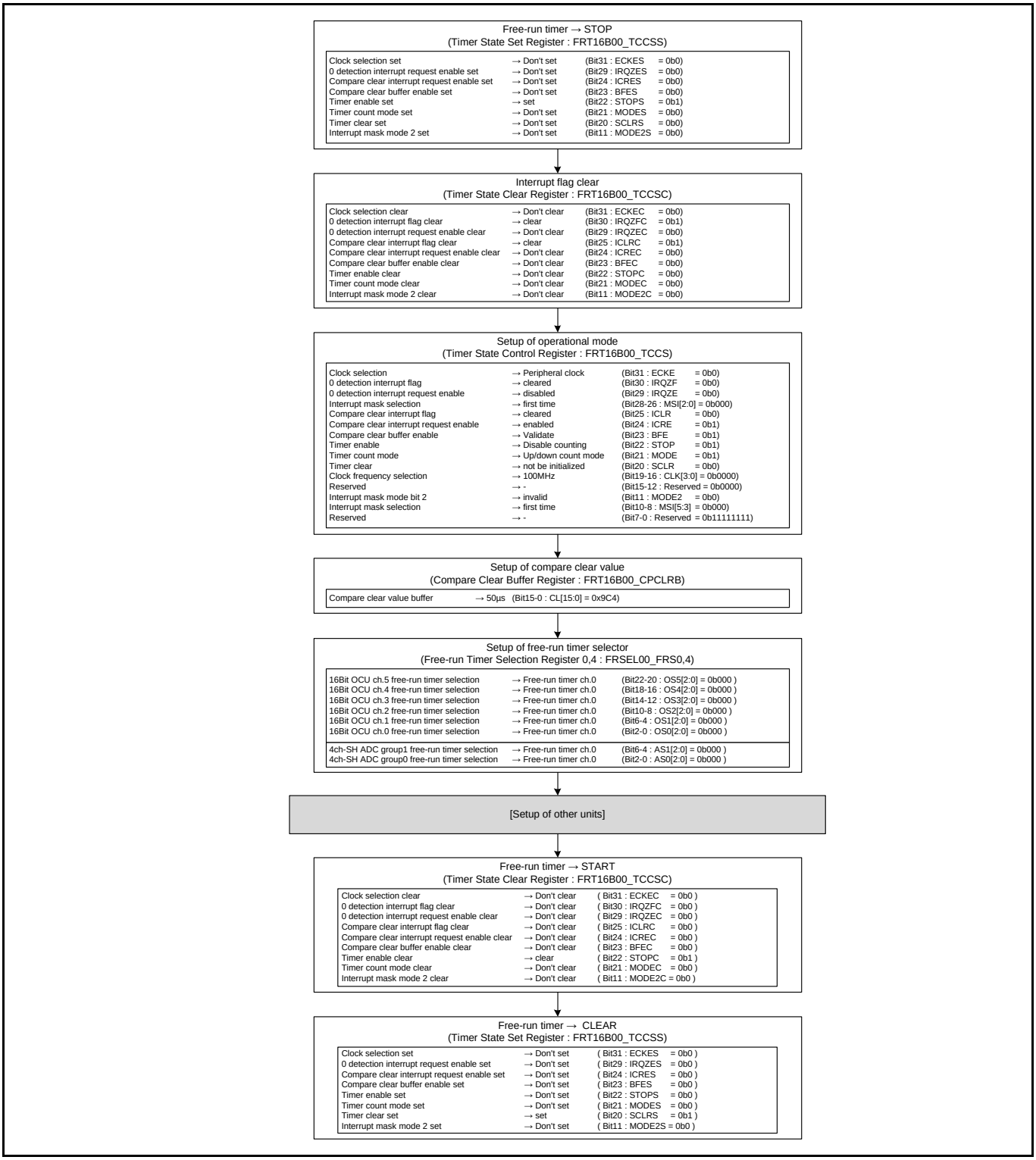


Note: Please perform start of the free-run timer after setup of each unit.

The register used for a setup of a 16-bit free-run timer is as follows. The example of a detailed setup is shown in Figure 7.

- FRT16Bxx_CPCLR : Compare Clear Register (xx = 00-19)
- FRT16Bxx_TCCS : Timer State Control Register (xx = 00-19)
- FRT16Bxx_TCCSC : Timer State Clear Register (xx = 00-19)
- FRT16Bxx_TCCSS : Timer State Set Register (xx = 00-19)
- FRSELxx_FRS0 : Free-run Timer Selection Register 0 (xx = 00/01/02)
- FRSELxx_FRS4 : Free-run Timer Selection Register 4 (xx = 00/01)

Figure 7. Setup Example of 16-bit FRT



3.2.2 Setup of Timer State Control Register (TCCS)

The Timer State Control Register (FRT16Bxx_TCCS) is a register used for controlling the operation of the 16-bit free-run timer.

The contents of a setting in 3.2.1 Setup Procedure Example are as follows.

Table 1. Setup Example of Timer State Control Register (FRT16Bxx_TCCS)

Bit	Bit Name		Setting Register		Bit Clear (FRT16Bxx _TCCSC)	Bit Set (FRT16Bxx _TCCSS)
			Value	Contents		
31	ECKE	Clock selection	0b0	Peripheral clock	✓	✓
30	IRQZF	0 detection interrupt flag	0b0	Cleared	✓	-
29	IRQZE	0 detection interrupt request enable	0b0	Disabled	✓	✓
28-26	MSI[2:0]	Interrupt mask selection	0b000	First time	-	-
25	ICLR	Compare clear interrupt flag	0b0	Cleared	✓	-
24	ICRE	Compare clear interrupt request enable	0b1	Enabled	✓	✓
23	BFE	Compare clear buffer enable	0b1	Validate	✓	✓
22	STOP	Timer enable	0b1	Disable counting	✓	✓
21	MODE	Timer count mode	0b1	Up/down count mode	✓	✓
20	SCLR	Timer clear	0b0	Not be initialized	-	✓
19-16	CLK[3:0]	Clock frequency selection	0b0000	100 MHz	-	-
15-12	Reserved	Reserved	0b000	-	-	-
11	MODE2	Interrupt mask mode 2	0b0	Invalid	✓	✓
10-8	MSI[5:3]	Interrupt mask selection	0b000	First time	-	-
7-0	Reserved	Reserved	0b11111111	-	-	-

Note: In order to prevent the unexpected operation by clock selection change and clock frequency change, Bit31(ECKE), Bit19-16(CLK[3:0]) must make the same a setup at the time of a stop of operation and a start of operation.

Note: Please set up Bit20(SCLR) after a timer start. It is also possible to set up simultaneously.

If FRT16Bxx_TCCSC and FRT16Bxx_TCCSS are used, the bit which wants to change a setup can be cleared / set individually. It is also possible to clear / set plurality simultaneously. In 3.2.1 Setup Procedure Example, the timer is started after each completion of a setting by FRT16Bxx_TCCSC.

FRT16Bxx_TCCSC clears a bit to 0b0 and FRT16Bxx_TCCSS sets a bit to 0b1.

3.2.3 Calculation Method of Compare Clear Value

The cycle of an output signal is set as CPCLR.

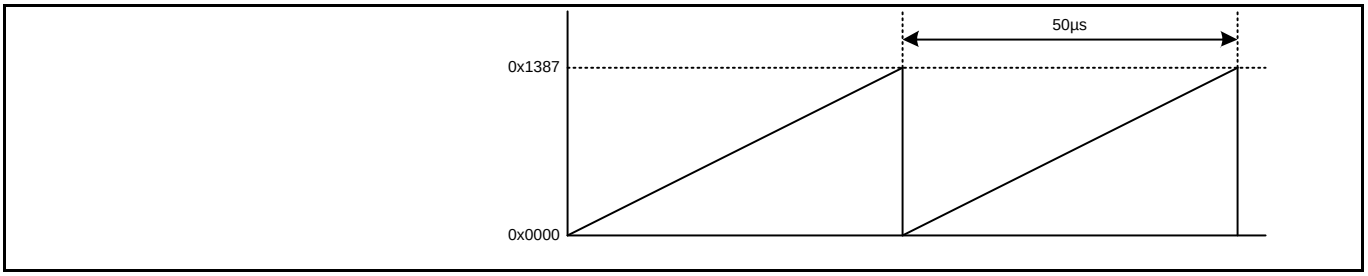
When counting 50µs with a clock (CLK PERI4, 100 MHz), the value to CPCLR can be computed as follows.

(1) In the case of Up count mode

Value to CPCLR = Count Value - 1
= (carrier period ÷ clock period) - 1
= (50µs ÷ 10ns) - 1
= 5000 - 1 = 4999
= 0x1387

Therefore, periodic signals will be 50µs if 0x1387 is set to FRT16Bxx_CPCLR.

Figure 8. Timer Operation at the Time of Up Count Mode

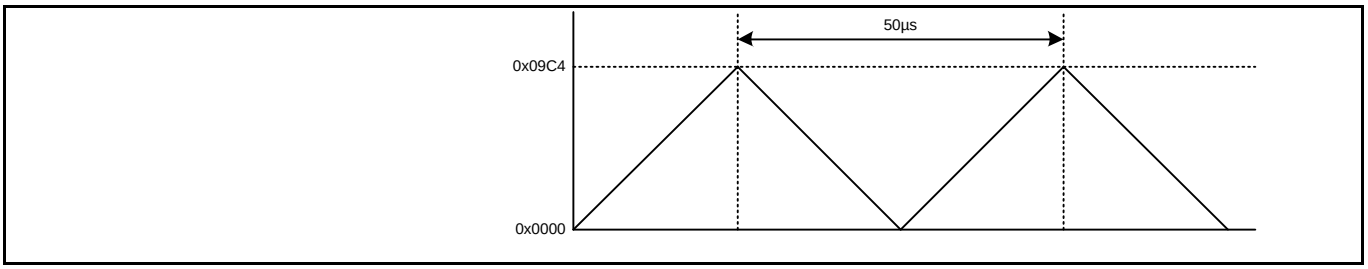


(2) In the case of Up/down count mode

Value to CPCLR = Count Value ÷ 2
= (carrier period ÷ clock period) ÷ 2
= (50µs ÷ 10ns) ÷ 2
= 5000 ÷ 2 = 2500
= 0x9C4

Therefore, periodic signals will be 50µs if 0x9C4 is set to FRT16Bxx_CPCLR.

Figure 9. Timer Operation at the Time of Up/down Count Mode



3.2.4 Updating Compare Clear Value

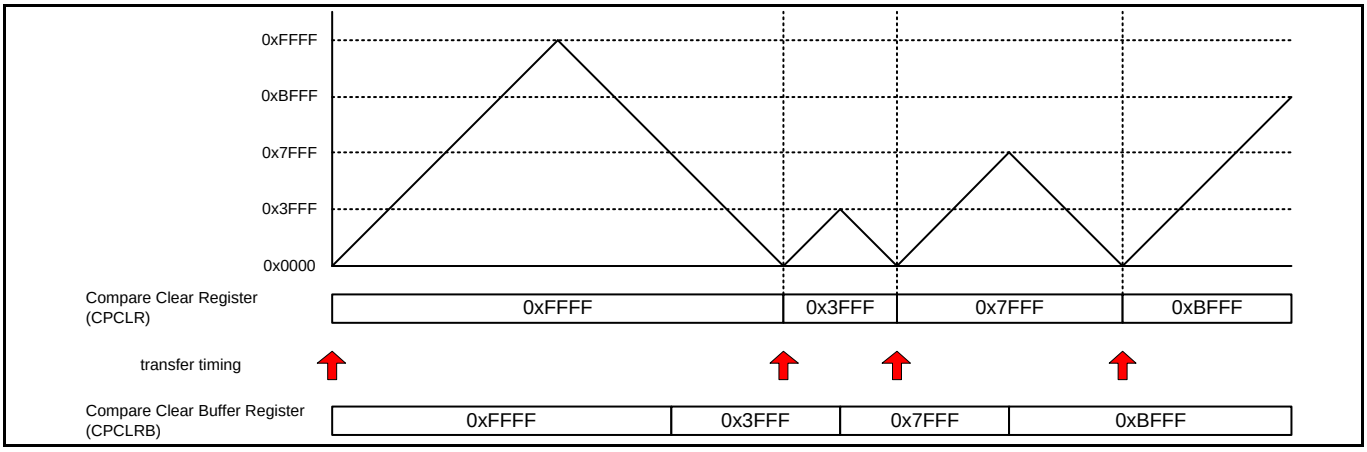
By the speed and torque of a motor, a carrier period may be changed at three-phase motor control.

In this case, you have to change a carrier period without suspending a timer. In changing a carrier period without suspending a timer, please refer to the following and set it up.

- A buffer is validated by Compare clear buffer enable (BFE).
- A new carrier period is set to FRT16Bxx_CPCLRB.
- A carrier period new at the time of zero detection is transmitted.

When a buffer is in-validate, the value written in the FRT16Bxx_CPCLRB is immediately reflected as the compare clear value.

Figure 10. Example of Updating Compare Clear Value (BFE = 0b1)



3.2.5 Setup of Free-run Timer Selection Register

16-bit FRT can operate in close cooperate with 16-bit OCU, 16-bit ICU, SH-ADC, and 4ch-SH-ADC by a free-run timer selection register.

There are 0, 1, and 2 in the free-run timer selector and it corresponds to free-run timer ch.0-5, ch.6-11, and ch.12-17, respectively. Block diagram is shown in Figure 11 and Figure 12.

Figure 11. Block Diagram of Free-run Timer Selector (FRSEL00, FRSEL01)

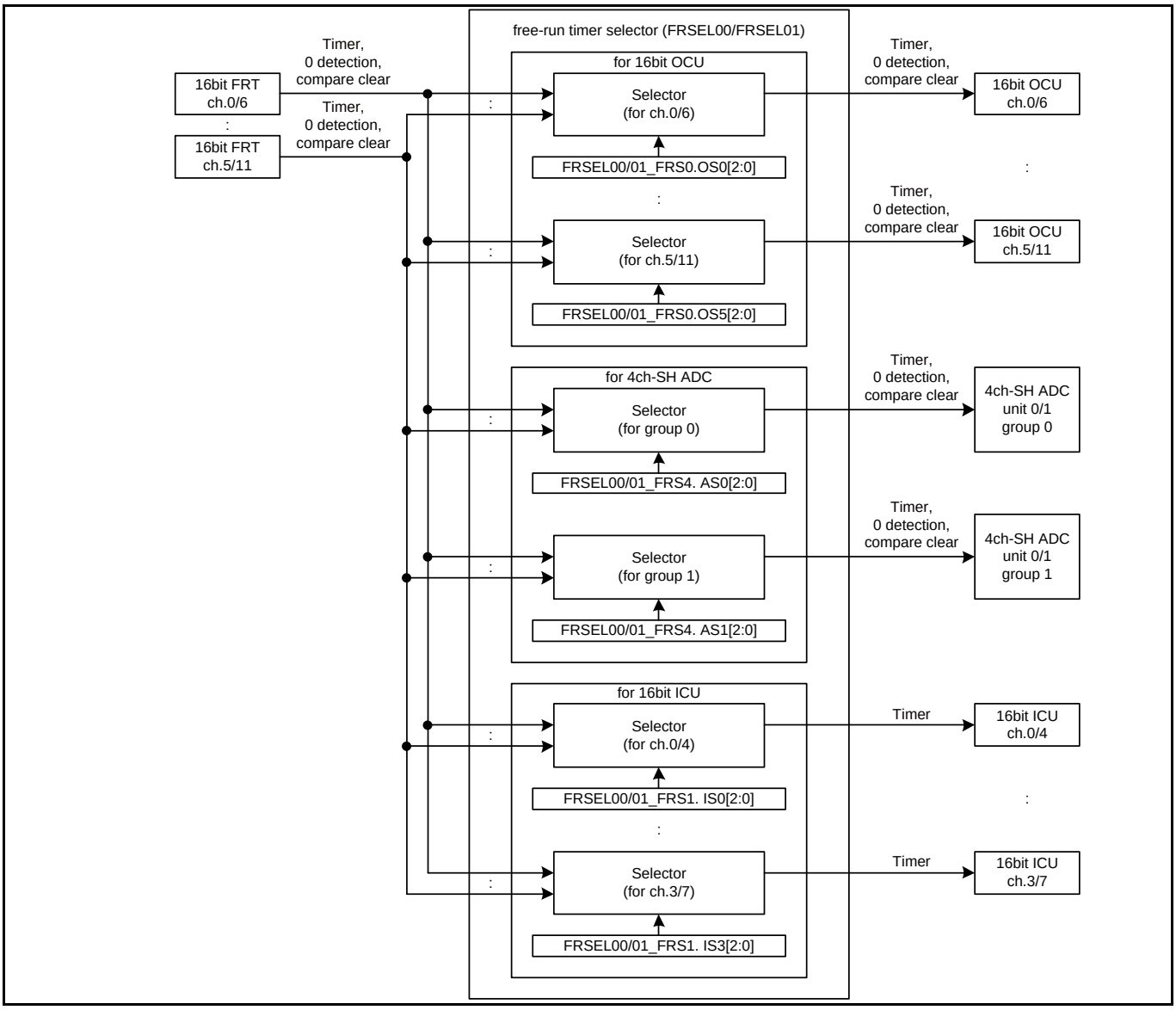
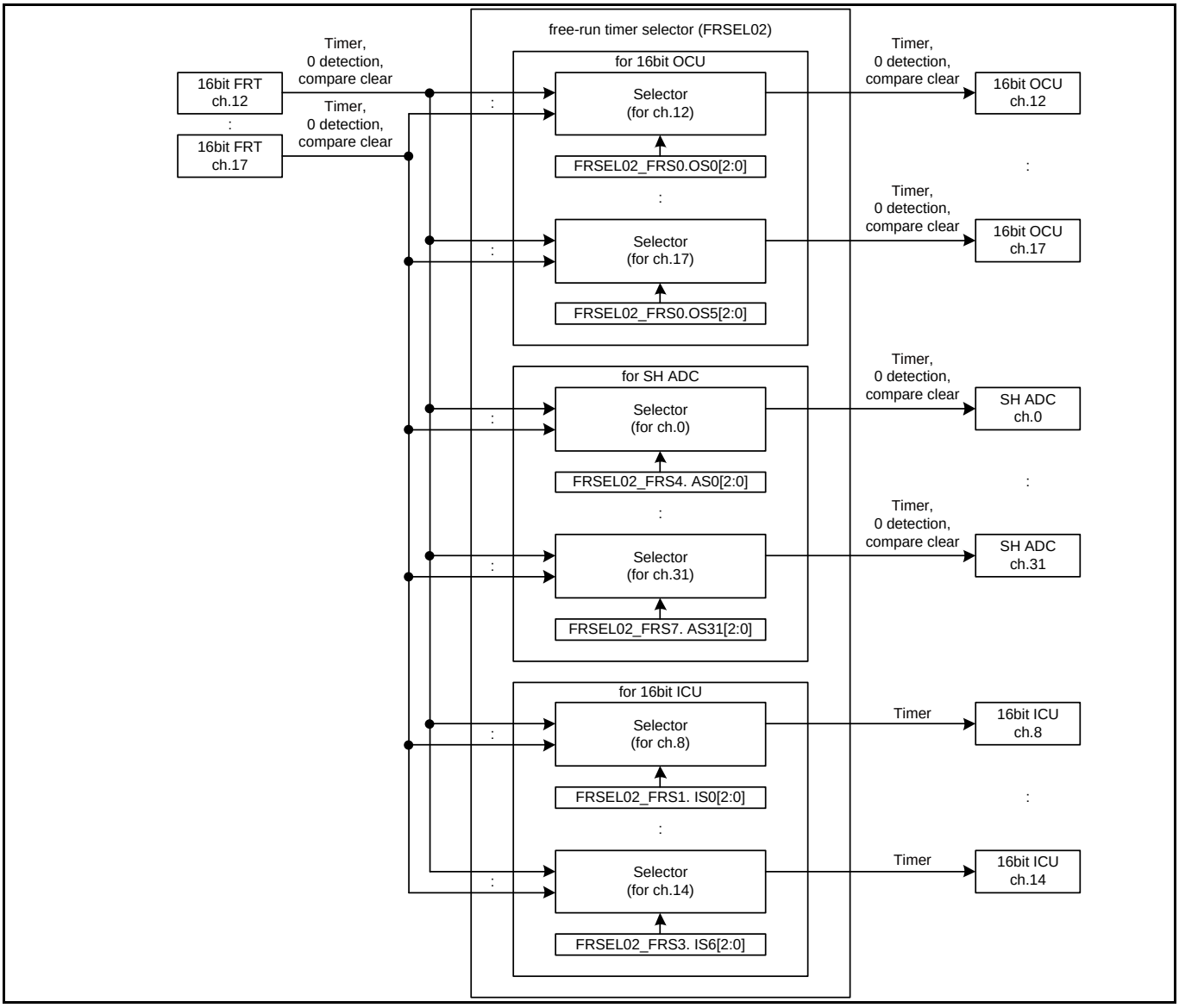


Figure 12. Block Diagram of Free-run Timer Selector (FRSEL02)



The setting method of 16-bit OCU and 4ch-SH ADC is indicated below.

16-bit Output Compare

16-bit FRT synchronized with 16-bit OCU is chosen by FRSELxx_FRS0.

When choosing the 0ch of 16-bit FRT, 0b000 is set to OS(channel number)[2:0]. When choosing the 1ch of 16-bit FRT, 0b001 is set to OS(channel number)[2:0].

In a setup of Table 2, 16-bit OCU0, 1, 2, 3, 4, and 5 synchronizes with the ch.0 of 16-bit FRT.

Table 2. Example of Free-run Timer Selection Register 0

16-bit Output Compare Channel	Register Name	Bit Name	Value
16-bit OCU (ch.0)	FRSEL00_FRS0	OS0[2:0]	0b000
16-bit OCU (ch.1)	FRSEL00_FRS0	OS1[2:0]	0b000
16-bit OCU (ch.2)	FRSEL00_FRS0	OS2[2:0]	0b000
16-bit OCU (ch.3)	FRSEL00_FRS0	OS3[2:0]	0b000
16-bit OCU (ch.4)	FRSEL00_FRS0	OS4[2:0]	0b000
16-bit OCU (ch.5)	FRSEL00_FRS0	OS5[2:0]	0b000

12-bit 4CH A/D Converter

16-bit FRT synchronized with 4ch-SH ADC is chosen by FRSELxx_FRS4.

When choosing the 0ch of 16-bit FRT, 0b000 is set to AS(unit number)[2:0]. When choosing the 1ch of 16-bit FRT, 0b001 is set to AS(channel number)[2:0].

In a setup of Table 3, activation group 0/1 of 4ch-SH ADC (unit0) synchronizes with the ch.0 of 16-bit FRT.

Table 3. Example of Free-run Timer Selection Register 4

12-bit 4ch A/D Converter Activation Group	Register Name	Bit Name	Value
4ch-SH ADC [unit 0, activation group 0]	FRSEL00_FRS4	AS0[2:0]	0b000
4ch-SH ADC [unit 0, activation group 1]	FRSEL00_FRS4	AS1[2:0]	0b000

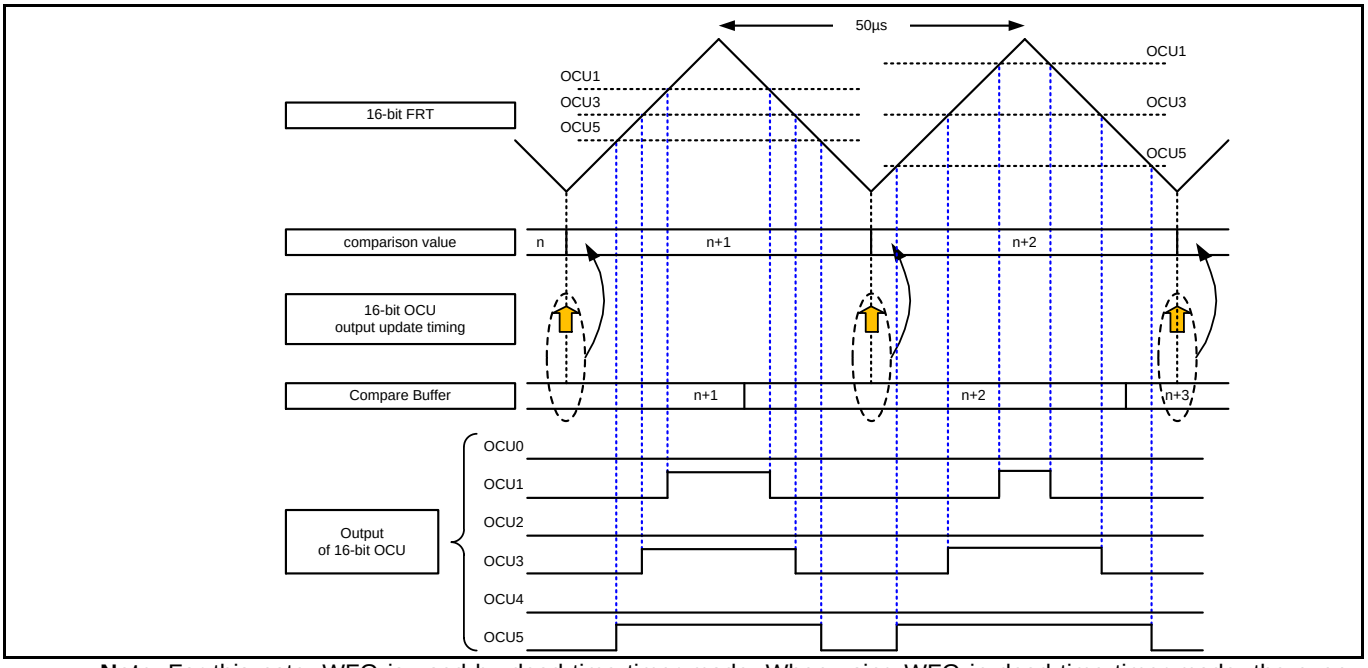
4 16-bit Output Compare (16-bit OCU)

16-bit output compare compares a comparison value set as register with counted value of 16-bit free-run timer. An output is reversed when a comparative result becomes the same. In motor control, 16-bit OCU is used for PWM waveform generation.

This section explains how to generate a carrier period signal with the 16-bit FRT (ch.0).

In this section, 16-bit OCU (ch.0 - ch.5) explains how to generate the PWM waveform (OCU1, OCU3, OCU5) shown in Figure 13.

Figure 13. The Example of PWM Waveform Generation.



Note: For this note, WFG is used by dead time timer mode. When using WFG in dead time timer mode, the even number output (OCU0, OCU2, OCU4) of 16-bit OCU is disregarded.

Note: Comparison value should set the value of 2 phase to 3 phase conversion calculated by the user program.

4.1 Overview

The setup of the 16-bit OCU is described below.

4.1.1 Operational Overview of 16-bit Output Compare

16-bit OCU compares the comparison value with the counter value of 16-bit FRT. When the counter value matched with the compare value, the compare-match interrupt is generated and the OCU output level is inverted.

4.1.2 Output of Compare Waveform

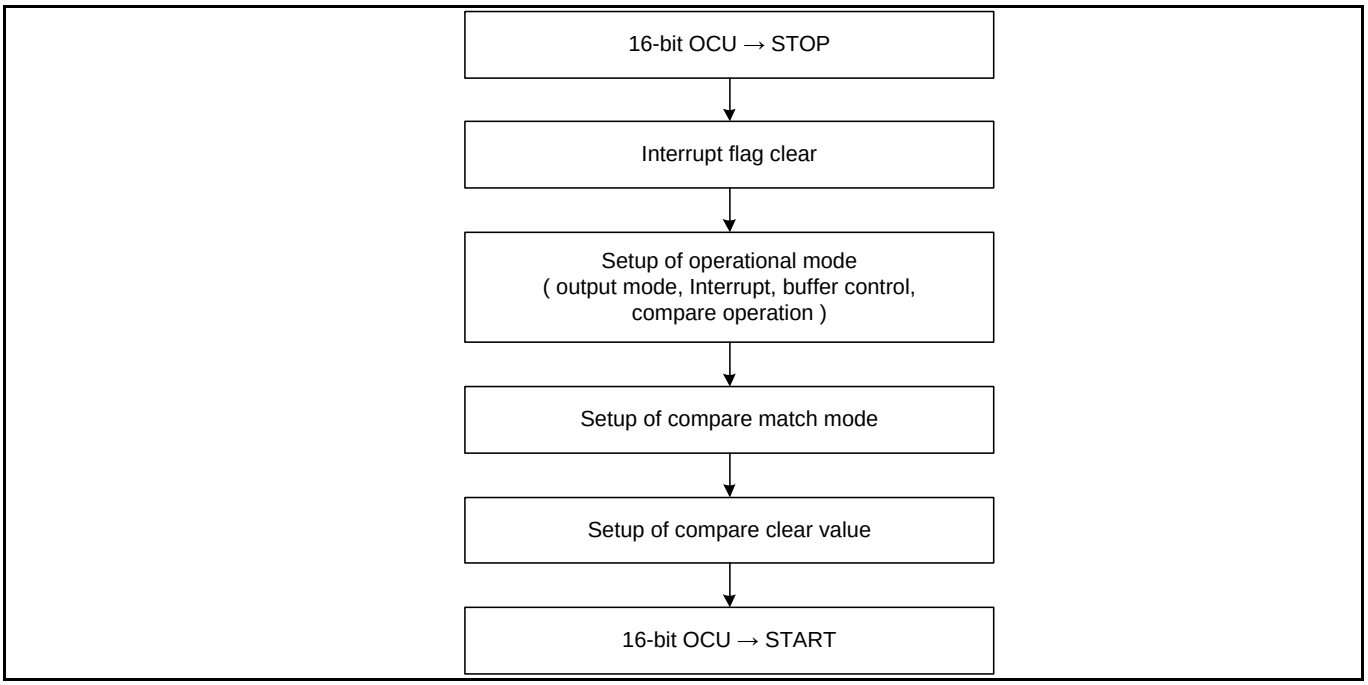
The output waveform is controlled by Output level inversion mode bit (CMOD) of the Compare Control Register (OCU16Bxx_OCS), and the Compare Mode Control Register (OCU16Bxx_OCMOD).

4.2 Details of Setup

4.2.1 Setup Procedure Example

The setup flow of the 16-bit OCU is as below.

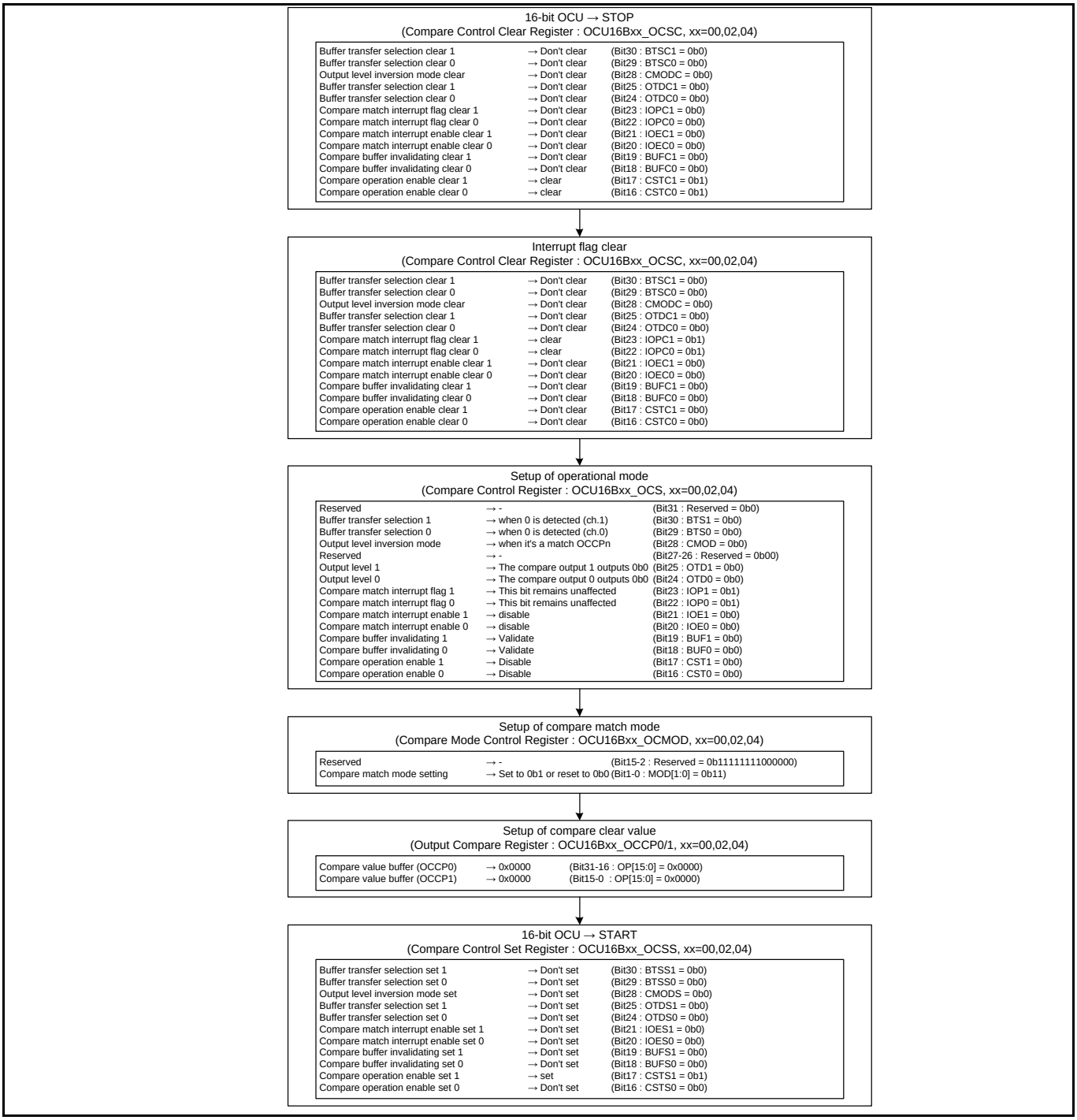
Figure 14. Setup Flow



The register used for a setup of a 16-bit OCU is as follows. The example of a details setup is shown in Figure 14.

- OCU16Bxx_OCS : Compare Control Register
- OCU16Bxx_OCSS : Compare Control Set Register
- OCU16Bxx_OCMOD : Compare Mode Control Register
- OCU16Bxx_OCCP0/1 : Output Compare Register 0/1
- OCU16Bxx_OCCPB0/1 : Output Compare Buffer Register 0/1
  - (Note) xx = 00, 02, 04, 06, 08, 10, 12, 14, 16, 18, 20, 22
  - xx=00 : 16-bit OCU ch.0/ch.1
  - xx=02 : 16-bit OCU ch.2/ch.3
  - :
  - xx=22 : 16-bit OCU ch.22/ch.23

Figure 15. Setup Example of 16-bit OCU



Note: The register with a comment (xx = 00,02,04) must set up three registers 00, 02, and 04.

4.2.2 Setup of Compare Control Register and Compare Mode Control Register

Compare Control Register (OCU16Bxx_OCS, xx = 00,02,04) performs various setup shown in the following Table 4. Compare Mode Control Register (OCU16Bxx_OCMOD) performs an output setup at the time of comparison coincidence.

Compare Control Register

Table 4 .Setup Example of Compare Control Register (OCU16Bxx_OCS, xx = 00,02,04)

Bit	Bit Name		Setting Register		Bit Clear (OCU16Bxx _OCSC)	Bit Set (OCU16Bxx _OCSS)
			Value	Contents		
31	Reserved	Reserved	0b0	-	-	-
30, 29	BTS[1:0]	Buffer transfer selection[1:0]	0b00	when 0b0 is detected	✓	✓
28	CMOD	Output level inversion mode	0b0	when it's a match OCCP0, OCCP1	✓	✓
27, 26	Reserved	Reserved	0b00	-	-	-
25, 24	OTD[1:0]	Output level[1:0]	0b00	compare output = 0b0	✓	✓
23, 22	IOP[1:0]	Compare match interrupt flag[1:0]	0b00	This bit remains unaffected	✓	-
21, 20	IOE[1:0]	Compare match interrupt enable[1:0]	0b00	disable	✓	✓
19, 18	BUF[1:0]	Compare buffer invalidating[1:0]	0b00	Validate	✓	✓
17, 16	CST[1:0]	Compare operation enable[1:9]	0b00	Disable	✓	✓

If OCU16Bxx_OCSC and OCU16Bxx_OCSS are used, the bit which wants to change a setup can be cleared/set individually. It is also possible to clear/set plurality simultaneously. In 4.2.1 Setup Procedure Example, the 16-bit OCU is started after each completion of a setting by OCU16Bxx_OCSS.

OCU16Bxx_OCSC clears a bit to 0b0 and OCU16Bxx_OCSS sets a bit to 0b1.

Compare Mode Control Register

Table 5. Setup Example of Compare Mode Control Register (OCU16B00_OCMOD, xx = 00,02,04)

Bit	Bit Name		Setting Register	
			Value	Contents
15 - 2	Reserved	Reserved	0b11111111000000	-
1, 0	MOD[1:0]	Compare match mode setting	0b11	Set the output value to 0b1 or reset it to 0b0 according to the setting of the CMOD bit in the compare control register (OCS).

Reverse Output Mode

By setting MOD [1:0] of OCMOD to 0b00, the 16-bit OCU operates reverse output mode.

1. In the case of CMOD = 0b0 of OCU16Bxx_OCS

In this mode, when a free-run timer value is the same as Output Compare Register value, the output of ch.0 and ch.1 is reversed.The output of ch.2/3, ch.4/5, ch.6/7, ch.8/9, and ch.10/11 is reversed as ch.0/1.

2. In the case of CMOD = 0b1 of OCU16Bxx_OCS

In this mode, when a free-run timer value is the same as Output Compare Register value, the output of ch.0 is reversed. Ch.1 is reversed when a free-run timer value is the same as the Output Compare Register value of ch.0 and ch.1.

The output of ch.2/3, ch.4/5, ch.6/7, ch.8/9, and ch.10/11 is reversed as ch.0/1.

Set/Reset Mode

By setting MOD [1:0] of OCMOD to 0b11, the 16-bit OCU operates set/reset mode.

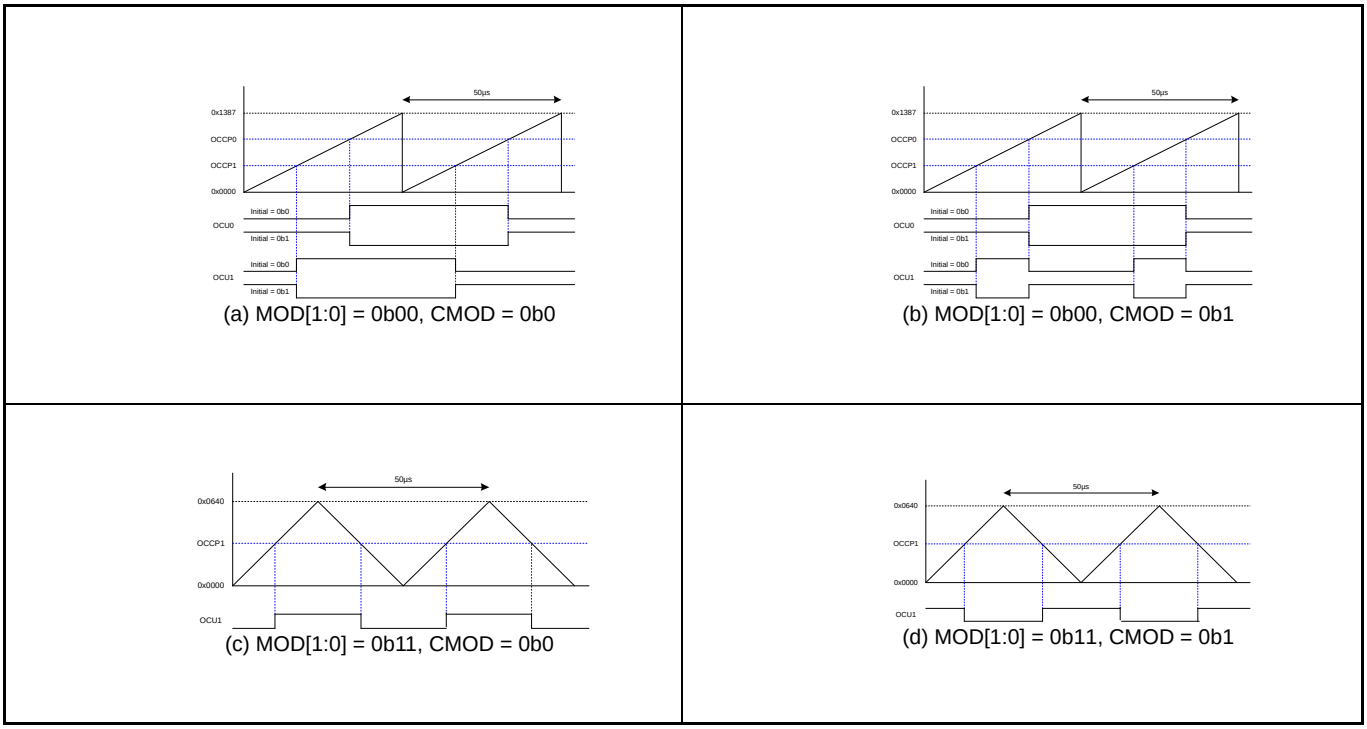
In the case of CMOD = 0b0 of OCU16Bxx_OCS

Coincidence of up count is set to 0b1 and coincidence of down count is reset by 0b0, in up/down count mode (triangle wave).

In the case of CMOD = 0b1 of OCU16Bxx_OCS

Coincidence of up count is reset to 0b0 and coincidence of down count is reset by 0b1, in up/down count mode (triangle wave).

Figure 16. Example of Waveform Generate



4.2.3 Setup of Output Compare (Buffer) Register

The register which sets up a comparison value consists of Output Compare Register (OCU16Bxx_OCCP0/1) and Output Compare Buffer Register (OCU16Bxx_OCCPB0/1).

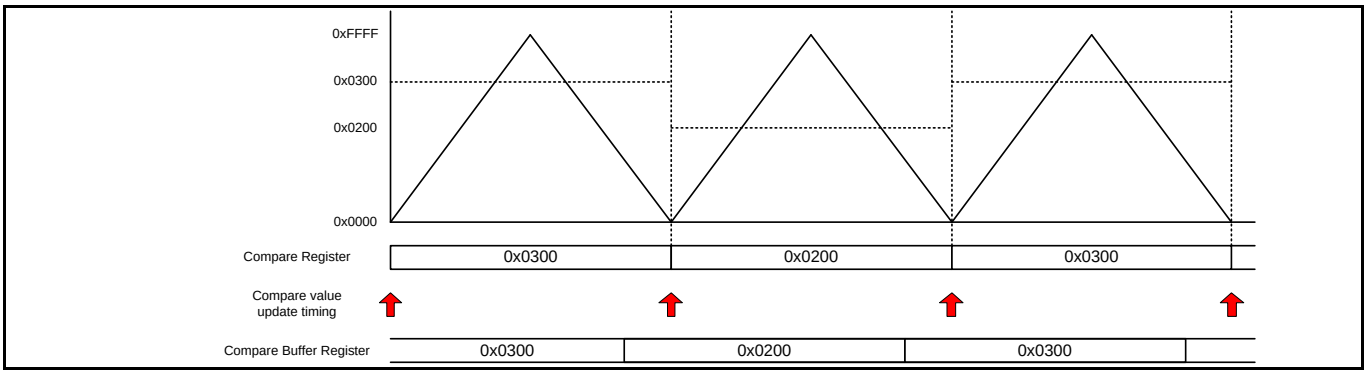
When a function of compare buffer is disabled, the value written in OCU16Bxx_OCCPB0/1 is immediately reflected in OCU16Bxx_OCCP0/1.

When a function of compare buffer is enabled, the value written in the OCU16Bxx_OCCPB0/1 is transmitted to a OCU16Bxx_OCCP0/1 by the specified transfer timing.

Note: Compare buffer invalidating : cf. BUF[1:0] of Compare Control Register (OCU16Bxx_OCS)

Note: Buffer transfer selection : cf. BTS[1:0] of Compare Control Register (OCU16Bxx_OCS)

Figure 17. Compare Value Update Timing (Transfer is activated when 0 is detected)

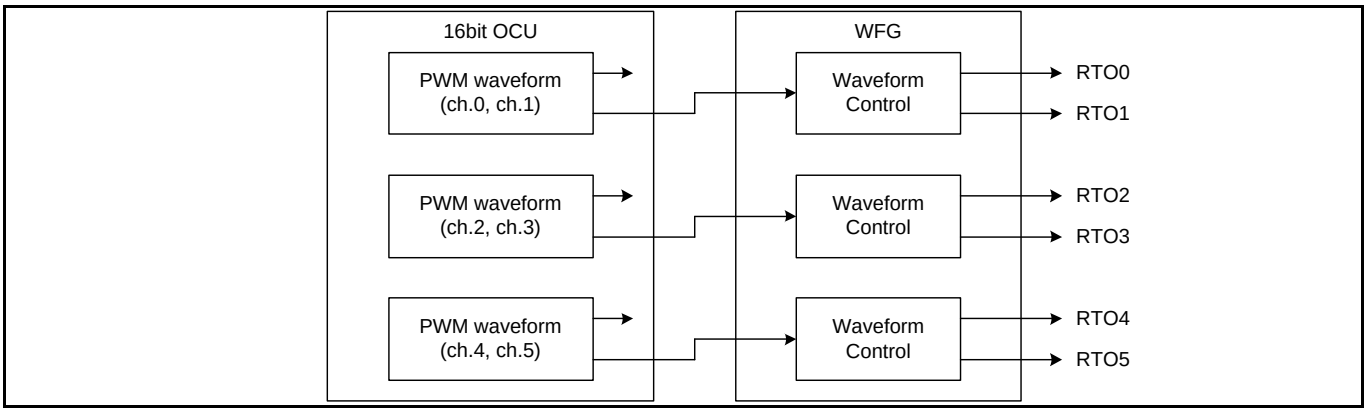


5 Waveform Generator (WFG)

WFG adds the dead time in Motor control to the output of 16-bit OCU. Moreover, WFG generates the upper and lower switching waveform for Motor control U phase, V phase, and W phase.

The connection of 16-bit OCU and WFG is as follows.

Figure 18. Connection of 16-bit OCU and WFG for Dead Timer Mode



This section explains how to generate the switching waveform of the upper and lower arm for Motor control, and how to generate the dead time for Motor control.

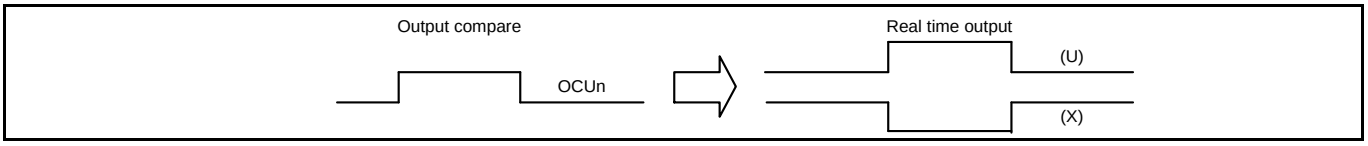
5.1 Overview

The setup of the WFG is described below.

5.1.1 Real-time Output

WFG generates two signals (real-time output) of positive-phase and negative-phase from the output signal of 16-bit OCU. In total, six RT outputs are generable.

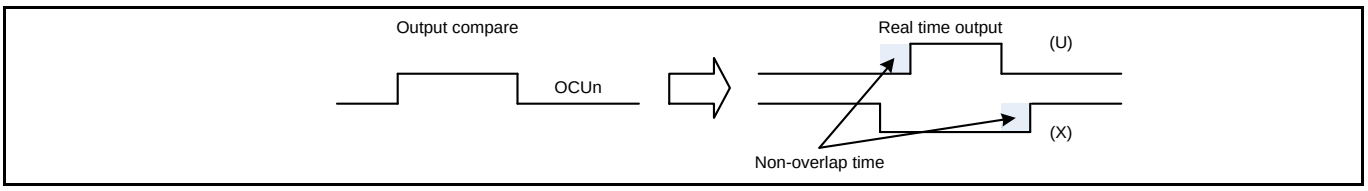
Figure 19. Real-time Output



5.1.2 Generation of Non-overlap Time

A non-overlap time is added to the above real-time output. A non-overlap time is set to 16-bit Dead Timer Register.

Figure 20. Non-overlap Time



5.1.3 Output Level Conversion Control

The real-time output of six is reversed independently. By this function, it is connectable with the inverter which differs in the switch polarity of an up-and-down arm.

Figure 21. Block Diagram of Output Level Conversion Control

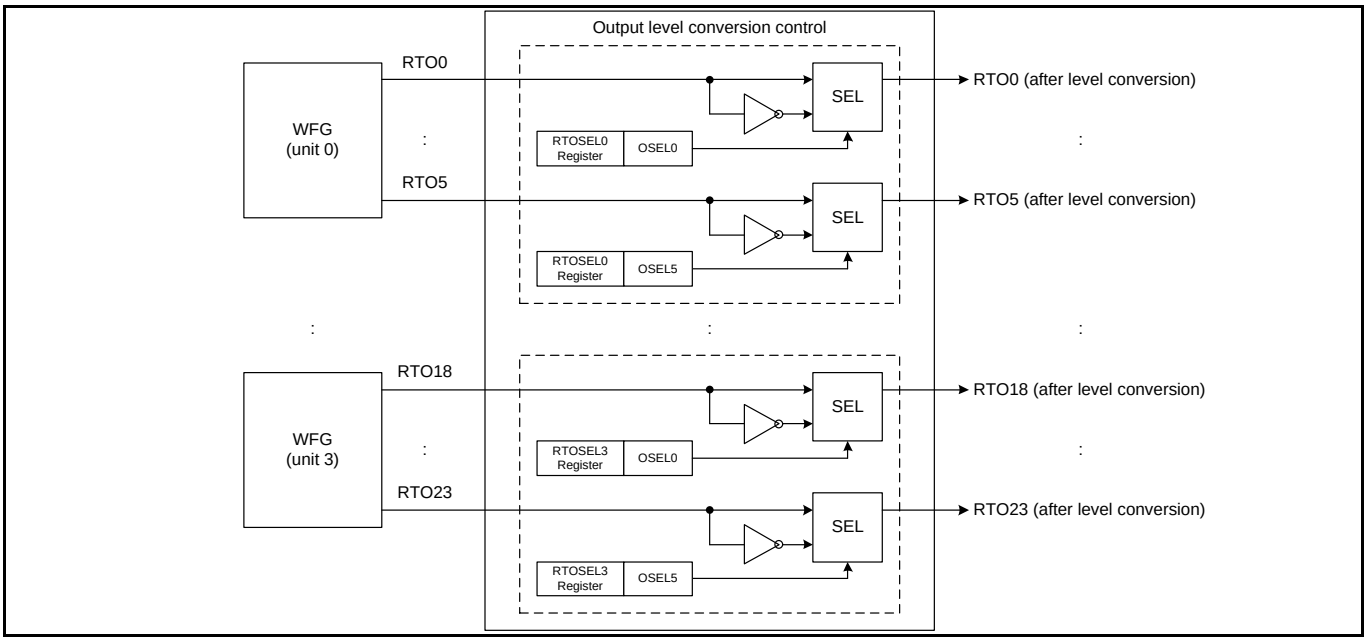
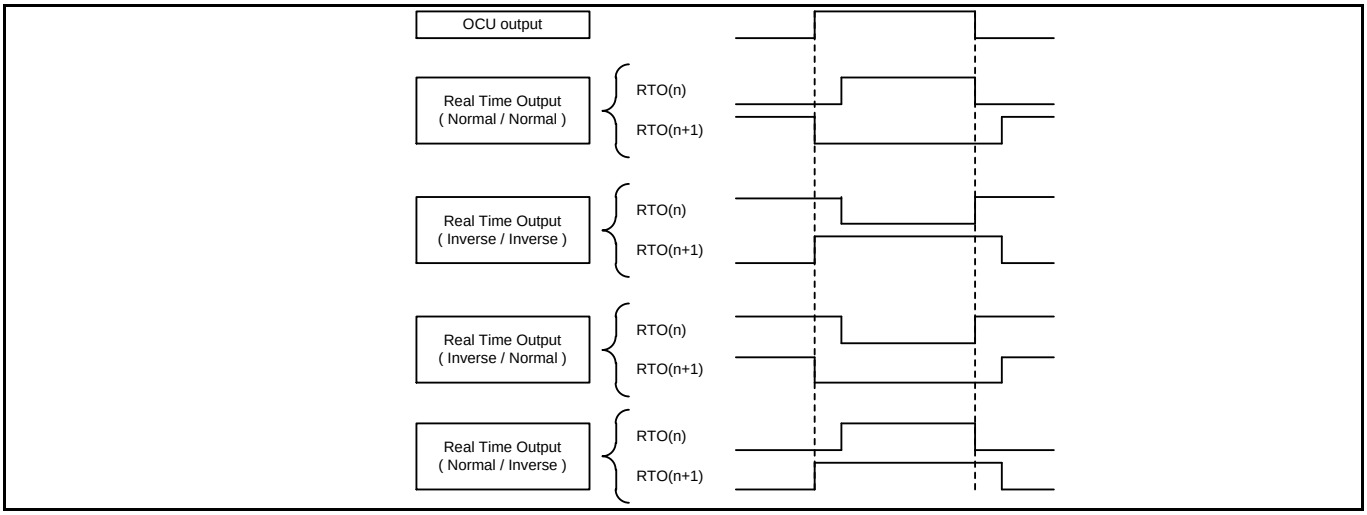


Figure 22. Timing Chart of Output Level Conversion Control



5.1.4 Operation of the DTTI Pin Control

The DTTI function is a function to forced stop a WFG output. The DTTI function operates by the specification from an external port and software.
The forcible stop operation of the DTTI pin and the DTTI register can forcibly disable waveform generator output and make the port work as a general-purpose port. This is achieved regardless of the setting of the POF[2:0] bits in the port setting register (PPC_PCFGRijj).

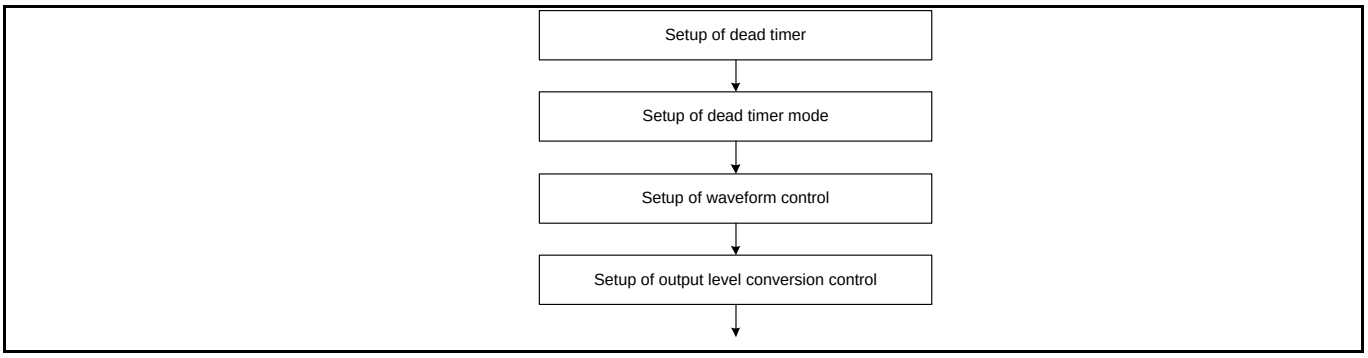
If it sets up so that a motor may stop a general-purpose port, motor control can be suspended only with specification of an external port.

5.2 Details of Setup

5.2.1 Setup Procedure Example

The setup flow of the WFG is as below.

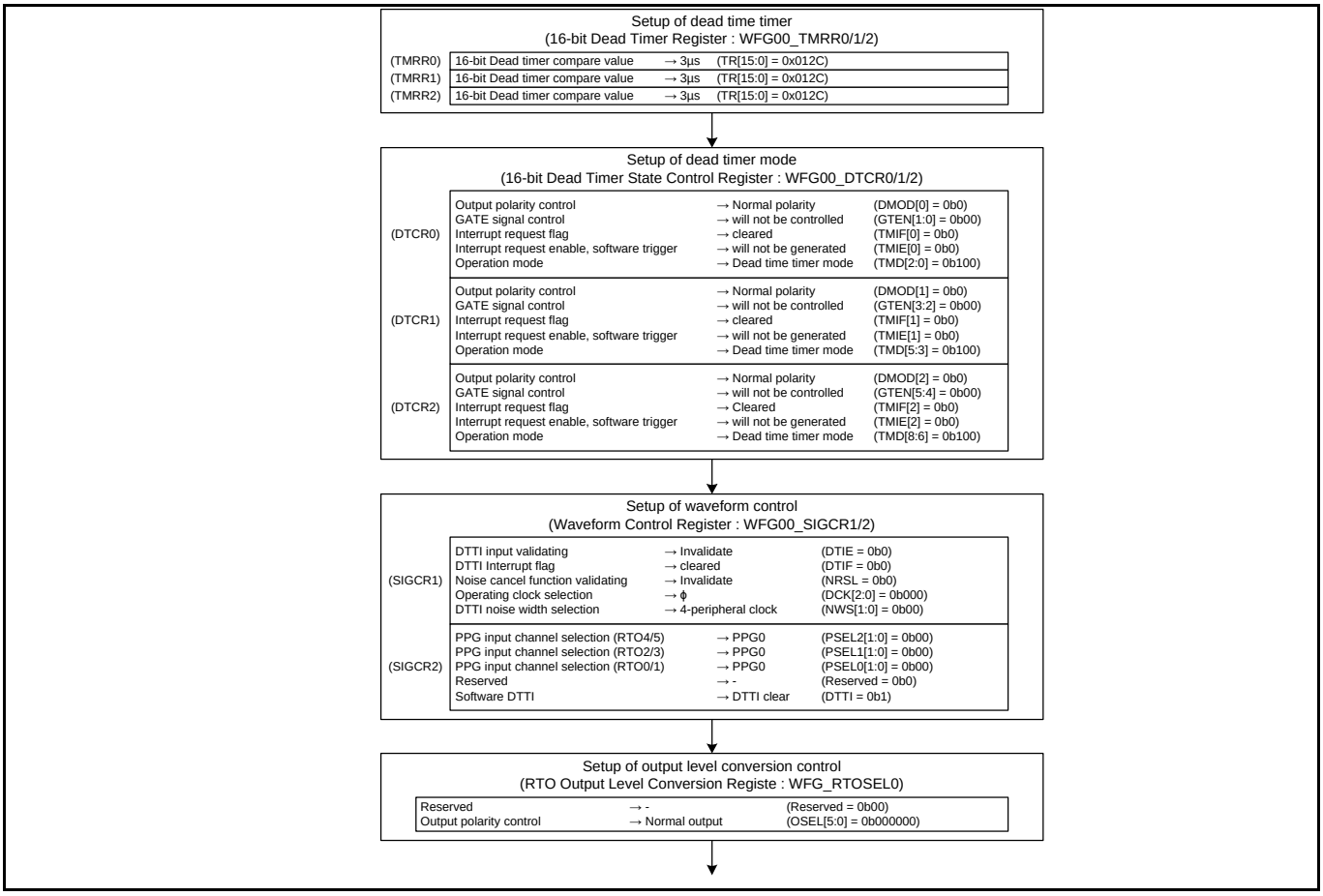
Figure 23. Setup Flow



The register used for a setup of a WFG is as follows. The example of a details setup is shown in Figure 24.

- WFGxx_TMRR0/1/2 : 16-bit Dead Timer Register (xx = 00,01,02,03)
- WFGxx_DTCR0/1/2 : 16-bit Dead Timer State Control Register (xx = 00,01,02,03)
- WFGxx_SIGCR1/2 : Waveform Control Register 1/2 (xx = 00,01,02,03)
- WFG_RTOSEL0 : RTO Output Level Conversion Register

Figure 24. Setup Example of WFG



5.2.2 Setup of 16-bit Dead Timer Register (WFGxx_TMRR0/1/2)

Dead time is set as WFGxx_TMRR0/1/2. When adding dead time of 3µs with a operation clock (CLK PERI4, 100 MHz), the setting value to WFGxx_TMRR0/1/2 can be computed as follows.

setting value = dead time count period
= 3µs ÷ 10ns
= 300
= 0x12C

5.2.3 Setup of 16-bit Dead Timer State Control Register (WFGxx_DTCR0/1/2)

The operation mode and polarity of output waveform of WFG is set to WFGxx_DTCR0/1/2.

Table 6. Setup Example of 16-bit Dead Timer State Control Register (WFGxx_DTCR0/1/2)

Bit	Bit Name		Setting Register		Bit Clear (WFGxx_ DTCRC0/1/2)	Bit Set (WFGxx_ DTCRS0/1/2)
			Value	Contents		
31	DMOD0	Output polarity control 0	0b0	Normal polarity	✓	✓
30, 29	GTEN[1:0]	GATE signal control 1/0	0b00	Will not be controlled	✓	✓
28	TMIF0	Interrupt request flag 0	0b0	Cleared	✓	-
27	TMIE0	Interrupt request enable, software trigger 0	0b0	Will not be generated	✓	✓
26-24	TMD[2:0]	Operation mode 2/1/0	0b100	Dead time timer mode	-	-
23	DMOD1	Output polarity control 1	0b0	Normal polarity	✓	✓
22, 21	GTEN[3:2]	GATE signal control 3/2	0b00	Will not be controlled	✓	✓
20	TMIF1	Interrupt request flag 1	0b0	Cleared	✓	-
19	TMIE1	Interrupt request enable, software trigger 1	0b0	Will not be generated	✓	✓
18-16	TMD[5:3]	Operation mode 5/4/3	0b100	Dead time timer mode	-	-
15	DMOD2	Output polarity control 2	0b0	Normal polarity	✓	✓
14, 13	GTEN[5:4]	GATE signal control 5/4	0b00	Will not be controlled	✓	✓
12	TMIF2	Interrupt request flag 2	0b0	Cleared	✓	-
11	TMIE2	Interrupt request enable, software trigger 2	0b0	Will not be generated	✓	✓
10-8	TMD[8:6]	Operation mode 8/7/6	0b100	Dead time timer mode	-	-

If WFGxx_DTCRC0/1/2 and WFGxx_DTCRS0/1/2 are used, the bit which wants to change a setup can be cleared/set individually. It is also possible to clear/set plurality simultaneously.

WFGxx_DTCRC0/1/2 clears a bit to 0b0 and WFGxx_DTCRS0/1/2 sets a bit to 0b1.

5.2.4 Setup of Waveform Control Register (WFGxx_SIGCR1/2)

Waveform Control Register 1/2 (WFGxx_SIGCR1/2) performs various setup shown in the following Table 7.

Table 7. Setup Example of Waveform Control Register 1 (WFGxx_SIGCR1)

Bit	Bit Name		Setting Register		Bit Clear (WFGxx_ SIGCR1C)	Bit Set (WFGxx_ SIGCR1S)
			Value	Contents		
23	DTIE	DTTI input validating	0b0	Invalidate	✓	✓
22	DTIF	DTTI Interrupt flag	0b0	Cleared	✓	-
21	NRSL	Noise cancel function validating	0b0	Invalidate	✓	✓
20-18	DCK[2:0]	Operating clock selection	0b000	ϕ (100MHz)	-	-
17, 16	NWS[1:0]	DTTI noise width selection	0b00	4-peripheral clock	-	-

If WFGxx_SIGCR1C and WFGxx_SIGCR1S are used, the bit which wants to change a setup can be cleared/set individually. It is also possible to clear / set plurality simultaneously.

WFGxx_SIGCR1C clears a bit to 0b0 and WFGxx_SIGCR1S sets a bit to 0b1.

Table 8. Setup Example of Waveform Control Register 2 (WFGxx_SIGCR2)

=Bit	Bit Name		Setting Register	
			Value	Contents
7, 6	PSEL2[1:0]	PPG input channel selection (RTO4/5)	0b00	PPG0
5, 4	PSEL1[1:0]	PPG input channel selection (RTO2/3)	0b00	PPG0
3, 2	PSEL0[1:0]	PPG input channel selection (RTO0/1)	0b00	PPG0
1	Reserved	Reserved	0b0	-
0	DTTI	Software DTTI	0b1	DTTI clear

There is no register which clears / sets each bit of WFGxx_SIGCR2.

5.2.5 Setup of RTO Output Level Conversion Register (WFG_RTOSEL0)

Please use this register to reverse PWM waveform output individually.

Table 9. Setup Example of RTO Output Level Conversion Register (WFG_RTOSEL0)

Bit	Bit Name		Setting Register	
			Value	Contents
31, 30	Reserved	Reserved	0b00	-
29-24	OSEL[5:0]	Output polarity control	0b000000	Normal output

Note: A setup of this register is applied immediately. Please be careful.

6 12-bit 4ch A/D Converter (4ch-SH ADC)

4ch-SH ADC is successive approximation type A-D converter. 4ch-SH ADC samples simultaneously the analog input voltage of 4ch at the maximum, and changes into the serial digital value of 12 bits.

4ch-SH ADC takes in the three phase current used by Motor control.

This section explains how the A/D conversion is started when a 16-bit FRT value is the same as comparison value, and this section explains how to take in conversion data.

6.1 Overview

The setup of the 4ch-SH ADC is described below.

6.1.1 A/D Converter

4ch-SH ADC is successive approximation type A-D converter, and changes the voltage of Analog input terminal into a digital signal. Analog input terminal can be used to 4ch at the maximum by a program.

After an AD conversion finishes, conversion data is stored in a data register for every channel, and end interrupt of A/D conversion can be generated. An error flag is also stored in a data register. Thereby, the state of A/D conversion data can be checked.

6.1.2 Activation Request Control and Arbitration of A/D Converter

4ch-SH ADC converters are started by one demand (activation request) of software activation, an external trigger, base timer, and comparison match (comparison coincidence with 16-bit FRT). Activation request is managed per unit.

If contention arises between Activation Requests, A/D activation arbitration controls their priority. The order of priority is the lowest activation group number is first (priority control by group number) and compare match > external trigger/base timer > software activation (priority control by activation factor).

The suspended activation factor is again arbitrated after the end of conversion of activation request with a high priority.

6.1.3 Data Protection Function

The data protection function can be configured for A/D data register. When data protection is enabled, the data protection function masks an A/D activation request until the data in the A/D data register is read and an interrupt flag is cleared. Also, it is possible to select whether to include the clearing of the interrupt flag as a protection condition.

The data protection function is enabled after conversion ends in all channels that had ongoing conversions.

6.1.4 Forced Termination of Activation Request

The current A/D activation request or conversion can be forced to terminate by writing 0b1 to the A/D activation request clear bit (ADTSC[n]:BUSYC).

6.1.5 Range Comparison Function

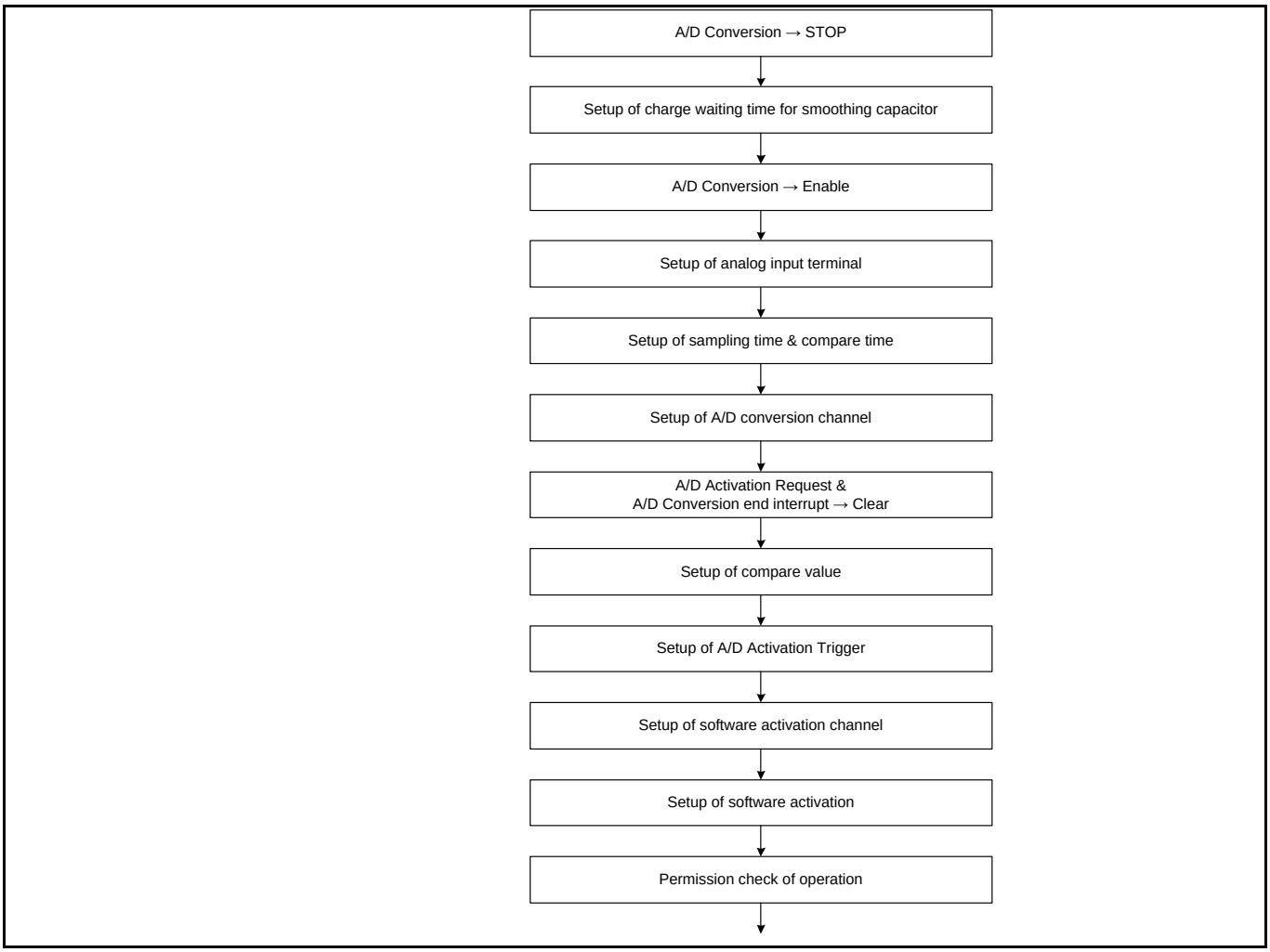
This function compares A/D conversion result with an upper and lower limit threshold value (range comparison). As a comparative result, above upper-limit threshold value and below lower-limit threshold value are detectable. An upper and lower limit threshold value chooses one from four kinds of upper and lower limit threshold value setting.

6.2 Details of Setup

6.2.1 Setup Procedure Example

The setup flow of the 4ch-SH ADC is as below.

Figure 25. Setup Flow

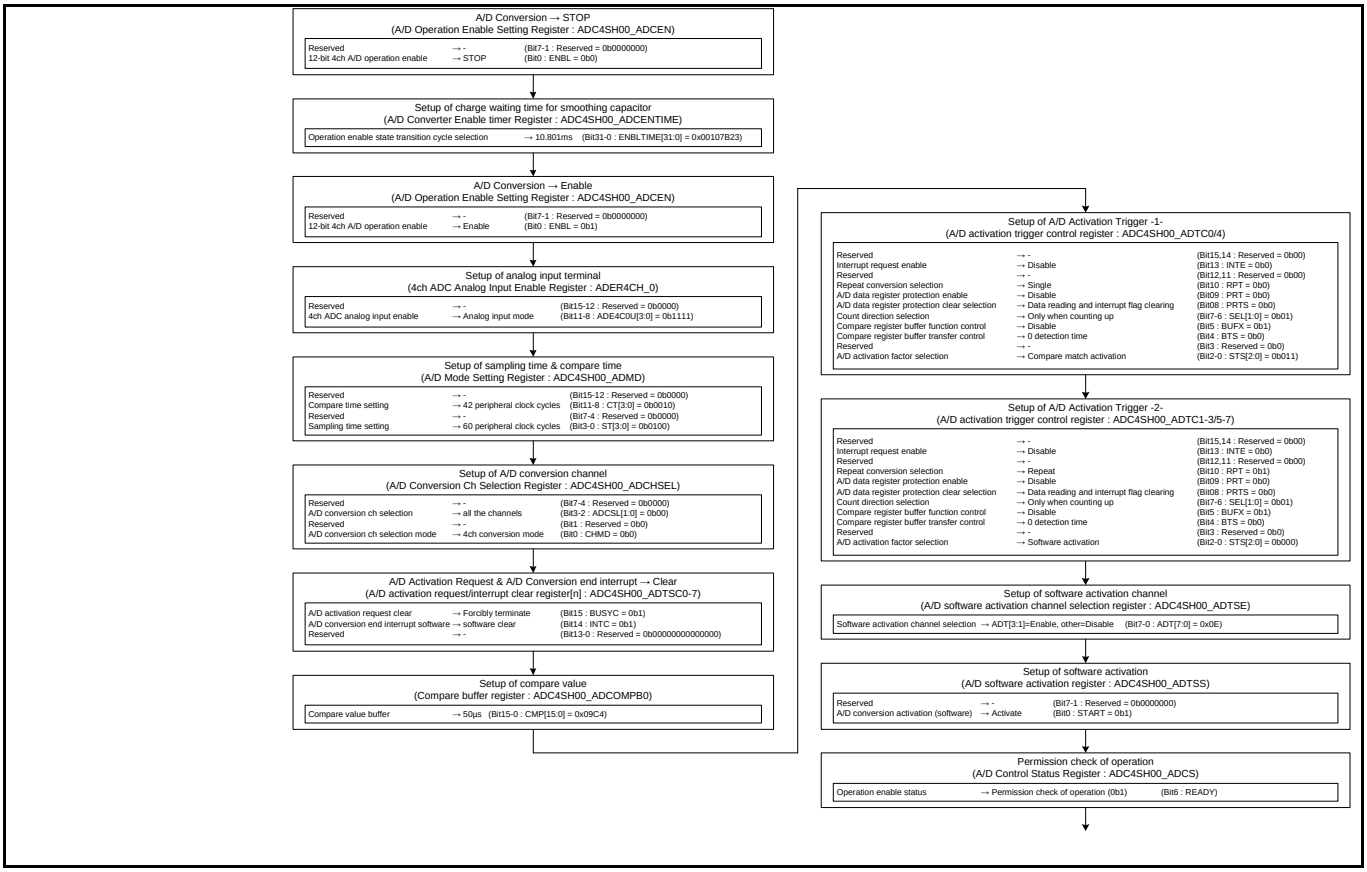


The register used for a setup of a 4ch-SH ADC is as follows. The example of a details setup is shown in Figure 25.

- ADC4SHxx_ADCEN : A/D Operation Enable Setting Register
- ADC4SHxx_ADCS : A/D Control Status Register
- ADER4CH_0 : 4ch ADC Analog Input Enable Register
- ADC4SHxx_ADMD : A/D Mode Setting Register
- ADC4SHxx_ADCHSEL : A/D Conversion Channel Selection Register
- ADC4SHxx_ADTSC[n] : A/D Activation Request/Interrupt Clear Register[n]
- ADC4SHxx_ADTC[n] : A/D Activation Trigger Control Register[n]
- ADC4SHxx_ADCENTIME : A/D Converter Enable Timer Register
- ADC4SHxx_ADCOMPB[n] : Compare Buffer Register[n]
- ADC4SHxx_ADTSE : A/D Software Activation Channel Selection Register
- ADC4SHxx_ADTSS : A/D Software Activation Register

(xx = 00/01, n = 0 - 7)

Figure 26. Setup Example of 4ch-SH ADC



Note:

ADC4SH00_ADTSC0-7 : Please set up all the registers (×8).

ADC4SH00_ADTC0 / 4 : Please set up all the registers (×2).

ADC4SH00_ADTC1-3 / 5-7 : Please set up all the registers (×6).

6.2.2 Setup of A/D Operation Enable Setting Register (ADC4SHxx_ADCEN)

The A/D operation enable setting register (ADC4SHxx_ADCEN) enables 4ch-SH ADC converter operation. Be sure that the 12-bit 4ch A/D operation enable bit (ENBL) is rewritten before the conversion operation while A/D operations are stopped (ADCS : BUSY is 0b0).

Table 10. Setup Example of A/D Operation Enable Setting Register (ADC4SHxx_ADCEN)

Bit	Bit Name		Setting Register	
			Value	Contents
7-1	Reserved	Reserved	0b0000000	-
0	ENBL	12-bit 4ch A/D operation enable	0b0 0b1	Stop operation Enable operation

6.2.3 Setup of A/D Control Status Register (ADC4SHxx_ADCS)

The A/D control status register (ADC4SHxx_ADCS) indicates that A/D conversion is in operation or has stopped.

Table 11. Sate of A/D Control Status Register (ADC4SHxx_ADCS[n])

Bit	Bit Name		Contents
7	BUSY	A/D conversion busy	0 : Stop, 1 : Activation until the end of conversion
6	READY	Operation enable status	0 : Stop, 1 : Enable

6.2.4 Setup of 4ch ADC Analog Input Enable Register (ADER4CH_0/1)

The 4ch ADC analog input enable registers (ADER4CH_1, ADER4CH_0) are registers that control 4ch-SH ADC analog input terminal.

In models equipped with a key code function, a key code setting is required for writing to this register. For details on which models have the key code function, see Model Options in the Data Sheet.

Table 12. Setup Example of 4ch ADC Analog Input Enable Register (ADER4CH_0)

Bit	Bit Name		Setting Register	
			Value	Contents
7-4	Reserved	Reserved	0b0000	-
3-0	ADE4C0U[3:0]	4ch ADC analog input enable	0b1111	Analog input mode

6.2.5 Setup of A/D Mode Setting Register (ADC4SHxx_ADMD)

The A/D conversion time of is the sum total of sampling time and compare time. Sampling time is the time when an electric charge is accumulated in an internal capacitor by the voltage impressed to an analog input terminal. Compare time is the time when the electric charge accumulated in the capacitor is changed into digital data by the internal comparator. Refer to the electrical property of a datasheet for the minimum time/maximum time of sampling time and compare time.

Sampling time and compare time are decided by the register setting value and the input clock. An example is shown below.

Table 13. Setup Example of A/D Mode Setting Register (ADC4SHxx_ADMD)

Bit	Bit Name		Setting Register	
			Value	Contents
15-12	Reserved	Reserved	0b0000	-
11-8	CT[3:0]	Compare time setting	0x0010	1680ns
7-4	Reserved	Reserved	0b0000	-
3-0	ST[3:0]	Sampling time setting	0x0100	600ns

6.2.6 Setup of A/D Conversion Channel Selection Register (ADC4SHxx_ADCHSEL)

The A/D conversion channel selection register (ADCHSEL) sets the number of A/D conversion channels.

Table 14. Setup Example of A/D Conversion Channel Selection Register (ADC4SHxx_ADCHSEL)

Bit	Bit Name		Setting Register	
			Value	Contents
7-4	Reserved	Reserved	0b0000	-
3,2	ADCSL[1:0]	A/D conversion channel selection	0b00	All the channels
1	Reserved	Reserved	0b0	-
0	CHMD	A/D conversion channel selection mode	0b0	A/D 4ch conversion mode

6.2.7 Setup of A/D Activation Request/Interrupt Clear Register[n] (ADC4SHxx_ADTSC[n])

Each A/D activation request/interrupt clear register (ADTSC[n]) is used to forcibly terminate A/D activation requests and to clear the A/D conversion end interrupt request flag.

Table 15. Setup Example of A/D Activation Request/Interrupt Clear Register[n] (ADC4SHxx_ADTSC[n])

Bit	Bit Name		Setting Register	
			Value	Contents
15	BUSYC	A/D activation request clear	0b1	Forcibly terminate
14	INTC	A/D conversion end interrupt software clear	0b1	Perform a software clear
13-0	Reserved	Reserved	0b00000000000000	-

6.2.8 Setup of A/D Activation Trigger Control Register[n] (ADC4SHxx_ADTC[n])

Each A/D activation trigger control register (ADTC[n]) enables/disables interrupt requests, selects an activation factor, selects a conversion mode, controls protection function, selects a compare value for use in compare operations, and controls a compare value buffer.

Table 16. Setup Example of A/D Activation Trigger Control Register[n] (ADC4SHxx_ADTC0/4)

Bit	Bit Name		Setting Register	
			Value	Contents
15, 14	Reserved	Reserved	0b00	-
13	INTE	Interrupt request enable	0b0	Disable
12, 11	Reserved	Reserved	0b00	-
10	RPT	Repeat conversion selection	0b0	Single conversion mode
9	PRT	A/D data register protection enable	0b0	Disable
8	PRTS	A/D data register protection clear selection	0b0	Data reading and interrupt flag clearing
7, 6	SEL[1:0]	Count direction selection	0b01	Only when counting up
5	BUFX	Compare register buffer function control	0b1	Disable
4	BTS	Compare register buffer transfer control	0b0	0 detection time
3	Reserved	Reserved	0b0	-
2-0	STS[2:0]	A/D activation factor selection	0b011	Compare match activation

Table 17. Setup Example of A/D Activation Trigger Control Register[n] (ADC4SHxx_ADTC1-3 / 5-7)

Bit	Bit Name		Setting Register	
			Value	Contents
15, 14	Reserved	Reserved	0b00	-
13	INTE	Interrupt request enable	0b0	Disable
12, 11	Reserved	Reserved	0b00	-
10	RPT	Repeat conversion selection	0b1	Repeat conversion mode
9	PRT	A/D data register protection enable	0b0	Disable
8	PRTS	A/D data register protection clear selection	0b0	Data reading and interrupt flag clearing
7, 6	SEL[1:0]	Count direction selection	0b01	Only when counting up
5	BUFX	Compare register buffer function control	0b1	Disable
4	BTS	Compare register buffer transfer control	0b0	0 detection time
3	Reserved	Reserved	0b0	-
2-0	STS[2:0]	A/D activation factor selection	0b000	Software activation

Note: About RPT / STS[2:0]

When you A/D conversion by activation channel 0 or 4, please set up RPT and STS[2:0] as follows.

Note: RPT : Repeat conversion mode

Note: STS[2:0] : Software activation

6.2.9 Setup of A/D Converter Enable Timer Register (ADC4SHxx_ADCENTIME)

The A/D converter cannot immediately operate after power on. Please wait until the smoothing capacitor (C_{REF}) connected to an external terminal is charged. The time (start-up time) until charge is completed is as follows. Please refer to the Electrical Characteristics 2.Recommended operating conditions of a datasheet.

$$\text{start-up time} = 9 \times C_{REF} \times 1.2k + 1\mu \quad [s]$$

When C_{REF} is set to 1µF (maximum), start-up time becomes the following. (tolerance of capacitance ignores).

$$\text{start-up time} = 9 \times 1\mu F \times 1.2k + 1\mu = 10.801 \quad [ms]$$

Please set start-up time to this register. If ENBL bit 0b1 of ADCEN register is written, the down-count which makes the value of this register an initial value will begin. The RDY bit of AD register is set to 0b1 after the end of a down-count, and it is shown that it can operate. Please be sure to perform this operation after power on.

When waiting for the start-up time with a clock (CLK PERI4, 100 MHz), the setting value of this register can be computed as follows.

$$\begin{aligned}\text{setting value} &= \text{number of down-count} - 1\\ &= (10.801ms \div 10ns) - 1\\ &= 1{,}080{,}100 - 1 = 1{,}080{,}099\\ &= 0x107B23\end{aligned}$$

6.2.10 Setup of Compare Buffer Register[n] (ADC4SHxx_ADCOMPB[n])

The register which sets up a compare value has two register of a compare register and a compare buffer register.

When a compare buffer function is disabled, the value written in the compare buffer register is immediately reflected in a compare register.

When a compare buffer function is enabled, the value written in the compare buffer register is transmitted to a comparison register to the specified timing.

Note: Compare buffer function setup : Refer to the BUFX of A/D activation trigger control register[n].

Compare register transfer timing : Refer to the BTS of A/D activation trigger control register[n].

6.2.11 Setup of A/D Software Activation Channel Selection Register (ADC4SHxx_ADTSE) and A/D Software Activation Register (ADC4SHxx_ADTSS)

A/D software activation channel selection register and A/D software activation register as follows.

Table 18. Setup Example of A/D Software Activation Channel Selection Register (ADC4SHxx_ADTSE)

Bit	Bit Name		Setting Register	
			Value	Contents
7-0	ADT[7:0]	Software activation channel selection	0x0E	ch[3:1] : Enable other : Disable

Table 19. Setup Example of A/D Software Activation Register (ADC4SHxx_ADTSS)

Bit	Bit Name		Setting Register	
			Value	Contents
7-1	Reserved	Reserved	0b0000000	-
0	START	A/D conversion activation (software)	0b1	Activate A/D conversion

7 R/D Converter (RDC)

The RDC generates excitation signal for resolvers, and detection of motor angle/motor angular velocity used by vector control in motor control. This section explains the setting method for controlling them.

7.1 Overview

The setup of the RDC is described below.

7.1.1 Resolver Excitation Signal Output

The RDC outputs the signal which magnetizes a resolver. The output frequency can choose 10 kHz and 20 kHz.

7.1.2 Angular / Angular Velocity Detection

The RDC convert a resolver response signal into a digital signal, and detects 12-bit angle data (θ_{org}) and 16-bit angular velocity data (ω_{org}).

RDC can also output the following calculation result, after detecting θ_{org} and ω_{org}.

- initial phase addition
- sine/cosine conversion
- lead angle correction

Initial Phase Addition

An initial phase is added to the angle data (θ_{org}) which a converter detects.

$$\theta = n \times \theta org + \delta$$

(n : The ratio of a resolver electric angle and a motor electric angle.)

An angle θ (synchronous angle) is kept synchronizing with 4ch-SH ADC starting timing which detects three phase current.

Sine Cosine Conversion

The R/D converter calculates sin θ and cos θ for the angle θ that is written in the sine/cosine conversion input register (RDCxx_SCCIR). The converted values are stored in the 32-bit sine data register (RDCxx_SINDR) and cosine data register (RDCxx_COSDR). The values are 32-bit floating-point numbers in the format compliant with IEEE754.

Lead Angle Correction

In order to calculate three-phase to two-phase conversion and two-phase to three-phase conversion, the value of sin θ and cos θ for the motor rotation angle θ is needed. However, the motor is rotating also during this conversion. Therefore, a difference occurs at an angle. The difference of this rotation angle is called lead angle correction (Δθ). At MB9D560, sin θ, cos θ, sin Δθ, and cos Δθ, are calculated by hardware. Thereby, lead angle correction can be compensation.

7.1.3 Anomaly Detection with Resolver

RDC can detect the following abnormalities and can notifies NMI.

- A/D converter error
- Frequency error in the excitation signal
- Offset amount error in the secondary coil of the resolver
- Ground fault of the secondary coil of the resolver
- Line break in the secondary coil of the resolver
- Amplitude error in the resolver response signal
- Tracking loop error

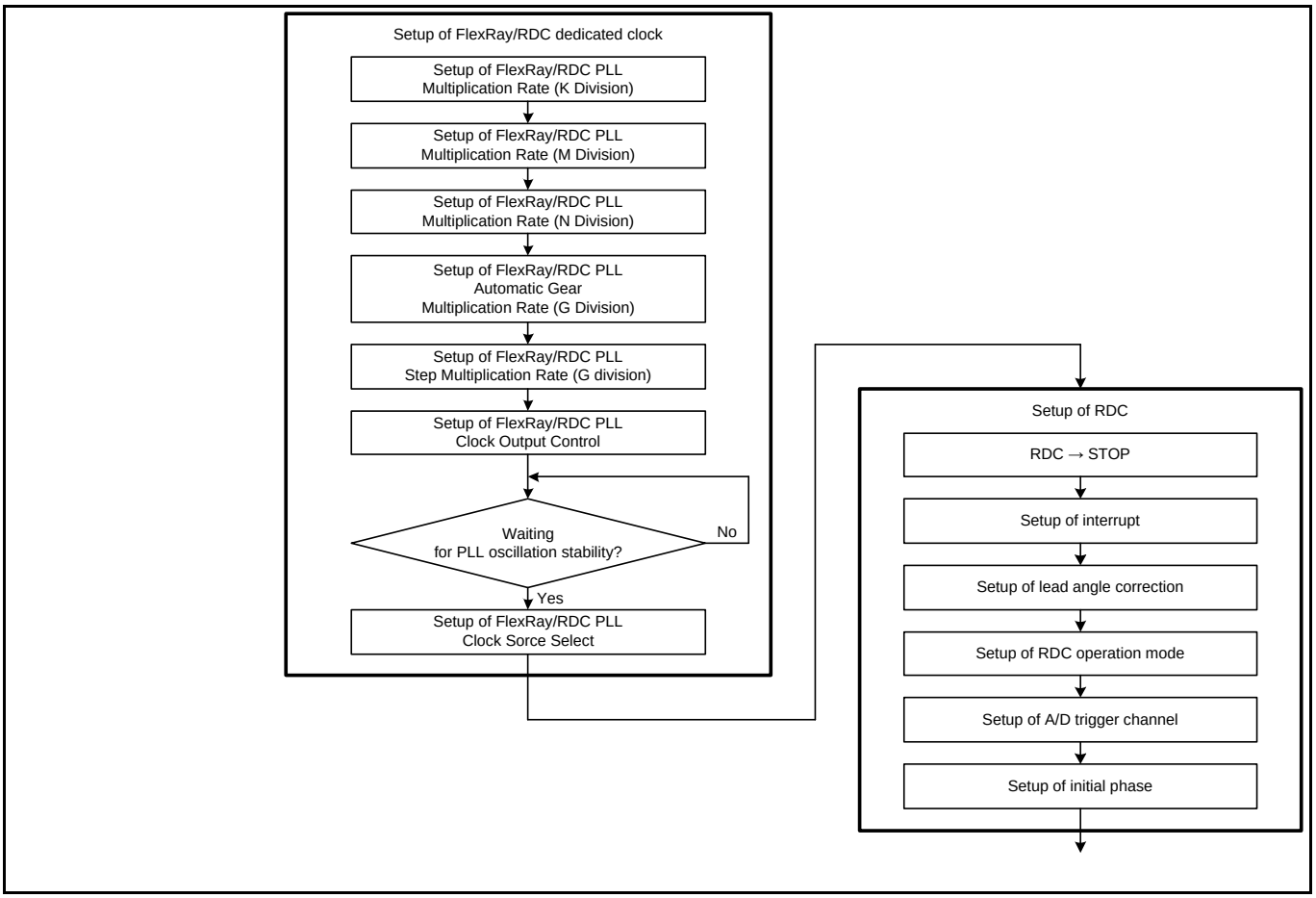
Anomaly detections may be detected after permitting RDCEN bit of RDC Operation Control Register 1 (RDCxx_RDCCTR1) until a resolver response signal is stabilized.

7.2 Details of Setup

7.2.1 Setup Procedure Example

The setup flow is as below.

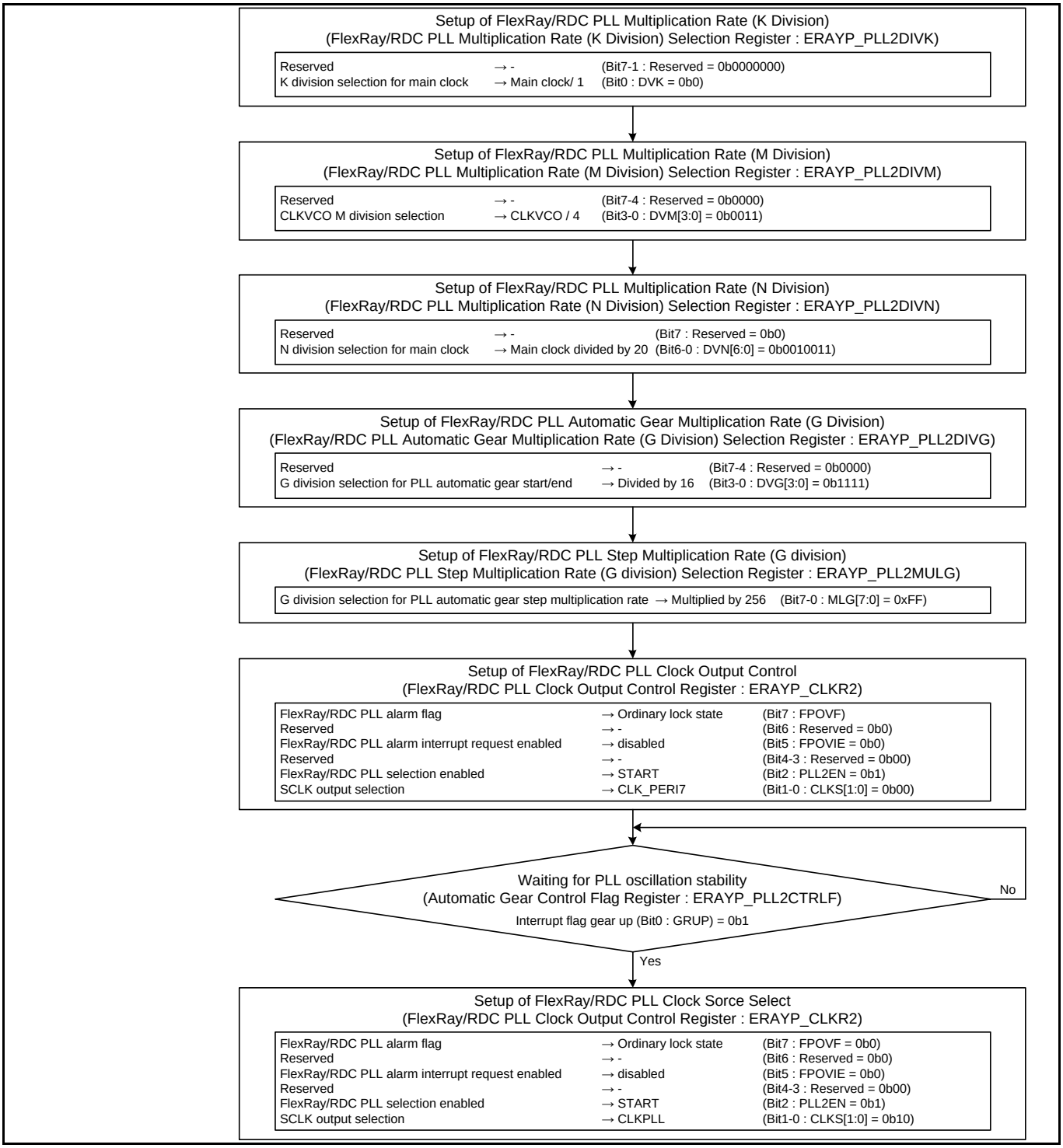
Figure 27. Setup Flow



The register used for a setup of a RDC is as follows. The example of a details setup is shown in Figure 27 and Figure 28.

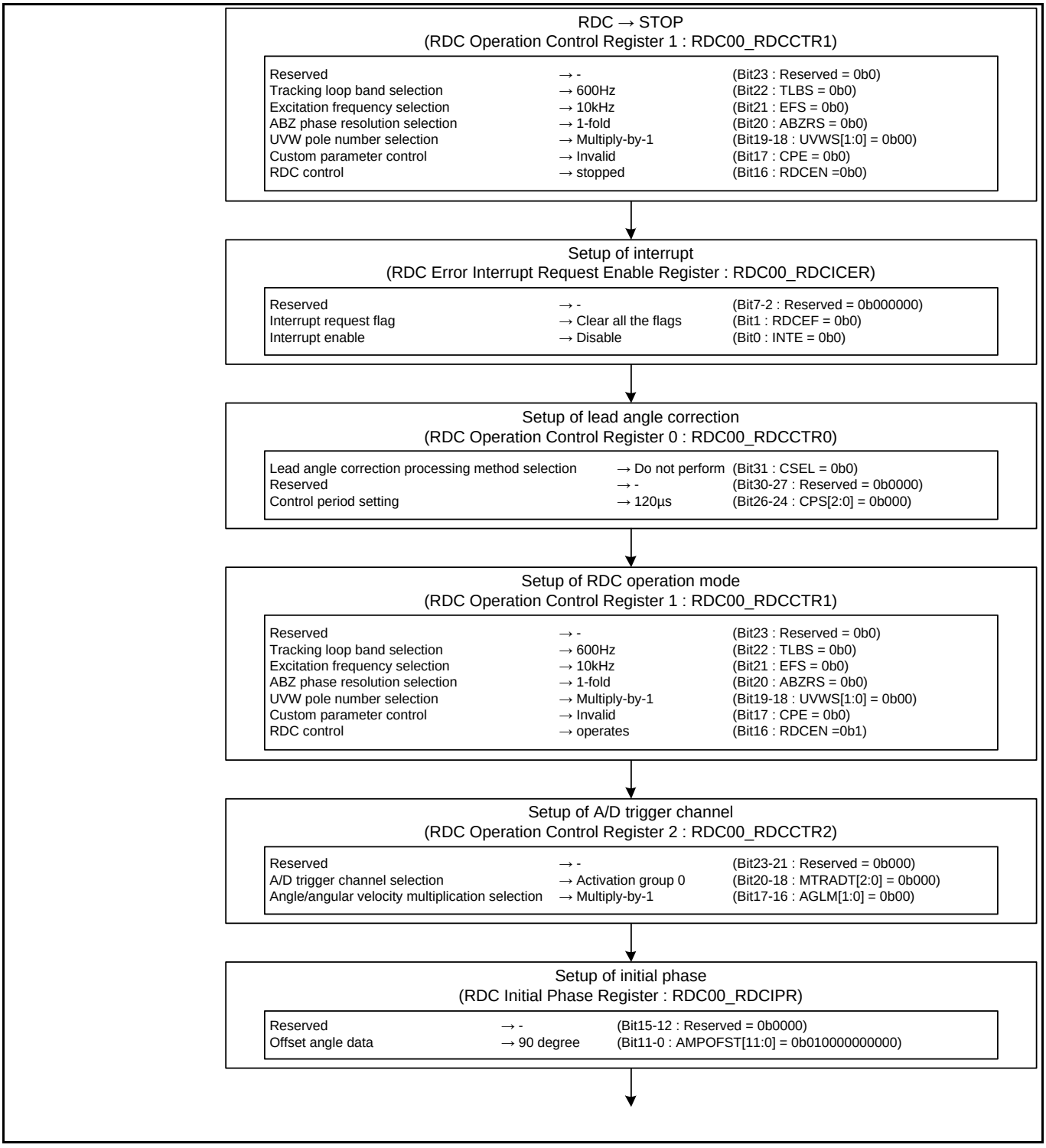
- ERAYP_PLL2DIVK : FlexRay/RDC PLL Multiplication Rate (K Division) Selection Register
- ERAYP_PLL2DIVM : FlexRay/RDC PLL Multiplication Rate (M Division) Selection Register
- ERAYP_PLL2DIVN : FlexRay/RDC PLL Multiplication Rate (N Division) Selection Register
- ERAYP_PLL2DIVG : FlexRay/RDC PLL Automatic Gear Multiplication Rate (G Division) Selection Register
- ERAYP_PLL2MULG : FlexRay/RDC PLL Step Multiplication Rate (G division) Selection Register
- ERAYP_CLKR2 : FlexRay/RDC PLL Clock Output Control Register
- ERAYP_PLL2CTRLF : Automatic Gear Control Flag Register
- RDCxx_RDCCTR0 : RDC Operation Control Register 0 (xx = 00/01)
- RDCxx_RDCCTR1 : RDC Operation Control Register 1 (xx = 00/01)
- RDCxx_RDCCTR2 : RDC Operation Control Register 2 (xx = 00/01)
- RDCxx_RDCIPR : RDC Initial Phase Register (xx = 00/01)
- RDCxx_RDCICER : RDC Error Interrupt Request Enable Register (xx = 00/01)

Figure 28. Setup Example of FlexRay/RDC Dedicated Clock



Note: The above figure is an example in the case of outputting an 80 MHz clock to RDC, when 16 MHz is inputted into main clock.

Figure 29. Setup Example of RDC

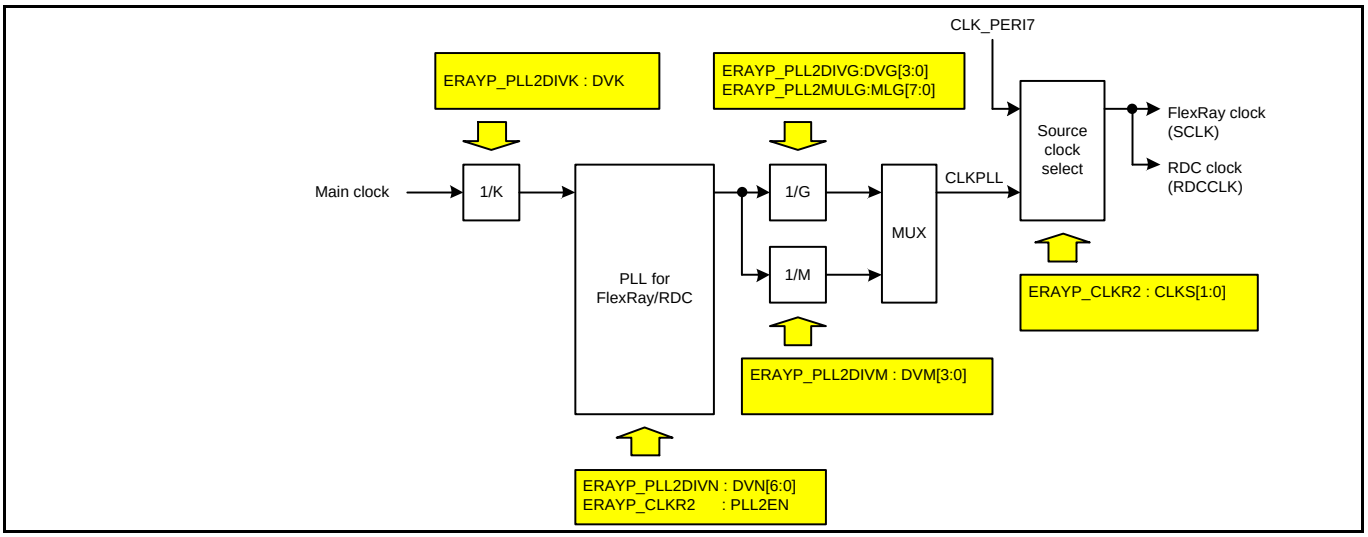


7.2.2 Setup of FlexRay/RDC Dedicated Clock

The R/D converter operates with an 80 MHz clock. In order to generate 80 MHz clock, MB9D560 embedded the FlexRay/RDC dedicated clock module. Please generate a clock by the FlexRay/RDC dedicated clock module and supply 80 MHz clock to R/D converter.

R/D converter divides an 80 MHz clock into two, and operates at 40 MHz.

Figure 30. Block Diagram



Setup of a Dividing Ratio (ERAYP_PLL2DIVK / ERAYP_PLL2DIVM / ERAYP_PLL2DIVN)

When a clock is 16 MHz, the setup for supplying an 80 MHz clock to R/D converter is as follows.

Table 20. Setup Example of Dividing Ratio (Main clock = 16 MHz, RDCCLK = 80 MHz)

Main Clock (MCLK)	ERAYP_PLL2DIVK	ERAYP_PLL2DIVN	ERAYP_PLL2DIVM	FlexRay/RDC Clock (SCLK/RDCCLK)
	DVK	DVN[6:0]	DVM[3:0]	
16 MHz	0 (×1/1)	0b001_0011 (×20)	0b0011 (×1/4)	80 MHz

Note: Please use the output frequency of PLL within the limits of a maximum/minimum.

200 MHz ≤ output frequency of PLL ≤ 400 MHz

Note: In the above setup example, output frequency changes as follows

×1/1 (16 MHz) → ×20 (320 MHz) → ×1/4 (80 MHz)

Setup of Clock Automatic Gear

When the output frequency of a clock is increased rapidly, power supply voltage may drops. Clock automatic gear is used in order to avoid a voltage drop.

FlexRay/RDC PLL Automatic Gear Multiplication Rate (G Division) Selection Register (ERAYP_PLL2DIVG)

A multiplication rate of a clock automatic gear is chosen.

Table 21. Setup Example of ERAYP_PLL2DIVG

Bit	Bit Name		Setting Register	
			Value	Contents
7-4	Reserved	Reserved	0b0000	-
3-0	DVG[3:0]	G division selection for PLL automatic gear start/end	0b1111	Divided by 16

FlexRay/RDC PLL Step Multiplication Rate (G division) Selection Register (ERAYP_PLL2MULG)

A step multiplication rate of a clock automatic gear is chosen.

Table 22. Setup Example of ERAYP_PLL2MULG

Bit	Bit Name		Setting Register	
			Value	Contents
7-0	MLG[7:0]	G division selection for PLL automatic gear step multiplication rate	0xFF	Multiplied by 256

Automatic Gear Control Flag Register (ERAYP_PLL2CTRLF)

When clock automatic gear up (a clock frequency is increased), please check a state in GRUP bit.

Table 23. Setup Example of ERAYP_PLL2CTRLF

Bit	Bit Name		Setup of Register
7-3	Reserved	Reserved	-
2	IEDN	Interrupt flag gear down	0 : Gear down interrupt inactive 1 : Gear down interrupt active
1	Reserved	Reserved	-
0	GRUP	Interrupt flag gear up	0 : Gear up interrupt inactive 1 : Gear up interrupt active

Setup of FlexRay/RDC PLL Clock Output Control Register (ERAYP_CLKR2)

This register performs a setup of operation for a RDCCLK output.

Table 24. Setup Example of ERAYP_CLKR2

Bit	Bit Name		Setting Register	
			Value	Contents
7	FPOVF	FlexRay/RDC PLL alarm flag	Don't Care (Read Only)	-
6	Reserved	Reserved	0b0	-
5	FPOVIE	FlexRay/RDC PLL alarm interrupt request enabled	0b0	Disabled
4,3	Reserved	Reserved	0b0	-
2	PLL2EN	FlexRay/RDC PLL selection enabled	0b0 → 0b1	Stop → Start
1,0	CLKS[1:0]	SCLK output selection	0b00 → 0b10	CLK_PERI7 → CLKPLL

Note: It is prohibition to change PLL2EN bit, when CLKPLL is chosen as clock source (CLKS[1:0] = 0b10).

7.2.3 Setup of R/D Converter

Setup of RDC Operation Control Register 0 (RDCxx_RDCCTR0)

This register can be used to select a method for lead angle correction processing and select a control period.

Table 25. Setup Example of RDC Operation Control Register 0 (RDCxx_RDCCTR0)

Bit	Bit Name		Setting Register	
			Value	Contents
31	CSEL	Lead angle correction processing method selection	0b0	Do not perform
30-27	Reserved	Reserved	0b0000	-
26-24	CPS[2:0]	Control period setting	0b000	120µs

Setup of RDC Operation Control Register 1 (RDCxx_RDCCTR1)

This register is used to set the operating mode of the R/D converter.

Table 26. Setup Example of RDC Operation Control Register 1 (RDCxx_RDCCTR1)

Bit	Bit Name		Setting Register	
			Value	Contents
23	Reserved	Reserved	0b0	-
22	TLBS	Tracking loop band selection	0b0	600 Hz
21	EFS	Excitation frequency selection	0b0	10 kHz
20	ABZRS	ABZ phase resolution selection	0b0	1-fold
19-18	UVWS[1:0]	UVW pole number selection	0b00	Multiply-by-1
17	CPE	Custom parameter control	0b0	Invalid
16	RDCEN	RDC control	0b1	Operates

Note: Tracking loop is the tracking interpolation arithmetic operation processing which a converter performs. Tracking loop can choose two kinds modes of 600 Hz and 1800 Hz.

Note: R/D converter starts operation by setting RDCEN bit to 0b1. When you make it stop, please set it 0b0.

Setup of RDC Operation Control Register 2 (RDCxx_RDCCTR2)

The angle (θ) and angular velocity (ω) which R/D converter outputs are synchronized with A/D activation triggers. Also, a multiplication rate of an angle (θ) and angular velocity (ω) is set up.

Table 27. Setup Example of RDC Operation Control Register 2 (RDCxx_RDCCTR2)

Bit	Bit Name		Setting Register	
			Value	Contents
23-21	Reserved	Reserved	0b000	-
20-18	MTRADT[2:0]	A/D trigger channel selection	0b000	Activation group 0
17-16	AGLM[1:0]	Angle/angular velocity multiplication selection	0b00	Multiply-by-1

Setup of RDC Initial Phase Register (RDCxx_RDCIPR)

The offset value added to the angle which R/D converter output is set up.

Table 28. RDC Initial Phase Register (RDCxx_RDCIPR)

Bit	Bit Name		Setting Register	
			Value	Contents
15-12	Reserved	Reserved	0b0000	-
11-0	AMPOFST[11:0]	Offset angle data	0b010000000000	90 [degree]

Note: Please set the offset value of a motor to the offset angle data.

Setup of RDC Error Interrupt Request Enable Register (RDCxx_RDCICER)

Interrupt when R/D converter detects an anomaly condition is set up. Also, the anomaly condition flag is cleared.

Table 29. Setup Example of RDC Error Interrupt Request Enable Register (RDCxx_RDCICER)

Bit	Bit Name		Setting Register	
			Value	Contents
7-2	Reserved	Reserved	0b000000	-
1	RDCEF	Interrupt request flag	0b0	Clear all the flags
0	INTE	Interrupt enable	0b0	Disable error interrupts

8 Appendix

8.1 Relevant Unit for Three-phase Motor Control

Block diagram and channel number of associated unit for three-phase motor control in MB9D560 Series is shown below.

Figure 31. Block Diagram

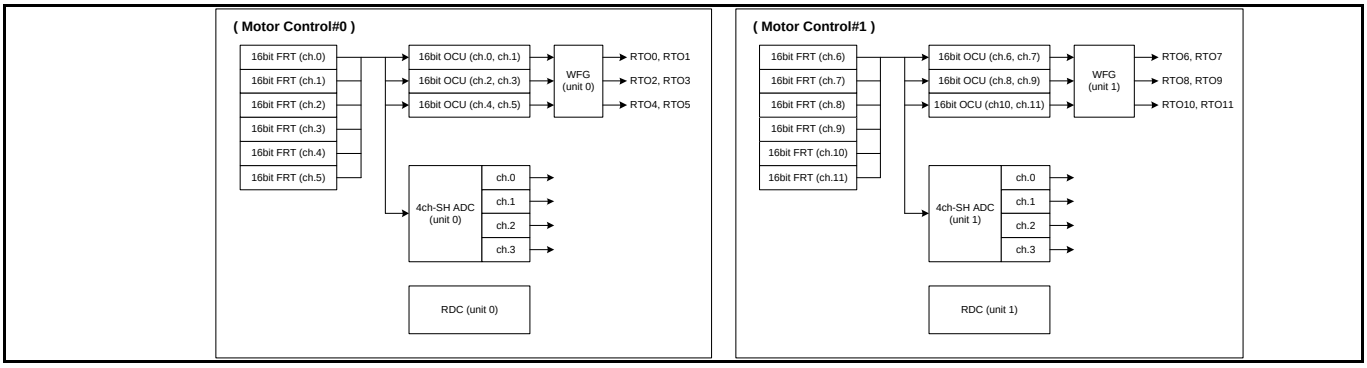


Table 30. Assignment and Channel Number of Unit

Unit	Channel Number	Assignment		Remarks
16-bit free-run timer (16-bit FRT)	20 ch	ch.0 - ch.5 ch.6 - ch.11	: For Motor Control #0 control : For Motor Control #1 control	Used for activation timing and interrupt signal generation of each unit
		ch.12 - ch.19	: For other control	-
16-bit output compare (16-bit OCU)	24 ch	ch.0 - ch.5 ch.6 - ch.11	: For Motor Control #0 control : For Motor Control #1 control	Generate PWM waveform
		ch.12 - ch.23	: For other control	-
Waveform generator (WFG)	4 unit (24ch)	unit 0 unit 1	: For Motor Control #0 control : For Motor Control #1 control	Add the dead time
		unit 2, 3	: For other control	-
12-bit 4ch A/D converter (4ch-SH ADC)	2 unit (8ch)	unit 0 unit 1	: For Motor Control #0 control : For Motor Control #1 control	Obtain current for three-phase
R/D converter (RDC)	2 unit	unit 0 unit 1	: For Motor Control #0 control : For Motor Control #1 control	Detect angle and angular velocity

8.2 Abbreviations

This section explains abbreviations about MB9D560 Series.

Table 31. Abbreviations about MB9D560 Series

Abbreviations	Meaning
CLK_PERI4 CLK_PERI5	CLK_PERI4 : Peripheral clock for Motor Control unit 0 CLK_PERI5 : Peripheral clock for Motor Control unit 1
PLL	Phase Locked Loop
PPG	Programmable Pulse Generator
PWM	Pulse Width Modulation
RDC	Resolver Digital Converter
WFG	Wave Form Generator

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**	_	HIHA	01/30/2015	Initial release
*A	5037939	HIHA	12/04/2015	Converted Spansion Application Note “MB9D560_AN708-00002” to Cypress format
*B	5872522	AESATP12	09/05/2017	Updated logo and copyright.
*C	6038268	YOST	01/19/2018	Updated the Cypress logo, Sales information and legal. Completing Sunset Review.

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