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AN205492

FCR4, FCR4 Cluster Series, Boundary Scan

The FCR4 based MCU offering boundary scan possibility for PCB test purposes via the Arm® CoreSight™ debug interface. This application Note is briefly describing the settings. The FCR4 series MCU supporting a 5-pin IEEE 1149.1 JTAG interface. For each series a boundary file (*.bsdl) is offered.

1 Introduction

The Cypress Arm® Cortex®-R4 (FCR4) based MCU offering boundary scan possibility for PCB test purposes via the Arm CoreSight™ debug interface. This application Note is briefly describing the settings.

2 Boundary Scan

This chapter list additional information for boundary scan mode

The FCR4 series MCU supporting a 5-pin IEEE 1149.1 JTAG interface. For each series a boundary file (*.bsdl) is offered. Contact Cypress to receive the file. See bsdl file or device specific datasheet for available instructions. Information about the JTAG hardware connection is available in application note mcu-an-300176-e-vxx-fcr4_hardware_setup.pdf. While ARM® CoreSight debug interface ports (AHB-AP and APB-AP) can be used for debug purposes, a Cypress implementation is used for boundary scan via Test Access Port (TAP).

2.1 Entering boundary scan mode

There exist two options to enter boundary scan mode.

- Via User mode
- Via board test mode

2.1.1 Enter boundary scan via User mode

Using this method no level at any pin has to be changed compared to Application setting.

The MODE pin stays connected to GND. At the Debug access port (DAP) the memory access port (MEM-AP) is active at JTAG pin interface. To enter boundary scan mode the Test Access Port (TAP) needs to be activated. This is done by accessing the MCFG_DTAR Register via DAP access (using APB-AP).

A 32-bit write access has to be executed, writing 0x00000001 to address 0x0000E004 using the AHB-AP of the CoreSight debug interface.

After this write access the TAP is getting active and accessing of scan chain using the bsdl file information is possible.

The access flow is following:

1. Reset MCU
2. Apply minimum 16 JTAG Clock cycles (TCLK) required for JTAG tool recognition
3. Power up JTAG DP (CTRL/STAT) via tool access
4. Select APB-AP
5. Write DTAR Register to enter boundary scan mode
6. TAP active continue with bsdl file instructions

2.1.2 Enter boundary scan via board test mode

With this method boundary scan mode is entered via external pin levels.

During active Reset level (Low Level) at RSTX pin change levels of following Pins:

Set MODE pin to ‘1’

In addition following Port pin have to be set externally

Table 2-1: Pin level for boundary scan

Series	Pin	Level
MB9DF125	P1_29	0
MB9DF126	P1_29	0
MB9EF226	P1_32	0

After Reset release Test Access Port is getting active and scan chain can be accessed using the bsdl file information.

2.2 Port input activation

In FCR4 series, port input needs to be activated separately. Therefore an additional private instruction, IO_CNTRL, is used in bsdl file beside the standard instructions. Two OPCODES are available, ENALBE and DISABLE. Enabling the IO_CNTRL will enable all GPIO inputs. See device specific datasheet and bsdl file.

2.3 GPIO Input Level and Output Drive Strength

The Port input level and output drive strength are configurable in FCR4 devices.

However in boundary scan mode they are fixed:

Table 2-2: GPIO input level and output drive strength

Cell Type	Input Level	Drive Strength	Pull-Up / -Down
BIDI50	Hysteresis	1 mA	inactive
SMC	Hysteresis	1 mA	inactive
BIDI33	Hysteresis	12 mA	inactive

2.4 JTAG Port Input Level and Output Drive Strength

The JTAG input pins using TTL input level. For input level range see corresponding device datasheet. As reference BIDI50 IO Circuit type can be used.

Table 2-3: Input level JTAG pins

JTAG pin	Cell type	Input level	Pull-up / -down
JTAG_TDI	JTAGIUP	TTL	Pull-up
JTAG_TCK	JTAGIUP	TTL	Pull-up
JTAG_TMS	JTAGIUP	TTL	Pull-up
JTAG_NTRST	JTAGIDN	TTL	Pull-down

JTAG_TDO Output level is CMOS type. As reference Pin type ‘Normal output (VDP5)’ can be used. The output drive strength is:

Table 2-4: JTAG_TDO output drive strength

FCR4 series	Cell type	Output level	Drive strength	Pull-up / -down
MB9DF125	JTAGO	Normal output (VDP5)	2mA	n.a.
MB9DF126	JTAGO	Normal output (VDP5)	1mA	n.a.
MB9EF226	JTAGO	Normal output (VDP5)	2mA	n.a.

Appendix A.

A.1 Abbreviation

Arm®	Arm® is a registered trademark of ARM Limited in the EU and other countries
DAP	Debug Access Port
FCR4	Cypress ARM® Cortex®-R4 series
JTAG	Joint Test Action Group (IEEE 1149.1 standard)
MCU	Microcontroller Unit
TAP	Test Access Port

A.2 Related information

Ref. #	Document file name	Description
1	FCR4_Cluster_Series_Hardware_Manual.pdf	FCR4 Cluster Series Hardware Manual
2	mb9df126-ds707-00002-e.pdf	FCR4 Cluster Series MB9DF126 - ATLAS Datasheet
3	MB9DF125_Atlas-L_MB9DF125_Series.pdf	FCR4 Cluster Series MB9DF125 – ATLAS-L Datasheet
4	MB9EF226_Series_32-bit_Microcontrollers_FCR4_Family.pdf	FCR4 Cluster Series MB9EF226 – TITAN Datasheet
5	DDI0363D_cortexr4_r1p3_trm.pdf	ARM® Cortex-R4 and Cortex-R4F Technical Reference Manual
6	DDI0406B_arm_architecture_reference_manual_errata_markup_4_0.pdf	ARM® Architecture Reference Manual ARM®v7-A and ARM®v7-R edition
	DDI0314H_coresight_components_trm.pdf	ARM® CoreSight™ Components Technical Reference Manual
7	mcu-an-300176-e-vxx-fcr4_hardware_setup.pdf	Application Note discussion FCR4 series hardware considerations
8	mcu-an-300125-e-vxx-fcr4_debug_requirements_for_tool_chain	Application Note discussion FCR4 debug features to be setup at tool vendors

Document History

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*A	5071287	MKEA	01/07/2016	Converted Spansion Application Note “MCU-AN-300180-E-V10” to Cypress format
*B	5840847	AESATP12	08/01/2017	Updated logo and copyright.
*C	6054547	NOFL	02/12/2018	Updated links

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