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AN205431

Fr, Mb91460, Clock Supervisor

This application note gives an overview of the Clock Supervisor. Purpose of the Clock Supervisor is the supervision of the Main and Sub oscillators. In case of oscillation (OSCMAIN or OSCSUB) failure the Clock Supervisor control logic will take action, i.e. switching to an internal RC-oscillation clock (CLKRC 100 kHz), depending on the operation mode set in the control register.

1 Introduction

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Purpose of the Clock Supervisor is the supervision of the Main and Sub oscillators. In case of oscillation (OSCMAIN or OSCSUB) failure the Clock Supervisor control logic will take action, i.e. switching to an internal RC-oscillation clock (CLKRC 100 kHz), depending on the operation mode set in the control register.

2 Clock Supervisor

This chapter explains the Clock Supervisor in detail.

2.1 Overview

There are two independent supervisors one for the Main clock and one for the Sub clock. They can be enabled/ disabled separately.

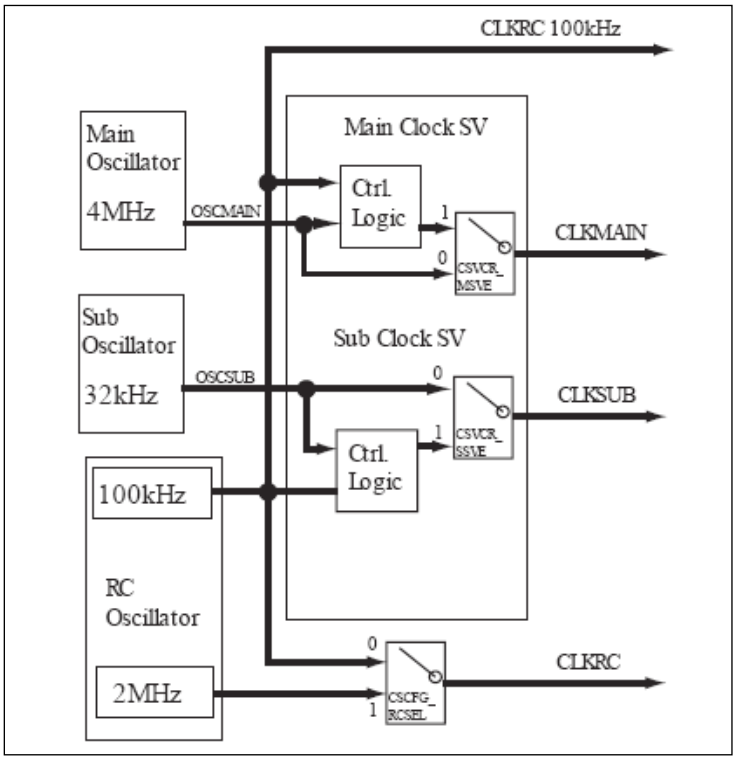
Main clock and Sub clock supervisor are disabled and re-enabled automatically if the corresponding oscillator is disabled and re-enabled.

There are two status bits in the Clock Supervisor Control Register, which indicate the failure of the Main clock and Sub clock. These bits can be available at two port pins (device dependent).

If a clock used by MCU fails for a certain time (20-80µs for Main clock / 160-640µs for Sub clock) the MCU is reset and the reset cause can be checked after reset vector fetch.

To find out whether the Clock Supervisor has asserted reset, the software must check the reset cause by reading the RSRR register. If INIT (bit 7 of RSRR) is set, the cause was either external reset at the INITX pin or the clock supervisor. If neither SM bit nor MM bit (bit 5 and bit 6 of CSVCR) is set, reset cause was the external reset. If SM is ’1’ the reset cause is a missing Sub clock and if MM is ’1’ the reset cause is a missing Main clock.

Figure 1. Block Diagram of Clock Supervisor



2.2 Registers

This section lists the Clock Supervisor Control Register and describes the function of each bit in detail.

2.2.1 Clock Supervisor Control Register (CSVCR)

The Clock Supervisor Control Register (CSVCR) sets the operation mode of the Clock Supervisor.

Bit No.	Name	Explanation	Initial Value	Value	Operation
0	OUTE	Output enable*	0	0	Do not enable ports for MCLK_MISSING and SCLK_MISSING output pins
				1	Enable ports for MCLK_MISSING and SCLK_MISSING output pins
1	SRST	Sub clock mode reset	0	0	Do not perform reset upon transition from Main clock to Sub clock modes if Sub clock is already missing
				1	Perform reset upon transition from Main clock to Sub clock modes if Sub clock is already missing
2	SSVE	Sub clock supervisor enable	1	0	Disable Sub clock supervisor
				1	Enable Sub clock supervisor
3	MSVE	Main clock supervisor enable	1	0	Disable Main clock supervisor
				1	Enable Main clock supervisor
4	RCE	RC oscillator enable	1	0	Disable RC-oscillator in STOP mode
				1	Enable RC-oscillator in STOP mode
5	SM	Sub clock missing	0	0	Missing Sub clock has not been detected
				1	Missing Sub clock has been detected

Bit No.	Name	Explanation	Initial Value	Value	Operation
6	MM	Main clock missing	0	0	Missing Main clock has not been detected
				1	Missing Main clock has been detected
7	SCKS	Sub clock select (only used for single clock devices)	0	0	32k oscillation used as Sub clock
				1	RC oscillation used as Sub clock

*Note: This bit can be used as an output enable to output the signals MCLK_MISSING (bit 3 of CSVCR) and SCLK_MISSING (bit 4 of CSVCR) to port pins. For MB9F1460D series it is available at Pin number 3 and 2 respectively.

For more information about the pins see the corresponding Datasheet.

2.3 Operation Modes

2.3.1 Operation mode with initial settings

In case the clock supervisor control register (CSVCR) is not configured at the beginning of the user program, the RC-oscillator, the Main clock supervisor and the Sub clock supervisor is enabled.

The Main clock supervisor is enabled after the ‘oscillation stabilization wait time’ or in case the Main clock is missing before the completion of the ‘oscillation stabilization wait time’, after the ‘Main clock timeout’ (TO_MCLK) from the timeout counter. (The timeout counter is clocked with CLKRC) If the Main clock is missing from power-on, the power-on reset state is never left, which in this case is a safe state. The user must make sure with external pull-up/pull-down resistors that all relevant signals are pulled to the correct level.

The Sub clock supervisor is enabled after the completion of the ‘Sub clock timeout’ (TO_SCLK) from the timeout counter.

If the Main clock stops while the Main clock supervisor is enabled, the Main clock is replaced with CLKRC 100kHz, the MM bit is set to ‘1’ and reset (EXT_RST_OUT) is asserted.

If the Sub clock stops and if the Sub clock supervisor is enabled, the behavior depends on whether the MCU is in Main clock mode or in Sub clock mode. If the Sub clock stops in Sub clock mode, CLKRC divided by two substitutes the Sub clock, the SM bit is set to ‘1’ and reset (EXT_RST_OUT) is asserted. If the Sub clock stops in Main clock mode, CLKRC divided by two substitutes the Sub clock, the SM bit is set to ‘1’ and no reset occurs upon transition to Sub clock mode, since the SRST bit has its initial value of ’0’. If the SRST bit is ‘1’ a reset (INIT) occurs.

If a clock missing was detected, the Application cannot change back to MAIN or Sub clock operation. The MM or SM bit are read-only bits. Only external INIT reset at pin INITX will reset the condition.

2.3.2 Disabling the clock supervisors

If clock supervision is not required or sub clock is not used / connected to the device it is possible to disable the supervision of each clock.

The Main clock supervisor is disabled by setting MSVE (bit 3 of CSVCR) to ‘0’.

The Sub clock supervisor is disabled by setting SSVE (bit 2 of CVSVR) to ‘0’.

2.3.3 Re-enabling the clock supervisors

The Main clock supervisor is enabled by setting MSVE (bit 3 of CSVCR) to ‘1’.

The Sub clock supervisor is enabled by setting SSVE (bit 2 of CSVCR) to ‘1’.

2.3.4 Enabling / Disabling RC-oscillator in STOP mode

It is possible to select if RC-Oscillator is enabled or disabled in STOP mode. In all other modes the RC-oscillator is always enabled. When entering STOP mode the RCE bit is checked an RC-Oscillator is stopped or remains running. In case of a wakeup event in STOP mode the RC-Oscillator is activated automatically (if RCE bit is set to ‘0’).

Disabling the RC-oscillator in STOP mode is done by setting bit RCE (bit 4 of CSVCR) to ’0’. Enabling the RC-oscillator in STOP mode is done by setting bit RCE (bit 4 of CSVCR) to ‘1’.

Note:

In some devices of MB91460 series it is possible to select if Hardware Watchdog is enabled in STOP mode. If this is enabled, the RC-oscillator is enabled in STOP mode, independent from RCE value. See datasheet if this feature is supported.

2.3.5 Clock Supervisor in STOP mode

If RC-oscillator, Main clock and Sub clock supervisors are automatically disabled at transition into STOP mode if they are enabled already. The corresponding enable bits in the clock supervisor control register remain unchanged. So after wake-up from STOP mode the RC-oscillator and the clock supervisors will be enabled again.

If the corresponding enable bits are set to ‘0’, the clock supervisors will stay disabled after wake-up from STOP mode.

The RC-oscillator is enabled immediately after wake-up from STOP mode.

The Main clock supervisor is enabled after the ‘oscillation stabilization wait time’ or in case the Main clock is missing after wake-up from STOP mode, after the ‘Main clock timeout’ (TO_MCLK) from the timeout counter which is clocked with the CLKRC.

The Sub clock supervisor is enabled after the ‘Sub clock timeout’ (TO_SCLK) from the timeout counter which is clocked with the CLKRC.

2.3.6 Switching back from RC Oscillation to Clock Oscillation

In some devices of MB91460 series it is possible to switch back from RC-oscillator in case a clock miss was detected without asserting external INITX reset at the pin. Check corresponding Datasheet if this feature is supported.

2.3.6.1 Switching back from RC–Oscillation to Main Oscillation

In case of MAIN clock miss the clock source is switched to RC-Oscillation and a Reset is asserted. The Application can check the reset cause during init phase the `RSRR` and `CSVCR` register to find out the reset cause. In case the `MM` bit is set to 1 in `CSVCR` register a Main clock miss was detected. It is possible to switch back to MAIN Oscillator by clearing bit `MM` in `CSVCR` register. In case the main clock is still missing the write access to the bit is ignored and RC-Oscillator is used as clock source. In case the main clock is operating, clock source is switched from RC-Oscillator to main oscillator.

2.3.6.2 Switching back from RC–Oscillation to Sub Oscillation

MCU is running on SUB clock and a sub clock miss was detected, switching to RC-Oscillator. The SRST bit in CSVCR register set to 0, no reset is generated in case of SUB clock miss detection. It is possible to switch back to Sub Oscillation by clearing the `CM` bit in `CSVCR` register. In case the sub clock is still missing the write access to the bit is ignored and RC-Oscillator is used as clock source. In case the sub clock is operating, clock source is switched from RC-Oscillator to main oscillator.

3 Clock Supervisor Example

Example for Clock Supervisor

3.3 Enabling and Disabling RC Oscillator in STOP mode

```
char Set_RCE(char state){
 if (state) {
        CSVCR_RCE = 1;              /* Enable RC Oscillator in STOP mode*/
 } else {
        CSVCR_MSVE = 0;             /* Disable Clock supervisor */
        CSVCR_SSVE = 0;
        while (CSVCR_SM == 1 || CSVCR_MM == 1){
                        HWWD = 0;
               }
               CSVCR_RCE = 0;              /*Disable RC Oscillator in STOP mode*/
               }
        return 0;
 }
```

3.4 Enabling and Disabling Main Clock and Sub Clock Supervisor

```
char Set_MSVE(char state){              /*Enable Main clock supervisor*/
        if (state)
               CSVCR_MSVE = 1;
        else
               CSVCR_MSVE = 0;
        return 0;
 }

 char Set_SSVE(char state){             /*Enable Sub clock supervisor*/

        if (state)
               CSVCR_SSVE = 1;
        else
               CSVCR_SSVE = 0;
        return 0;
 }
```

4 Additional Information

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The software examples related to this application note is:

91460_clock_supervisor

It can be found on the following Internet page:

http://www.cypress.com/cypress-mcu-product-softwareexamples

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	NOFL	06/18/2008	V1.0, First draft, HPi
			08/28/2008	V1.1, MSt Added information of feature in new devices, RCE bit description corrected
*A	5137428	NOFL	02/15.2016	Converted Spansion Application Note “MCU-AN-300104-E-V11” to Cypress format
*B	5873630	AESATMP9	09/05/2017	Updated logo and copyright.
*C	6054547	NOFL	02/12/2018	Updated links Updated template

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