AN205349

FM3 MB9AF112L/ MB9AF314L Series Single Shunt

This application note describes single shunt implementation in MB9AF112L/MB9AF314LSeries and also describes about the algorithm implementation of software and hardware.

Contents

1 Introduction

This application note describes single shunt implementation in- MB9AF112L/MB9AF314LSeries.

This application note describes the algorithm implementation of software and hardware.

1.1 Advantages and disadvantages of using a single-shunt resistor

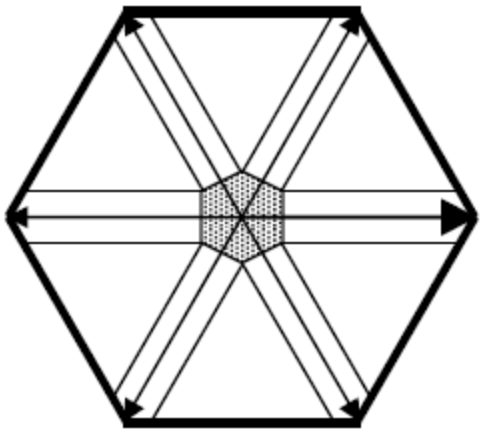
Advantages

One of most important reasons for single-shunt three-phase reconstruction is cost reduction. Which in turn, simplifies the sampling circuit to one shunt resistor and one differentia amplifier. In addition to cost reduction benefits, the single-hunt algorithm allows the use of power modules that do not provide individual ground connection of each phase. Another benefit of single-shunt measurement is that the same circuit is being used to sense all three phases. Gains and offset will be the same for all measurements, which eliminates the need to calibrate each phase amplification circuit or compensate in software.

Disadvantages

During single-shunt measurements, a modification on the sinusoidal-modulation pattern needs to be made in order to allow current to be measured (for example: low-modulation index region). This pattern modification could generate some current ripple. Due to modification of patterns and correction of the same modifications, more CPU is used to implement this algorithm. As shown bellows:

Figure 1. low-modulation index region



1.2 Possible Techniques to Overcome These Problems

One possible solution to this problem is to ignore current measurements during these critical periods. This is not desirable since some algorithms, including the one used in this application note, require information from all three currents in order to estimate the position of the rotor. Another solution is to estimate current measurements. This could be one good solution, but requires fine tuning since current increase would depend on pass current measurement, motor parameters, and so on. The third solution is to expand the period of time where measurement is taking place. This would force a minimum time (critical measuring time) so that current stabilizes to a new value that is actually measurable by the Analog-to-Digital Converter (ADC). We will focus on modifying the switching pattern to a minimum measurement time window (RETRIT), which is present all of the time.

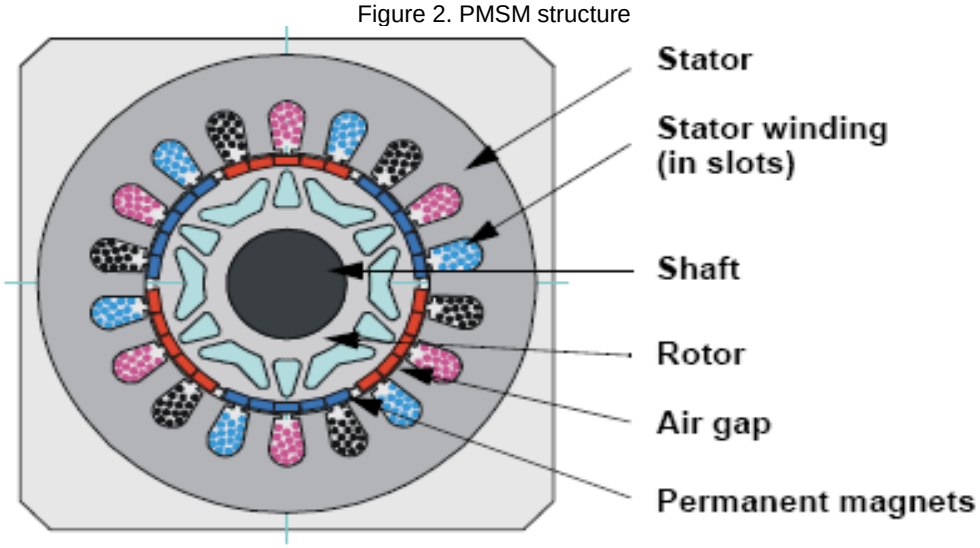
2 Single Shunt Principle

2.1 Control Motor Structure

2.1.1 Three-Phase PM Synchronous Motor

The PM synchronous motor is a rotating electric machine with a classic three-phase stator like that of an induction motor; the rotor has surface-mounted permanent magnets.

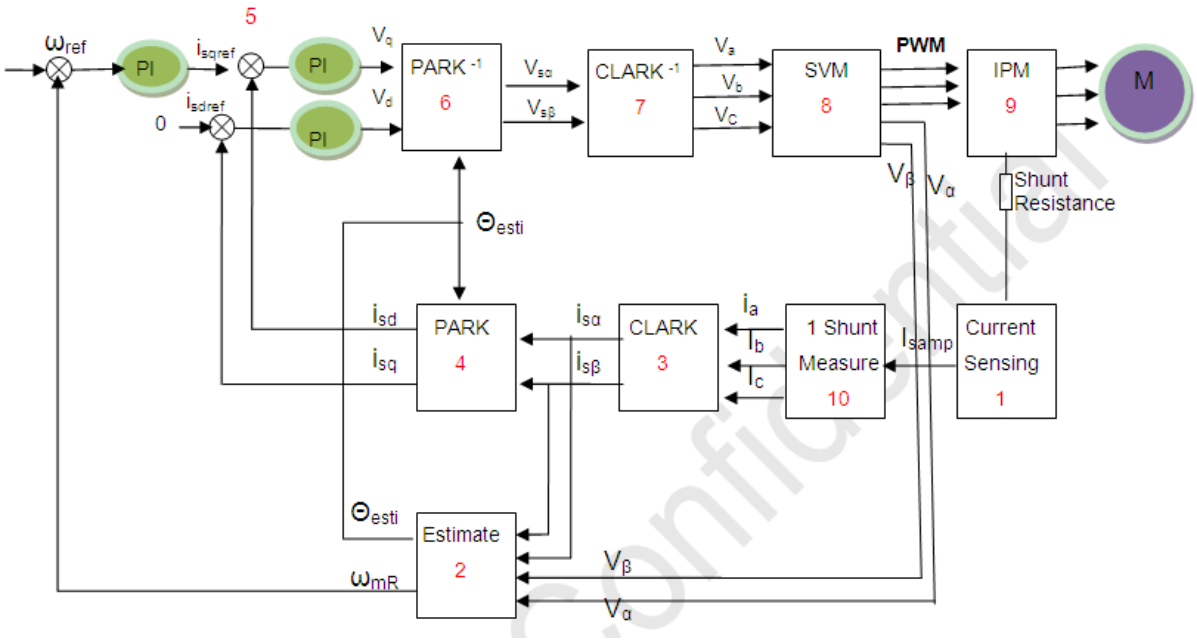
Figure 2. PMSM structure



2.2 Motor Control Block Overview

This section describes the PMSM FOC control theory with single shunt. Figure 3 below shows the whole block.

Figure 3. PMSM FOC Block with Single Shunt



Modules explanation:

1. When zero interrupt of PWM happen, the right OCCP buffer will change, when the top interrupt of PWM occurred, the duty of the PWM will updated. the DC bus current are measured by AD interrupt base on before cycle calculator AD timer from the DC bus current. These measurements provide values i1 and i2. In this period, running the motor functions except the motor arithmetic.
2. When top interrupt of PWM happen, three phase value using before detect the currents, i3 is calculated because i1, i2 and i3 have this relationship:

i1+ i2 + i3 = 0.

And i1, i2 and i3 compare with the ia, ib and ic base on the reconstruction table as shown below.

Table 1. Six PWM on or off and DC bus current

IH	2H	3H	1L	2L	3L	IBUS
ON	OFF	OFF	OFF	ON	ON	+IA
OFF	ON	OFF	ON	OFF	ON	+IB
OFF	OFF	ON	ON	ON	OFF	+IC
OFF	ON	ON	ON	OFF	OFF	–IA
ON	OFF	ON	OFF	ON	OFF	–IB
ON	ON	OFF	OFF	OFF	ON	–IC

Table 2. Relationship Between Sector and Current

sector	Current sampled		Current reconstructed
	i1	i2	
6	ic	-ib	ia
2	ia	-ib	ic
3	ia	-ic	ib
1	ib	-ic	ia
5	ib	-ia	ic
4	ic	-ia	ib
0	0	0	0
7	0	0	0

The 3-phase currents are converted to a two axis system. This conversion provides the variables iα and iβ from the measured ia and ib and the calculated ic values. iα and iβ are time-varying quadrature current values as viewed from the perspective of the stator.

3. The two axis coordinate system is rotated to align with the rotor flux using a transformation angle calculated at the last iteration of the control loop. This conversion provides the Id and Iq variables from iα and iβ. Id and Iq are the quadrature currents transformed to the rotating coordinate system. For steady state conditions, Id and Iq are constant.
4. Error signals are formed using Id, Iq and reference values for each. The Id reference controls rotor magnetizing flux. The Iq reference controls the torque output of the motor. The error signals are input to PI controllers. The output of the controllers provide Vd and Vq, which is a voltage vector that will be sent to the motor.
5. A new transformation angle is estimated where vα, vβ, iα and iβ are the inputs. The new angle guides the FOC algorithm as to where to place the next voltage vector.
6. The Vd and Vq output values from the PI controllers are rotated back to the stationary reference frame using the new angle. This calculation provides the next quadrature voltage values vα and vβ.
7. The vα and vβ values are transformed back to 3- phase values va, vb and vc. The 3-phase voltage values are used to calculate new PWM duty cycle values that generate the desired voltage vector. The entire process of transforming, PI iteration, transforming back and generating PWM is illustrated in Figure 9. Next cycle DC bus current detecting of AD trigger timers are calculated and in this time the left OCCP buffer will change , when zero of PWM occurred, the duty of PWM will updated.

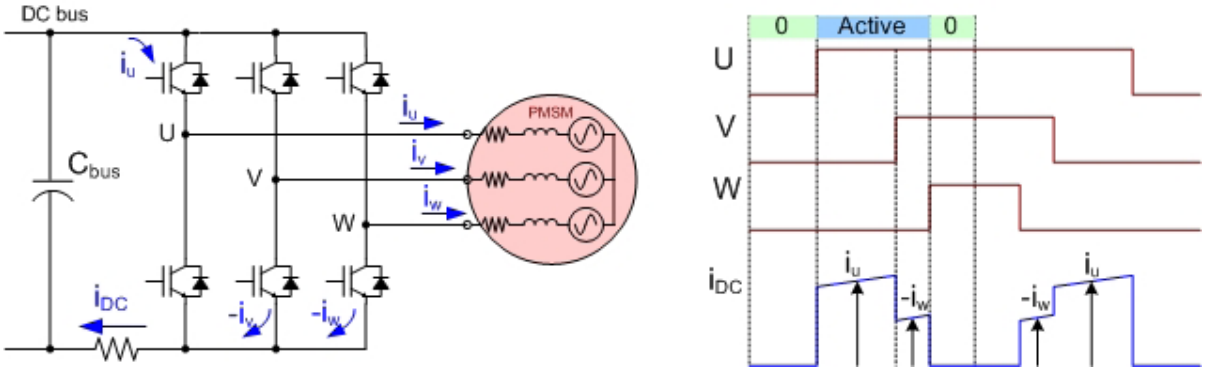
2.3 Single-shunt Current Measurement

Figure 4 shows the current sensing circuit.

Direct measurement of the motor winding current requires isolation circuits to handle the high common mode voltage and switching frequency at the motor windings. The phase current reconstruction circuit avoids the isolation requirement by measuring current in the dc link. The motor winding currents are measured by synchronizing the sampling of the current in the dc link shunt with the power inverter switching. In every PWM cycle, there are two active states where the motor windings are connected between the two dc bus rails. In each active state, one dc bus rail connects to a single motor winding and the other bus rail connects to the other two motor windings. The motor flowing from the dc bus rail flows through one winding and returns from the remaining two windings via the dc link shunt. The current sampled in the dc link shunt during this period is equal to the current in the single motor winding. A second winding current is sampled during the second active PWM state. The third winding current is calculated from the sum of the first two currents since they all must sum to zero.

This can be seen by examining the current flow in the power circuit in Figure 4 as it relates to the state of the power inverter switches. The first inverter state is a zero vector state where all windings are shorted to the lower dc bus rail. The second state is an active state where the U phase is connected to the positive rail and the V and W phases are connected to the negative rail. The third inverter state is also an active state but now only the W phase is connected to the negative rail. The fourth inverter state is a zero vector state where the windings are shorted to the positive rail. The second half of the PWM cycle is a mirror image of the first half of the cycle. In this complete PWM cycle, there are two states when the dc link current equals the U phase current and two states when the dc link current equals the negative W phase current.

Figure 4. Single Shunt Current Sensing



The Space vector modulator generates the PWM switching signals and the dc link current sample timing signals. The current reconstruction circuits include the A/D converter and the analog amplifier to bring the current shunt signal within the range of the converter. Successful implementation requires careful circuit board layout and fine tuning of the sample timing to avoid the significant circuit noise generated by the power device switching.

(Remark: at this document only detect the DC current at left half of cycle).

At below content will describe the phase reconstruction arithmetic amply.

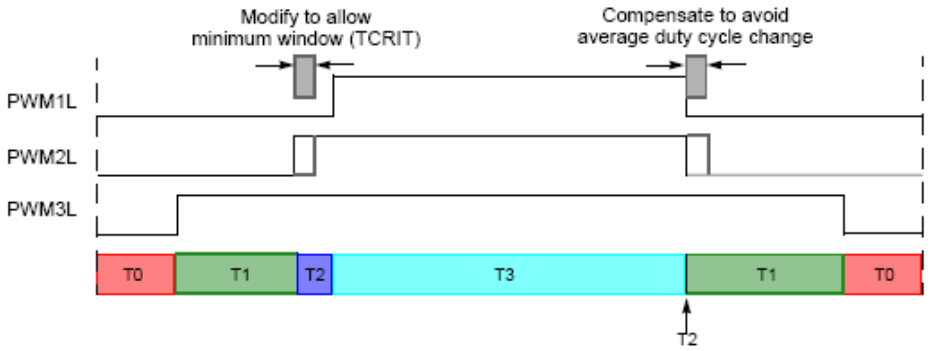
3 Single Shunt Implementation

3.1 How to sample single shunt current correctly

3.1.1 Compensation time

In some cases, t1 or t2 will be not available for AD sampling. It has to be moved a little to ensure enough time for current stability and AD sampling. As shown in Figure 5 below.

Figure 5. Compensation Time



There are three cases below about compensation:

T1 not available (Figure 6): compensating T1.

T2 not available (Figure 7): compensating T2.

Both T1 and T2 not available (Figure 8): compensating both T1 and T2.

So the minimum compensation time (A) must be existed for current stability and AD sampling.

Figure 6. T1 Compensation

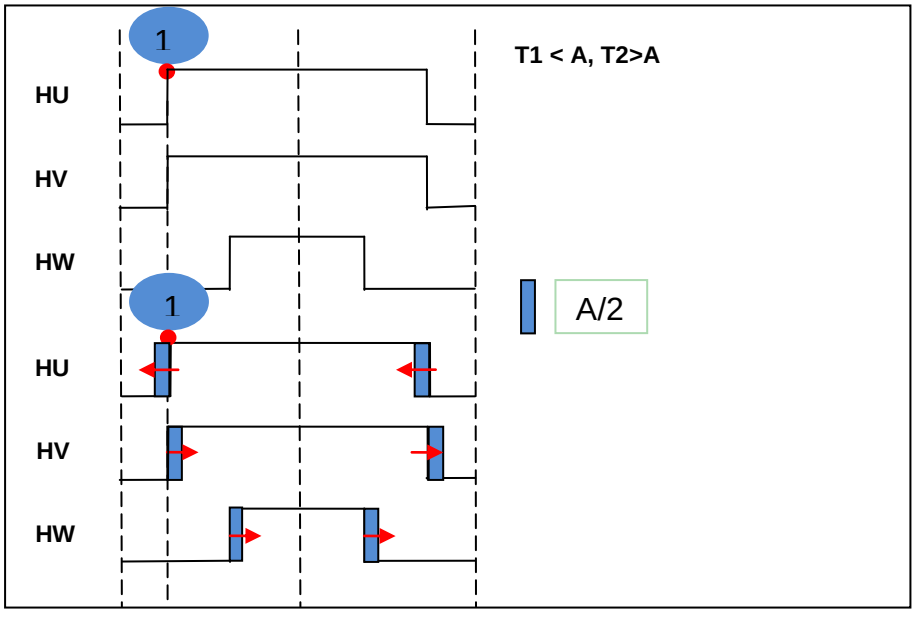


Figure 7. T2 Compensation

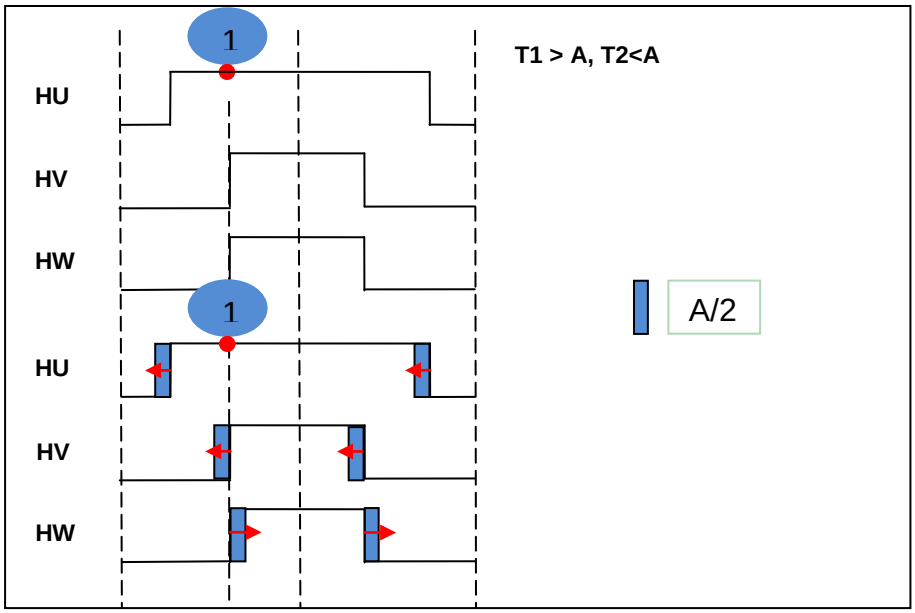
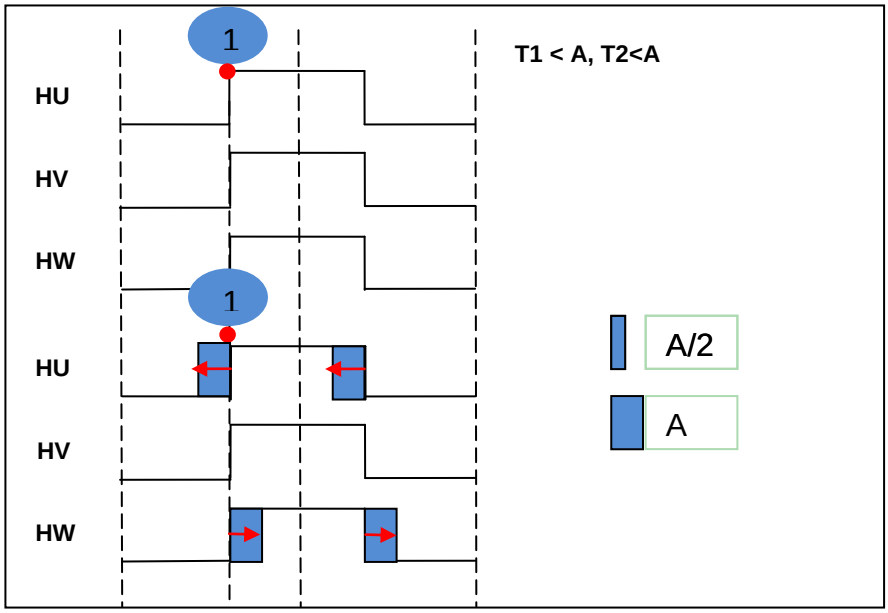


Figure 8. T1 and T2 Compensation

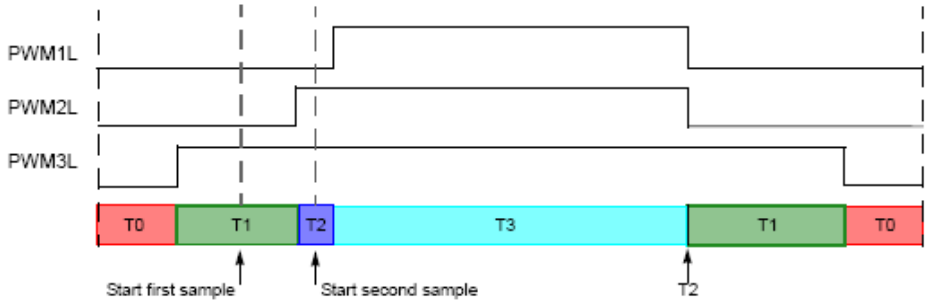


Above describing will occur at the voltage low 、 speed low and from one sector to another sector, that meaning low-modulation region.

3.1.2 Affection of Compensation Time

After compensated, we will compensate again at another half cycle in order to decrease the vector. Because the vector not changed in all cycle, so the vector was send will not change in every cycle. The changed vector between at the tow half of the cycle only. The operation as shown bellows:

Figure 9. The Vector Change at all Cycle



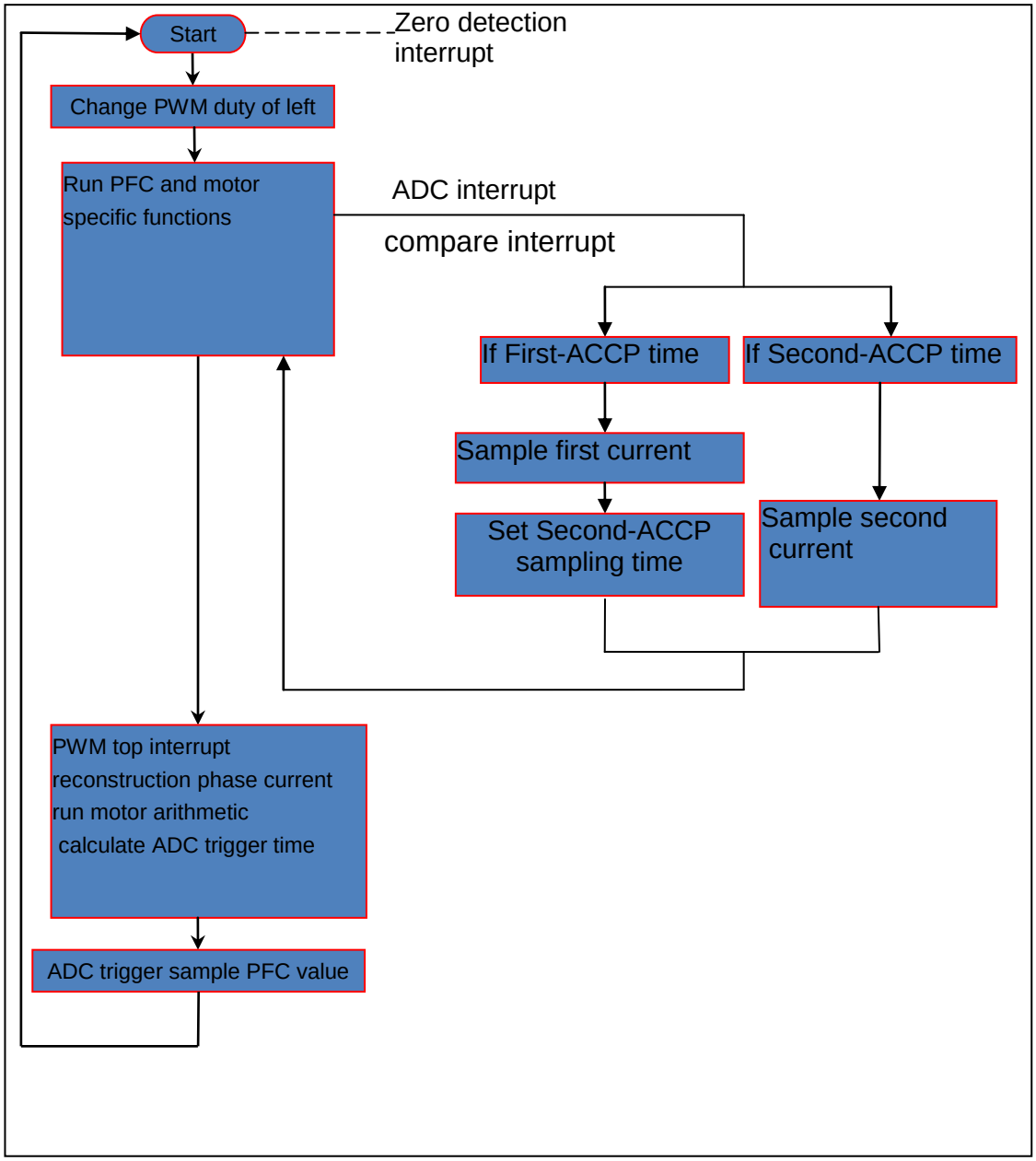
3.2 Single Shunt Software implementation

3.2.1 Software Flowchart

3.2.1.1 First Method

Right calculate the motor function and catch the current. Left run the arithmetic of motor.

Figure 10. First Method Software Flowchart

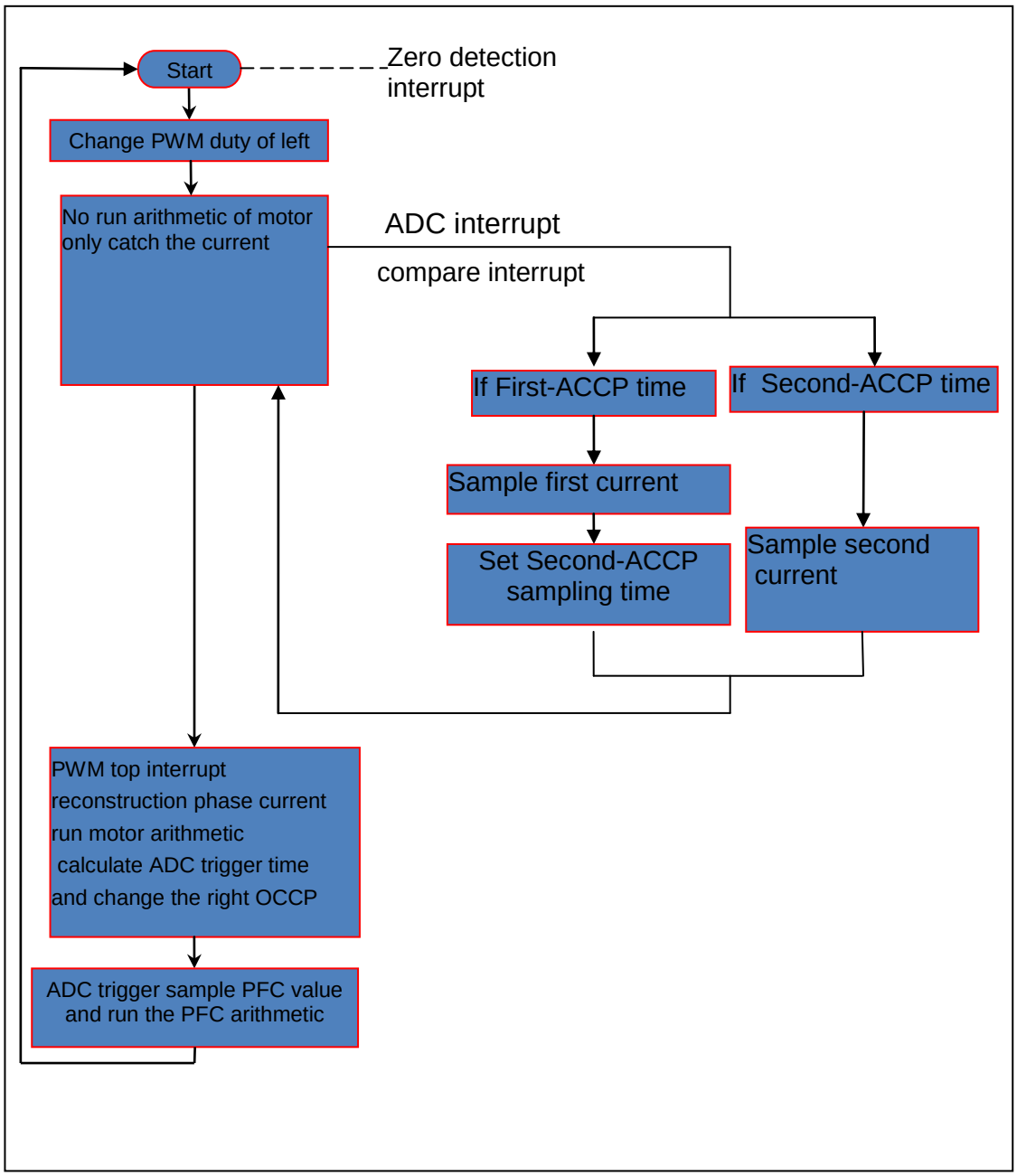


3.2.1.2 Second method

Left was used catch the current. Right run all function include motor arithmetic.

(Remark: this method needs the chip to run higher frequency).

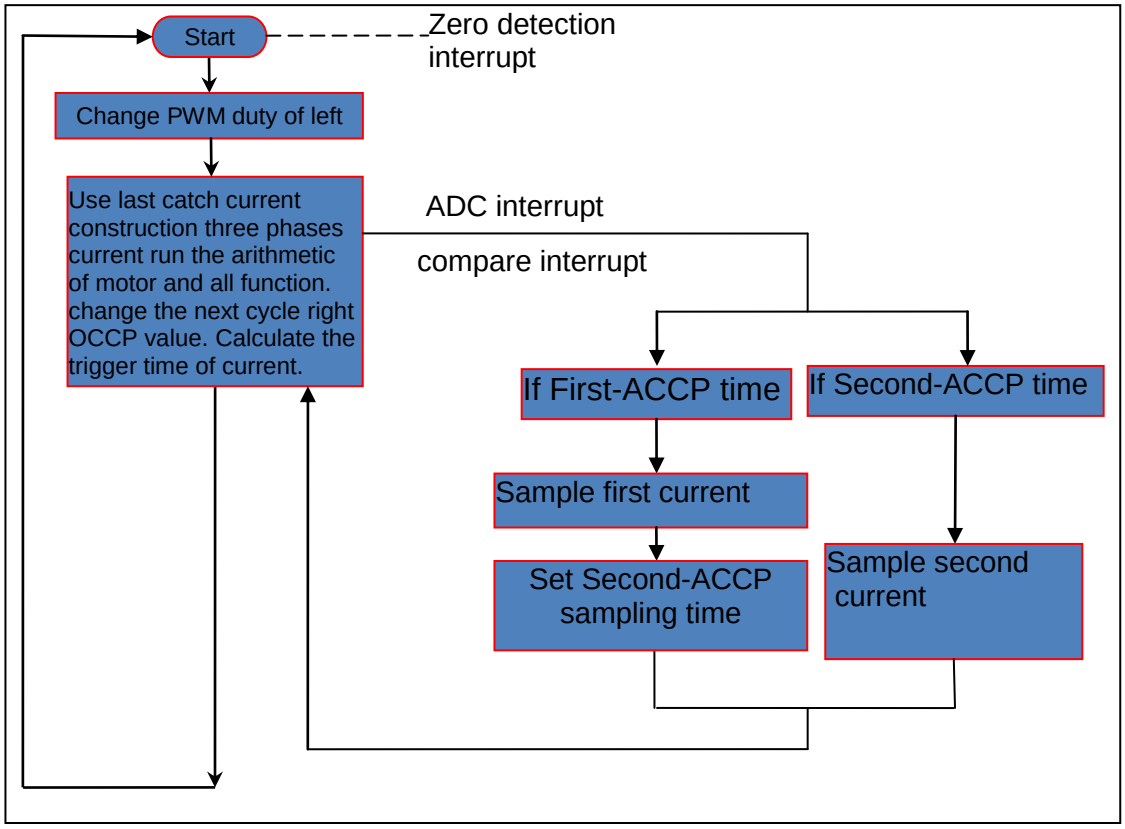
Figure 11. Second Method Software Flowchart



3.2.1.3 Third method

All cycle run the function and arithmetic that used last cycle catching the current.

Figure 12. Third Method Software Flowchart



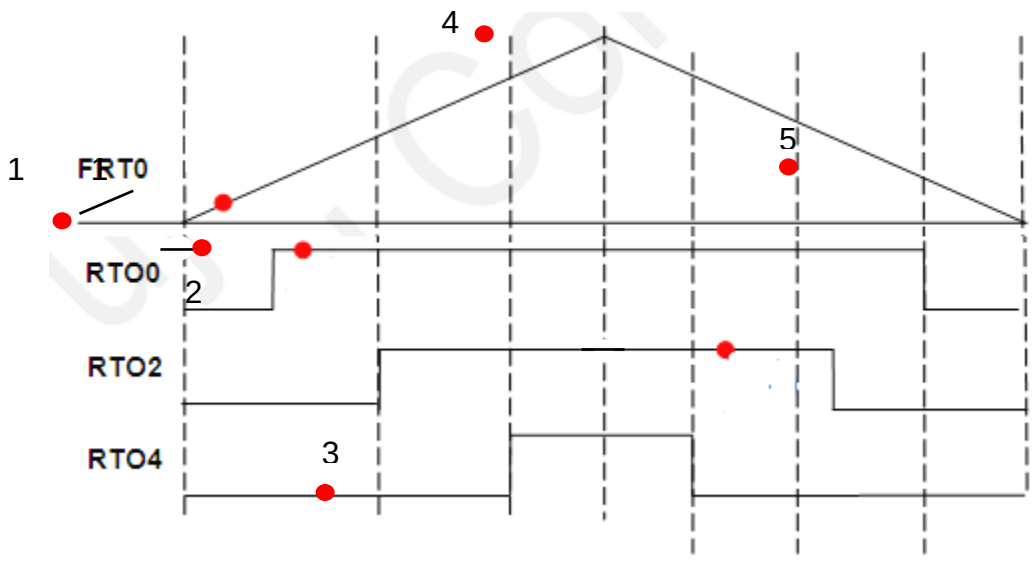
Algorithm flow explanation:

1. Write left register: it happens at the right time of zero interrupt triggering and run the PFC and other functions.
2. ADC0 First-ACCP trigger: AD start working that selecting timer trigger to sample current at T1 time and set the Second-ACCP.
3. ADC0 Second-ACCP trigger: AD start working that selecting timer trigger to sample current at T2 time;
4. Compare TOP interrupt: write right OCCP buffer register happens in this interrupt reconstruction three phase current and run the motor arithmetic, At the end, reload the AD trigger time.
5. ADC0 right half cycle trigger: It is used for sample IAC,VAC and VDC that be used calculate PFC and system parameters;

All cycle flows shown that bellow figure:

Point 1 shown the PWM zero interrupt;
Point 2 shown the ADC0 First-ACCP trigger;
Point 3 shown the ADC0 Second-ACCP trigger;
Point 4 shown the PWM top interrupt;
Point 5 shown the ADC0 of sample IAC,VAC and VDC;

Figure 13. Algorithm Flow



3.2.2 Compensation Time Calculation

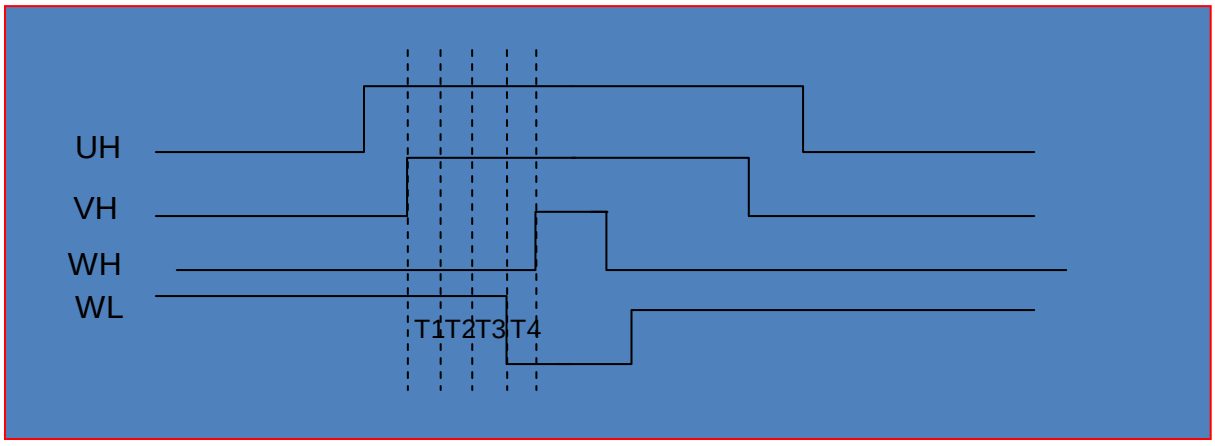
Compensation time contains four parts: T1, T2, T3, T4.

Restrict timer = T1 + T2 + T3 + T4.

Explanation of T1, T2, T3, T4:

1. T1: that time was taken on by IGBT on till it standing about resist on 1.5us.
2. T2: time for amplifier output stability. It relate on hardware. Output of amplifier needs enough time to be stable for AD sample.
3. T3: AD conversion time. The time was decided by AD conversion speed. If the AD conversion time bigger than resist time, catching value will distortion.
4. T4: dead time, The time come from inner dead time and it is set ensure value.

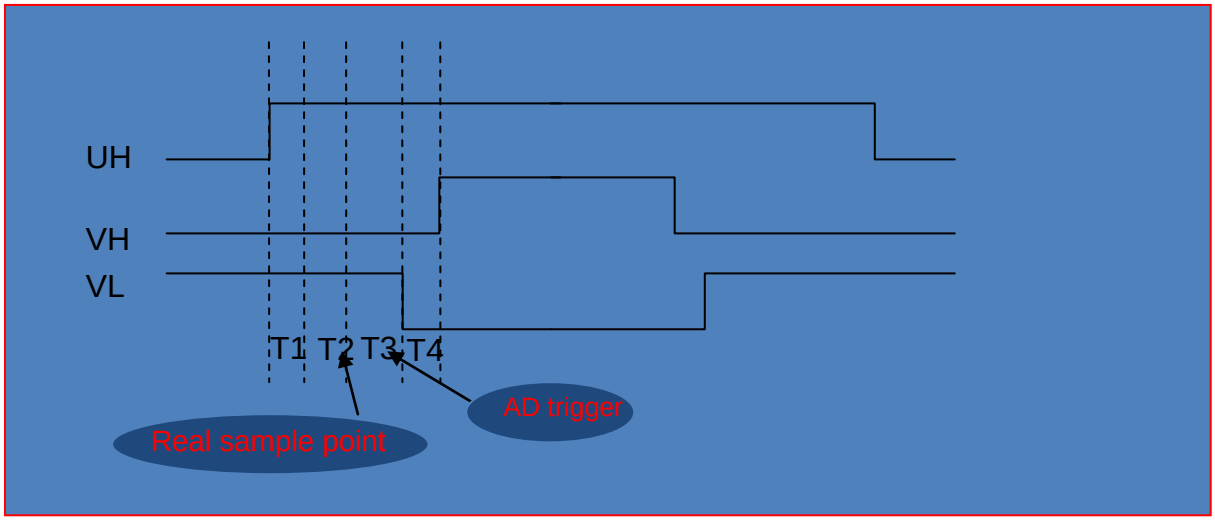
Figure 14. T2 Compensation Time Components



Vector T1 compensation time components are similar to vector T2.

3.2.3 AD First-ACCP trigger Point

Figure 15. T1 AD Trigger Point

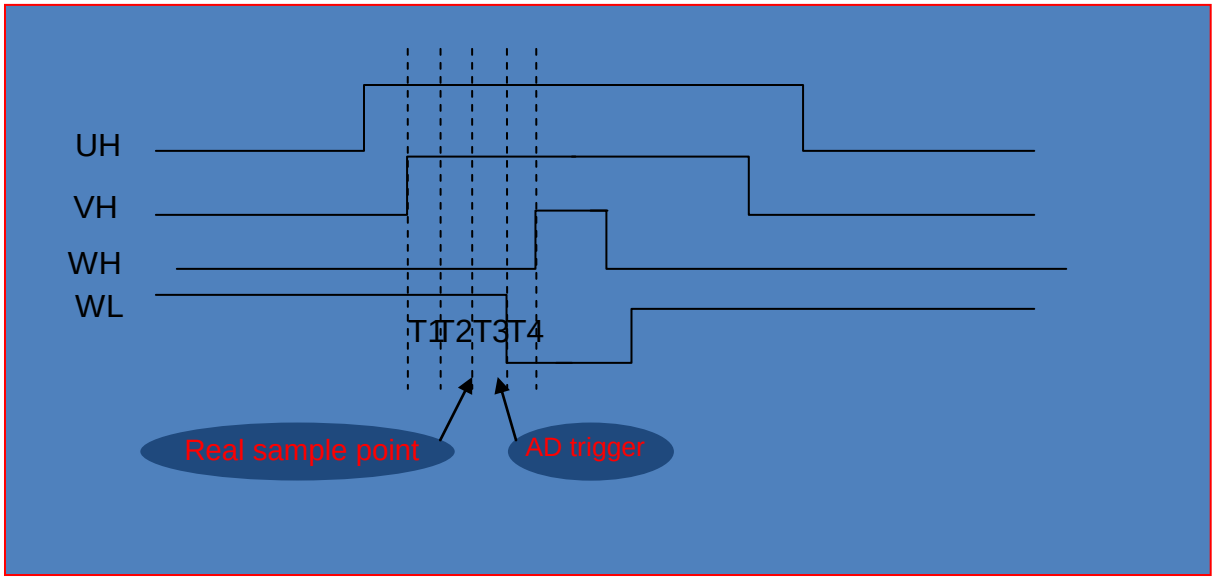


Explanation of T1, T2, T3, T4:

1. T1: that time was taken on by IGBT on till it standing about resist on 1us.
2. T2: time for amplifier output stability. It relate on hardware. Output of amplifier needs enough time to be stable for AD sample.
3. T3: AD conversion time. The time was decided by AD conversion speed. If the AD conversion time bigger than resist time, catching value will distortion.
4. T4: dead time, the time come from inner dead time and it is set ensure value.

3.2.4 AD Second-ACCP trigger Point

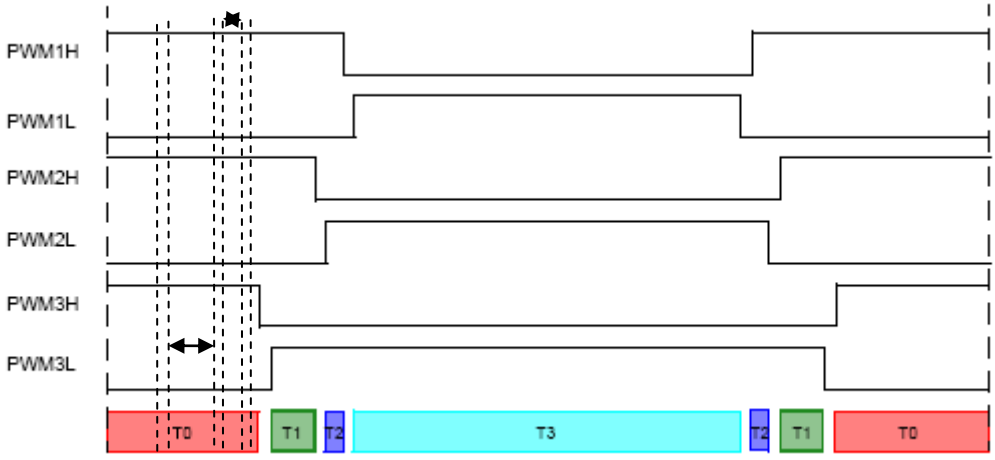
Figure 16. T2 AD Trigger Point



Vector T2 Meaning of T1, T2, T3, T4 is the same to vector T1.

T1, T2 at the same structure and influence by dead time as below:

Figure 17. T1 and T2 Valid Current Time at the same cycle

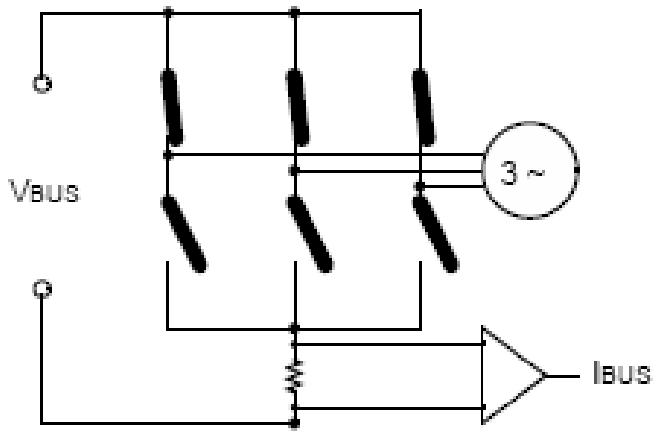


T0 and T3 as above all zero vector. We detect current only T1 and T2, they are taken part by dead time and increasing time at increasing edge.

3.3 Single Shunt Hardware

Single shunt hardware as below, it needs one amplifier and one shunt only:

Figure 18. Single Shunt Detect Hardware



And dual shunt and three shunt need more amplifiers and more shunts as belows :

Moreover , it need more amplifiers and shunts used the DC bus current protect.

So we need more cost for the dual and three shunt hardware.

Figure 19. Tow Shunt Detect Hardware

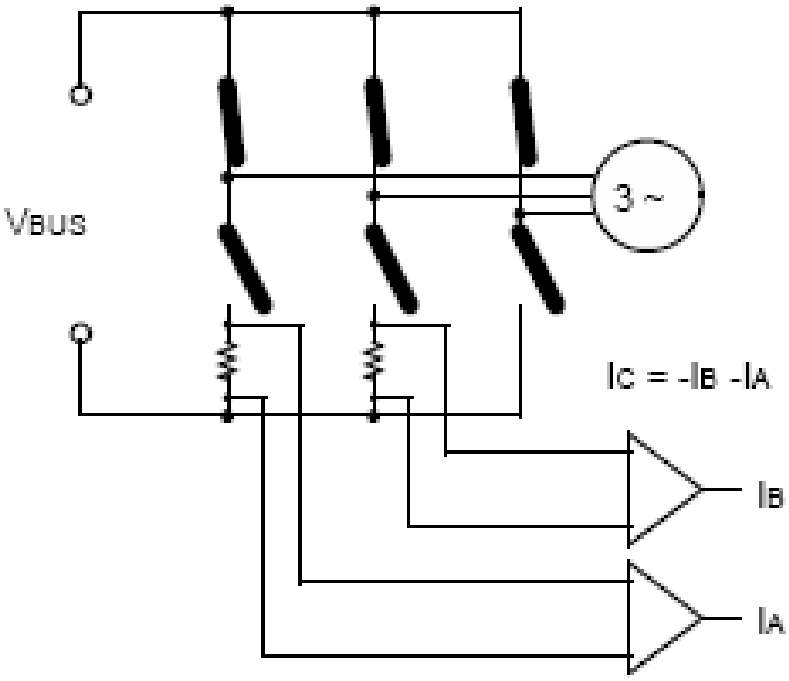
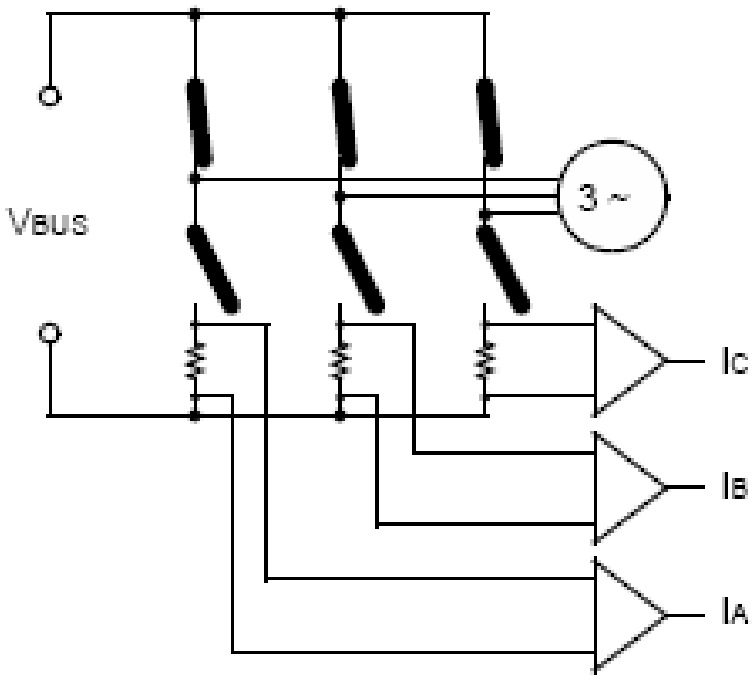


Figure 20. Three Shunt Detect Hardware



4 Single Shunt Function Verification

4.1 Basic Verification

4.1.1 Time for Amplifier Output Stability

The output of amplifier needs enough time for stability caused by IGBT switching time.

Different amplifier has different switching time, so component datasheet is needed. Figure 21 shows stability time.

Figure 21. Stability Time

4.1.2 Amplification times

Figure 22 shows amplifier output.

Figure 22. Amplifier Output

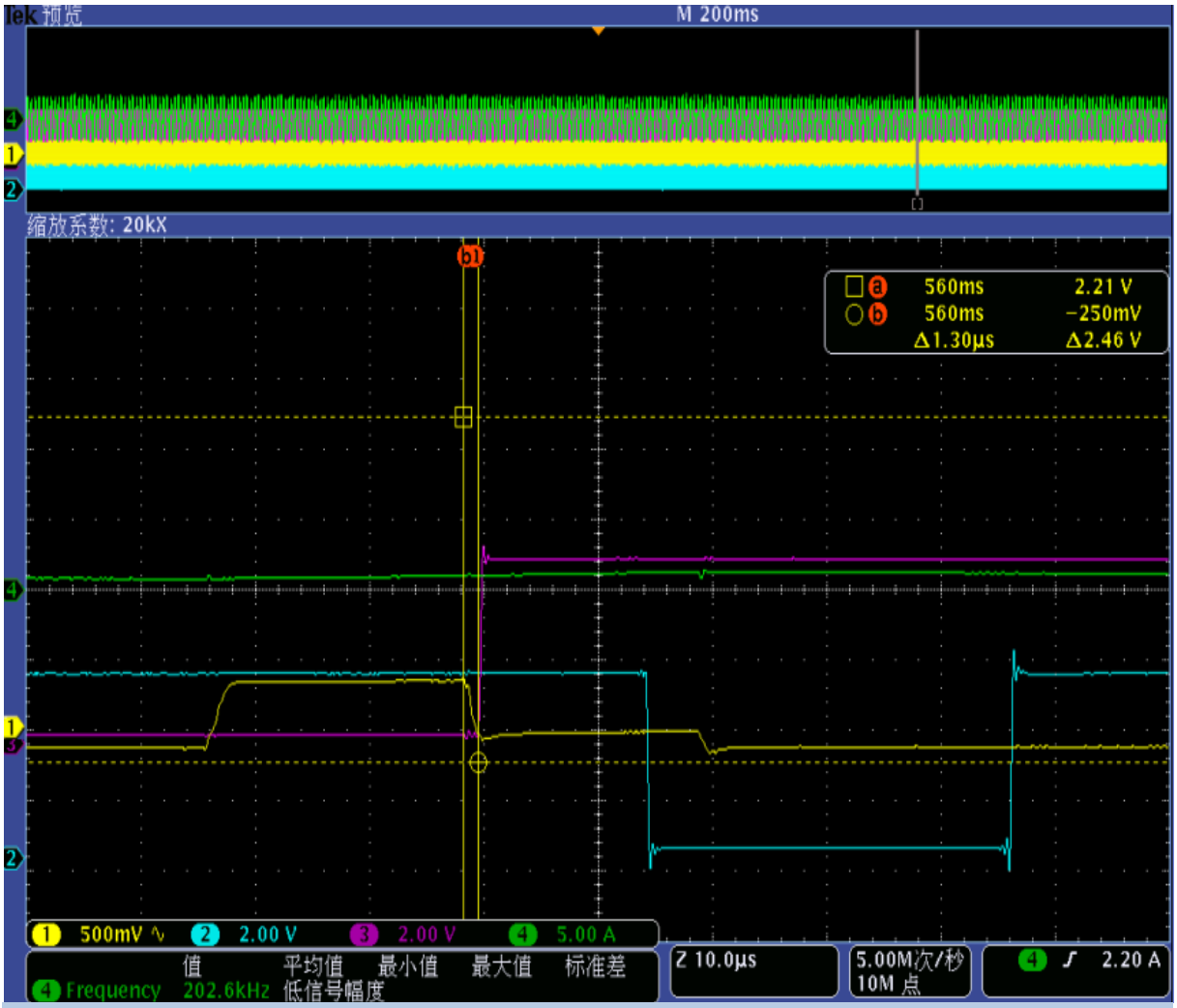


Figure 23 shows amplifier input.

Figure 23. Amplifier Input

From above, amplification times can be calculated.

4.1.3 Sector and Upper IGBT

To ensure waveform be generated correctly, sector and upper IGBT must be matched well.

4.1.4 Dead Time

To prevent upper and lower IGBT on at the same time, dead time must exist.

4.1.5 Compensation Time

The existence and correctness of compensation time can be recognized by upper IGBT waveform. Figure 24 shows T2 compensation information.

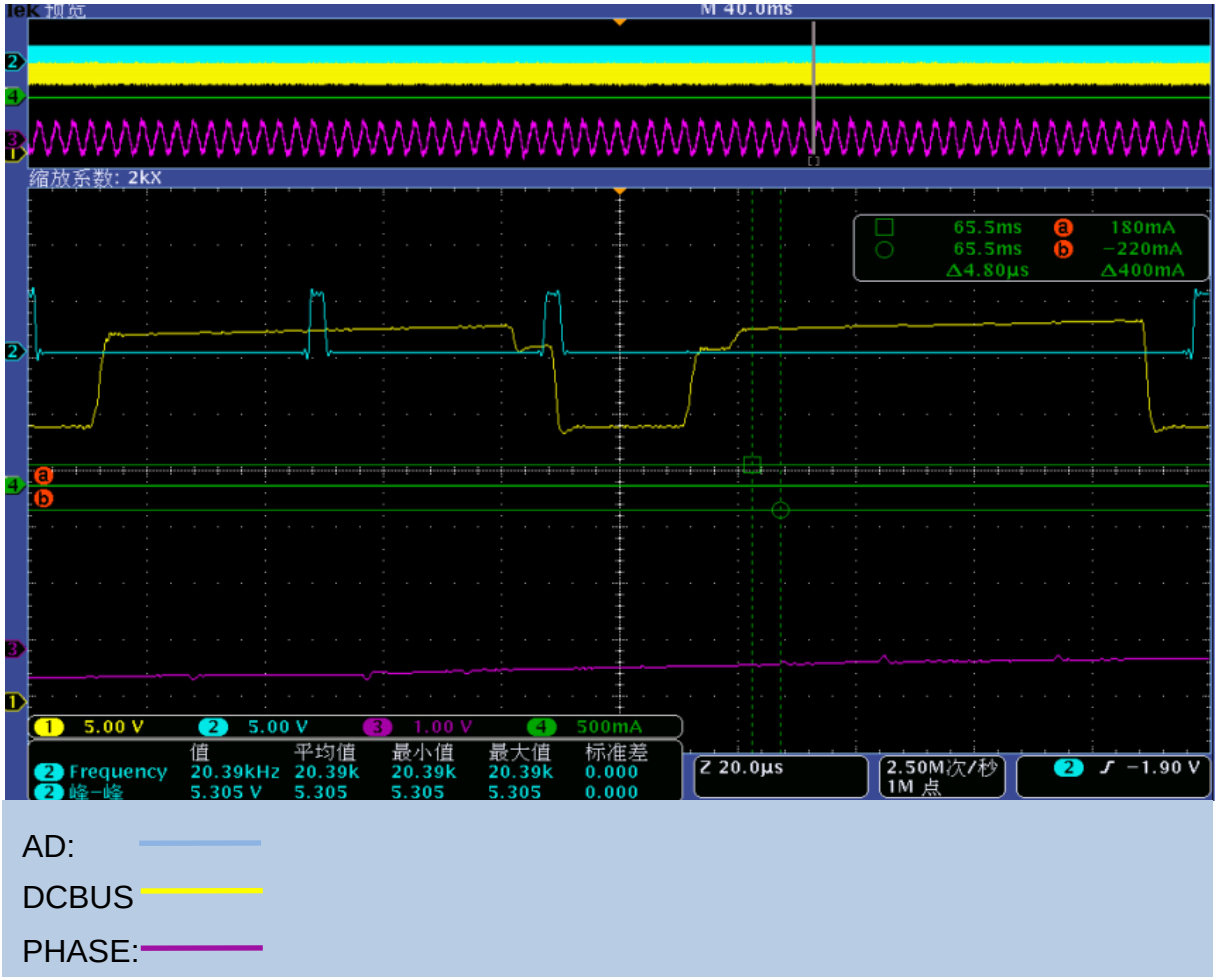
Figure 24. T2 Compensation

4.1.6 AD sample

Figure 25 shows AD trigger point based on correctness of sampling.

(Remark: AD single shown after the AD convert completion get into the AD interrupt, under 40M frequency AD convert time is about 1us).

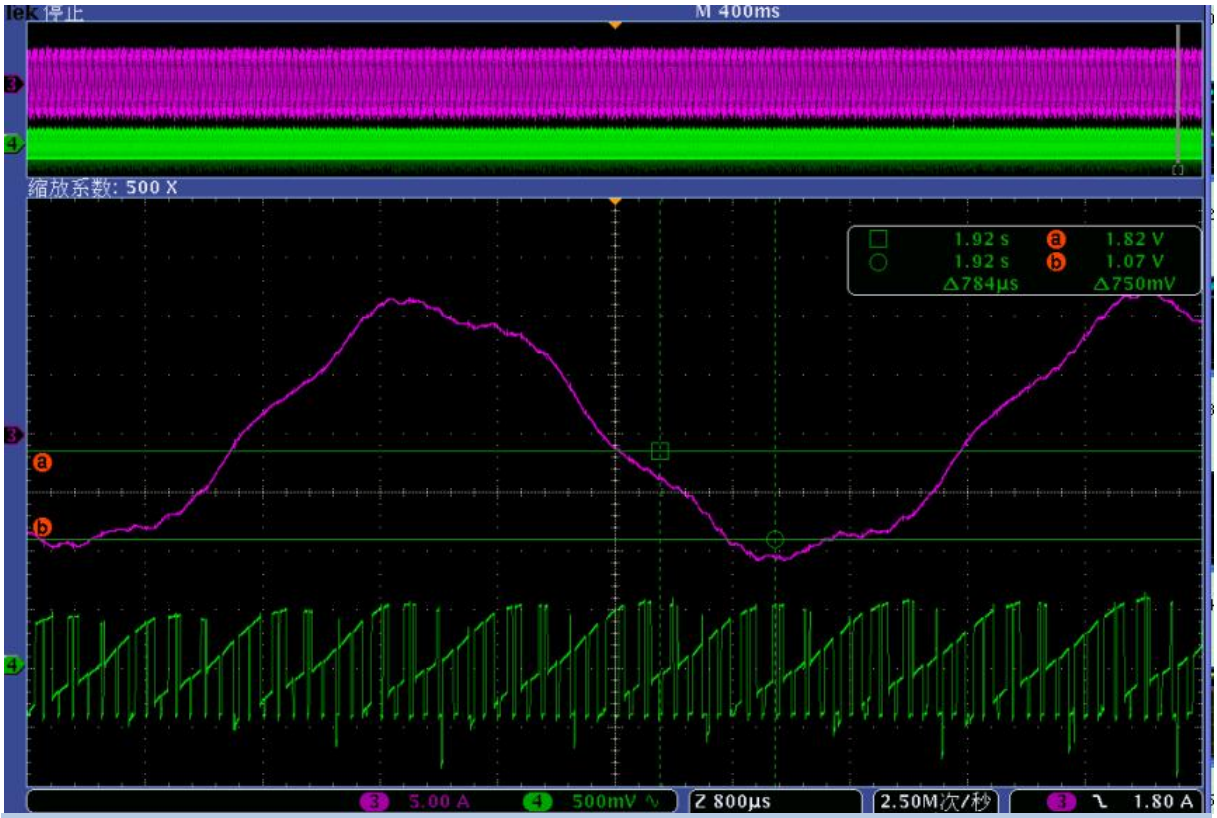
Figure 25. AD Trigger Point



4.1.7 Right Run Waveform Shown

Below shown the right detect and phase current and DC bus current.

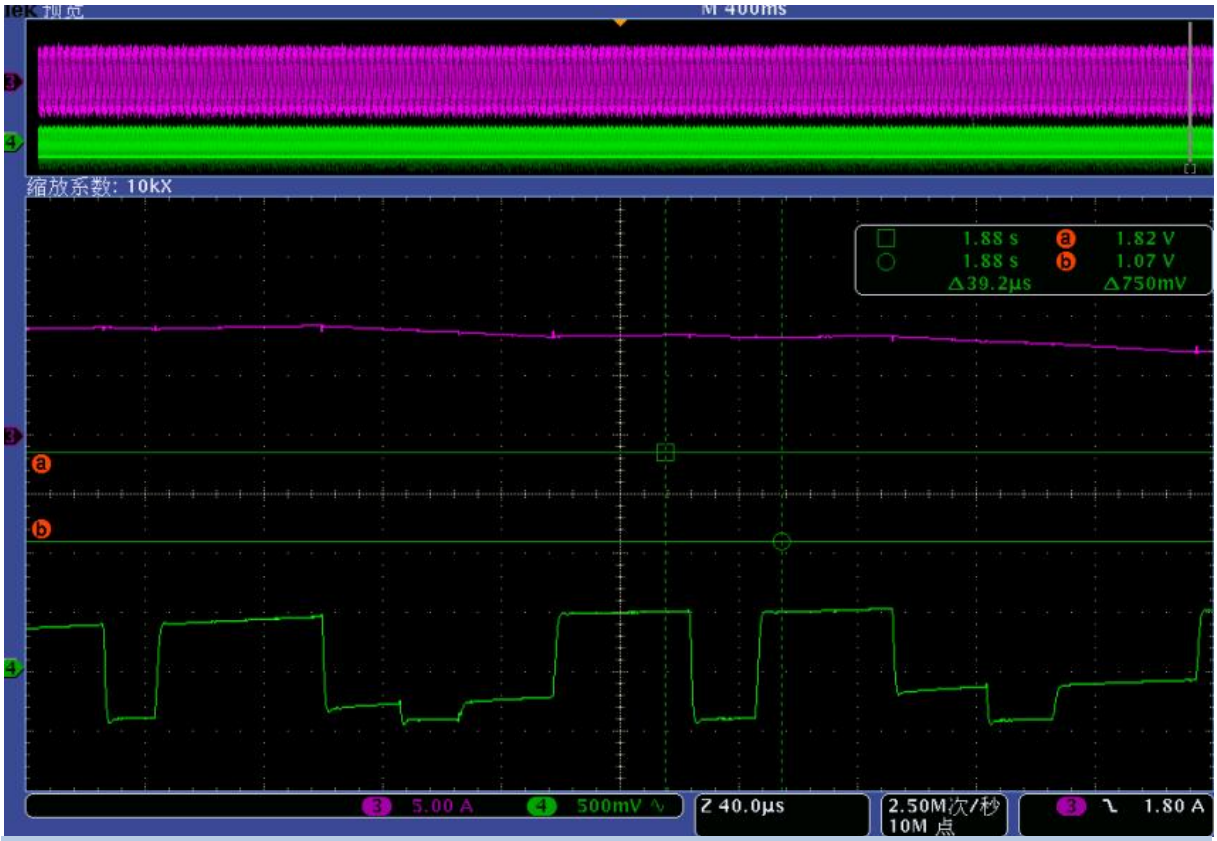
Figure 26. Phase Current and DC Bus Current



PHASE CURRENT:

BUS CURRENT:

Figure 27. Clear Phase Current and DC Bus Current



PHASE CURRENT:

BUS CURRENT:

Figure 28. At One Cycle Phase and DC bus current

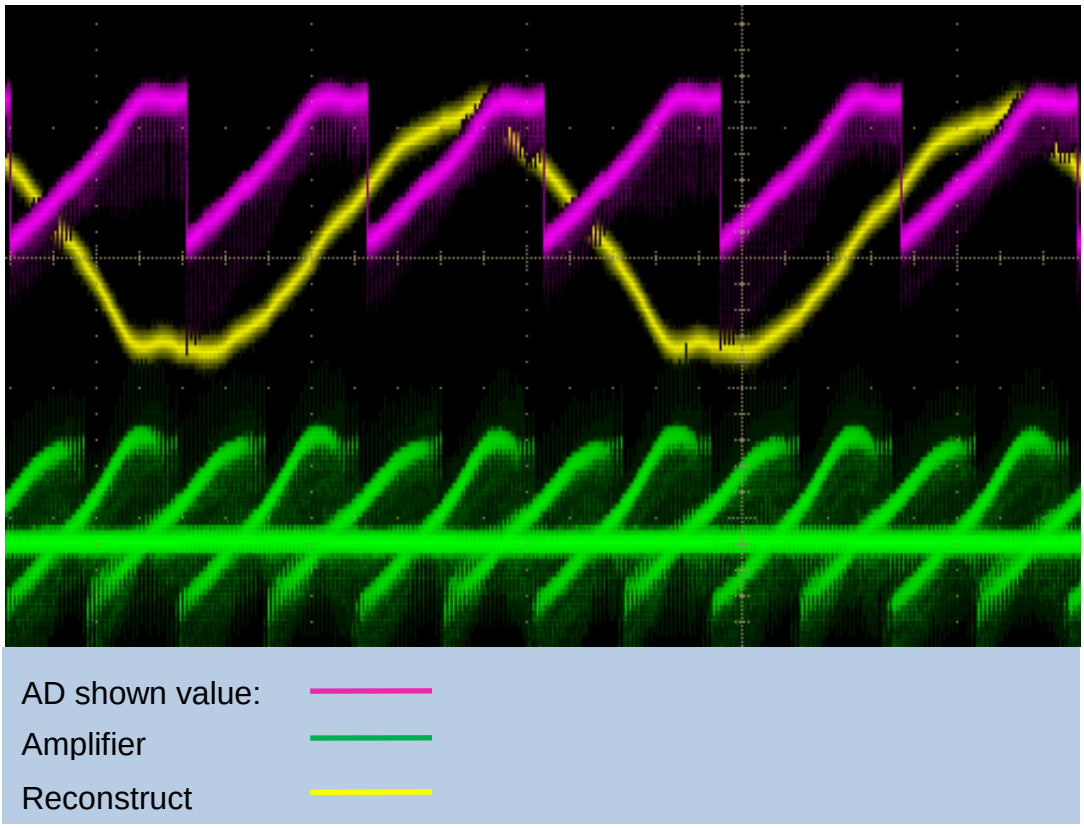
PHASE CURRENT:

BUS CURRENT:

4.1.8 AD Sample Veracity

AD sampling values are shown through DA board.

Figure 29. AD Current and DC bus Current



Red line shows AD sample current. Green line shows the output of amplifier. Only when ensuring the veracity of right AD sampling, reconstruct current can be similar to the real current, then speed and angle information can be calculated rightly.

5 Conclusion

This application note illustrates the advantages, limitations and constraints of the single-shunt algorithm. The single-shunt algorithm method is able to recreate the current flowing through the motor phases using a single-shunt resistor to sense the current flowing through the DC bus. In order to obtain the information contained in the DC bus current, Space Vector Modulation is used. SVM creates a series of sampling time windows that allows the observation of the current flowing through the motor phases. These time windows are classified and grouped in the shunt resistor truth table. This truth table shows the relationship between the information present at the shunt resistor versus the state of the electronic switches. However, it is not possible to obtain the desired information from the DC bus current in certain SVM areas. This limitation is overcome by modifying the SVM switching patterns. Modifying these patterns makes it possible to extract the desired information from the single-shunt resistor in every SVM operating state. These practical results demonstrate that the single-shunt resistor technique provides information accurate enough to meet the requirements of Field-Oriented Control. It is possible to obtain the motor information such as position and torque based on the reconstructed information extracted from the current flowing through the DC bus.

Document History

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Document Number: 002-05349

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	—	FCZH	07/02/2011	Initial release.
			06/07/2012	Changing Software Flowchart.
*A	5264548	FCZH	05/09/2016	Migrated Spansion Application note from MCU-AN-510110-E-11 to Cypress format.
*B	5843056	AESATMP9	08/03/2017	Updated logo and copyright.

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