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AN205316

FR, MB91460, Pulse Frequency Modulator

The PFM is used to generate pulses of a short duration in a long period. This is an alternative to using PWM signals in some applications. The 16-bit pulse frequency modulator consists of two 16-bit down-counters, two 16-bit reload registers, pre-scalars for generating the internal count clocks and control/status registers.

Contents

1 Introduction

The PFM is used to generate pulses of a short duration in a long period. This is an alternative to using PWM signals in some applications.

The 16-bit pulse frequency modulator consists of two 16-bit down-counters, two 16-bit reload registers, pre-scalars for generating the internal count clocks and control/status registers.

1.1 Key Features

- Two independent programmable 16-bit down-counters generating low and high pulses
- The input clock (count clock) can be selected from pre-scaled internal clocks (the peripheral clock (CLKP) divided by 2/8/32/64/128) separately for each counter.
- The mark level and output waveform can be inverted.

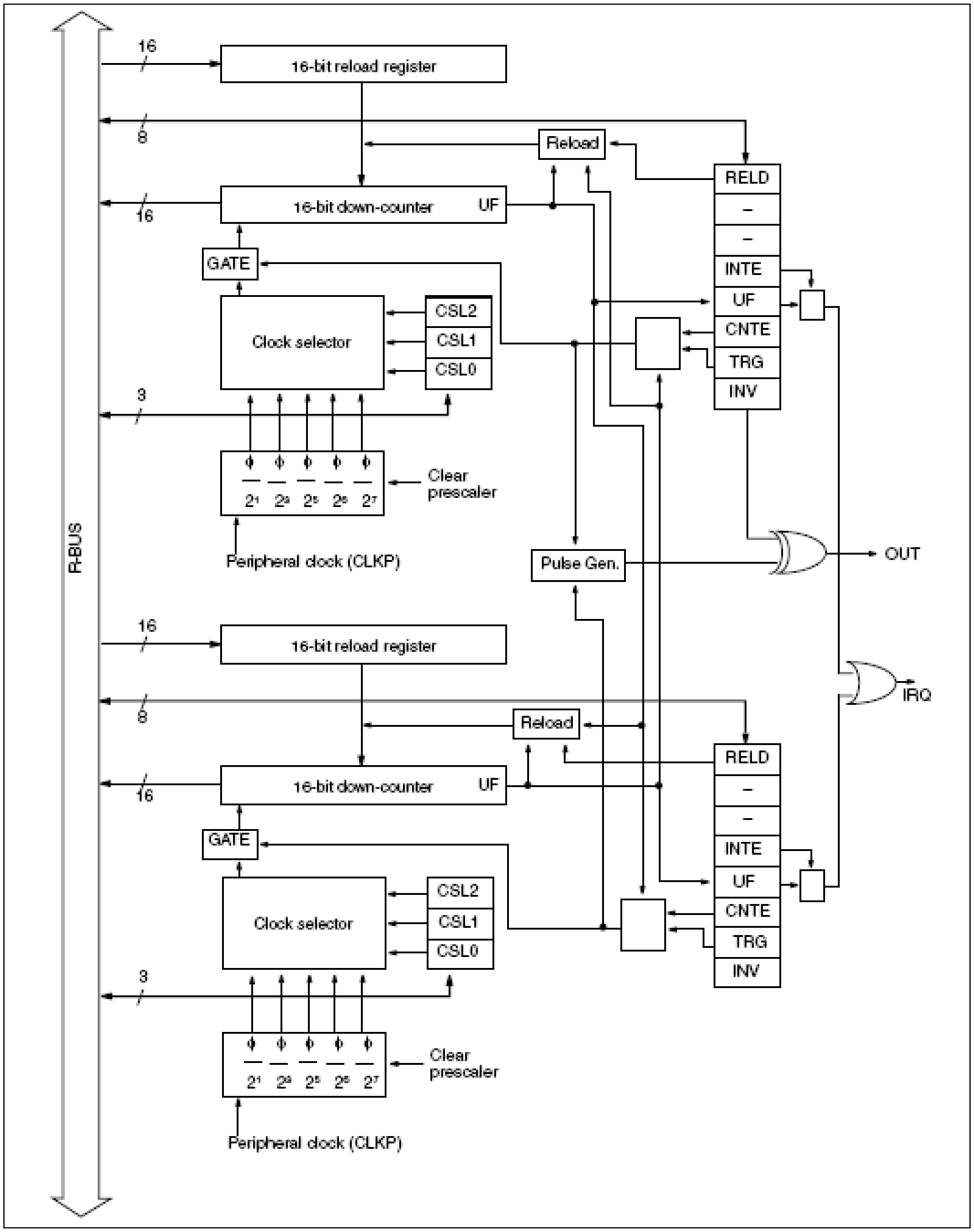
2 Pulse Frequency Modulator

The basic functionality of pulse frequency modulator is explained

2.1 Block Diagrams

Figure 1 shows the internal block diagram of a Pulse Frequency Modulator.

Figure 1. PFM Block Diagram



2.2 Registers

2.2.1 Control status register (P0TMCSR, P1TMCSR)

Controls the operation mode, shows the status of the reload counter and interrupts for the 16-bit reload. Only change the value of bits other than UF and TRG when CNTE = "0".

Table 1. P0TMCSR and P1TMCSR

Bit No.	Name	Explanation	Value	Operation
15	–	*Reserved*	-	*Always set to '0'*
14	INV	The output signal inversion bit	0	counter 0 high level, counter 1 low level
			1	counter 0 low level, counter 1 high level
13	–	*Reserved*	-	*Always set to '0'*
12-10	CSL2, CSL1, CSL0	The count clock select bits	000	CLKP / 2^1
			001	CLKP / 2^3
			010	CLKP / 2^5
			011	*resaved*
			100	Clock disabled
			101	CLKP / 2^6
			110	CLKP / 2^7
			111	Clock disabled
9	–	*Reserved*	-	*Always set to '0'*
8	MD1	Mode Bit	0	Setting prohibited
			1	Necessary for PFM operation
7-5	–	*Reserved*	-	*Always set to '010'*
4	RELD	This bit enables reload operations.	0	The count operation stops when an underflow occurs due to underflow
			1	The counter operates in reload mode
3	INTE	Interrupt request enable bit	0	Interrupt request is generated when the UF bit changes to "1".
			1	no interrupt requests are generated
2	UF	Underflow flag	0	Read: No counter underflow Write: Clears the Flag
			1	Read: Counter underflow occurred Write: No effect
1	CNTE	Counter count enable bit	0	stops count operation
			1	sets the counter to wait for a trigger
0	TRG	Software trigger bit	0	Write: No effect
			1	Write: Software trigger applied

2.2.2 16-bit Counter Register (P0TMR, P1TMR)

Reading this register reads the count value of the 16-bit down counter. Its initial value is indeterminate. Always read this register using 16-bit data transfer instructions Output Compare Unit

2.2.3 16-bit Reload Register (P0TMRLR, P1TMRLR)

The 16-bit reload register stores the initial count value. Its initial value is indeterminate. Always write to this register using 16-bit data transfer instructions.

2.2.4 Port function register (PFRxx, EPFRxx)

To enable PFM output one should enable its corresponding port function register. Please refer data sheet of corresponding device for more information

2.3 PFM Counter Operation

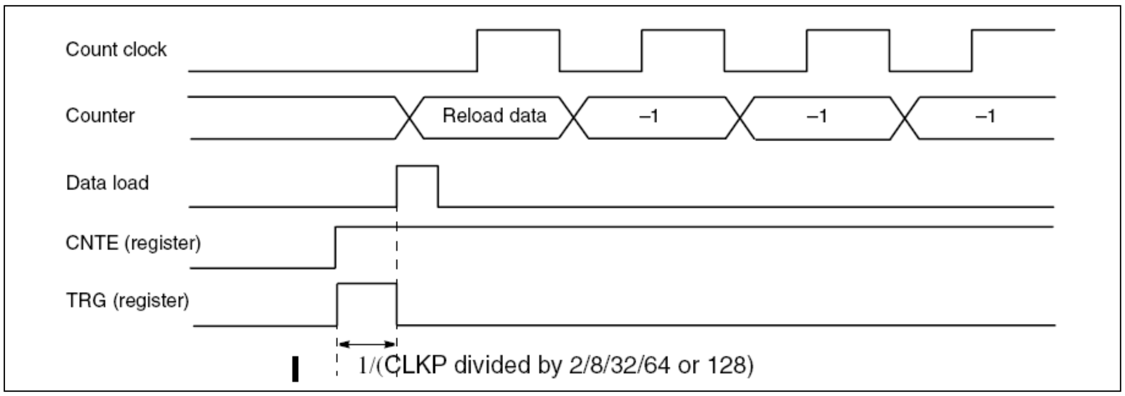
2.3.1 Reload Counter Operation

This section describes the operations of the 16-bit reload counter

The Peripheral Clock (CLKP) divided by 2, 8, 32, 64 or 128 can be selected as the clock source when operating the counter from an internal clock. Writing "1" to both the `CNTE` and `TRG` bits in the control status register enables and starts counting simultaneously.

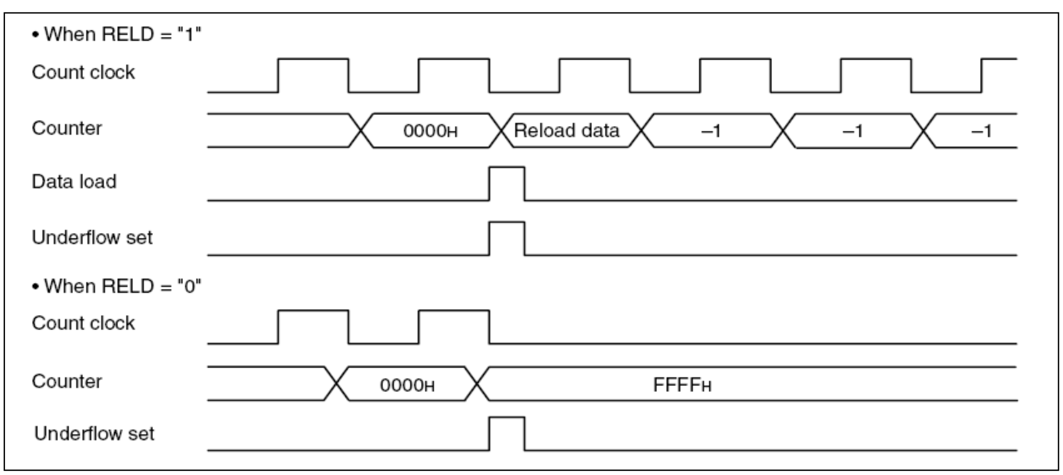
One clock cycle (CLKP divided by 2/8/32/64 or 128) is required from the counter start trigger

Figure 2. Counter activation and operation timing



An underflow occurs when the counter value changes from 0000H to FFFFH. Therefore, an underflow occurs after "reload register setting + 1" counts. If the RELD bit in the control register is "1" when the underflow occurs, the contents of the reload register are loaded into the counter and counting continues. When RELD is "0", counting stops with the counter at FFFFH. The UF bit in the control register is set when the underflow occurs. If the INTE bit is "1" at this time, an interrupt request is generated.

Figure 3. Underflow Operation Timing



2.3.2 PFM Operation and Setting

This section describes the following operations of the 16-bit pulse frequency modulator (combining the functionality of both reload counters).

The underflow output of reload counter channel 0 is connected internally to the trigger input reload counter channel. The underflow output of reload counter channel 1 is connected internally to the trigger input of reload counter channel 0.

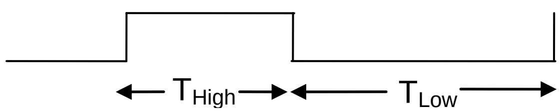
Both counters must be set up with RELD = “0”. Counter 0 should then be started by software trigger TRG = “1”. By starting counter 0 a high level is generated at the output. At the underflow condition of counter 0, counter 1 is automatically reloaded and started by the internal trigger (falling edge, set MOD1 = “1” for both counters) and a low level is generated at the output. At the underflow condition of counter 1, counter 0 is automatically reloaded and started by the internal trigger and a high level is generated at the output.

Interrupts can be set up on underflow condition of counter 0, counter 1 or both. The interrupts of counter 0 and counter 1 are combined together (logical OR).

The default output is low level if both CNTE = “0”, and both INV = “0”.

2.4 Calculation

If we need to generate a following waveform with T_{High} = 20ms and T_{Low} = 100ms



We can calculate T_{High} as,

T_{High} = (P0TMRLR + 1) * (1/ (CLKP/ P0TMCSR: CTS))

Let us assume CLKP is 16MHz and P0TMCSR: CTS is B’010

Than,

T_{High} = (P0TMRLR + 1) * (1/ (16MHz/32))

I.e. P0TMRLR = (20ms / (2µS)) + 1 = 10001

Similarly,

T_{Low} = (P1TMRLR + 1) * (1/ (CLKP/ P1TMCSR: CTS))

Let us assume P1TMCSR: CTS is B’101

Than,

T_{Low} = (P0TMRLR + 1) * (1/ (16MHz/64))

I.e. P0TMRLR = (100ms / (4µS)) + 1 = 25001

3 Software Example

Example for pulse frequency modulator

3.1 Basic Functionality of the PFM

The following example shows how to set up the Pulse Frequency Modulator.

```
/*                                SAMPLE CODE                                    */
/*---------------------------------------------------------------------------*/
void InitPFM(void)
{
   PFR16_D6 = 1;
   EPFR16_D6 = 1;
   P0TMRLR = 0x2711;       //Reload Register
   P0TMCSR_INV = 0; //default level
   P0TMCSR_CSL = 2; //CLKP / 2^5
   P0TMCSR_MOD1 = 1;       //PFM operation
   P0TMCSR_RELD = 0;   //Count operation stops when an underflow occurs
   P0TMCSR_INTE = 1;       //Interrupt enabled
   P0TMCSR_UF = 0;  // Clear underflow flag
   P0TMCSR_CNTE = 1;   //sets the counter to wait for a trigger

   P1TMRLR = 0x61A9;       //Reload Register
   P1TMCSR_INV = 0; //default level
   P1TMCSR_CSL = 5; //CLKP / 2^6
   P1TMCSR_MOD1 = 1;       //PFM operation
   P1TMCSR_RELD = 0;   //Count operation stops when an underflow occurs
   P1TMCSR_INTE = 1;       //Interrupt enabled
   P1TMCSR_UF = 0;  // Clear underflow flag
   P1TMCSR_CNTE = 1;  //sets the counter to wait for a trigger

   P0TMCSR_TRG = 1;   //TRG applies a software trigger

}
__interrupt void PFMIRQHandler (void)
{
   if(P0TMCSR_UF == 0)
   {
      P0TMCSR_UF = 0;
   }
   else if(P1TMCSR_UF == 0)
   {
      P1TMCSR_UF = 0;
   }
   else
   {
      P1TMCSR_UF = 0;
```

4 Additional Information

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http://www.cypress.com/cypress-microcontrollers

The software examples related to this application note is:

91460_PFM

It can be found on the following Internet page:

http://www.cypress.com/cypress-mcu-product-softwareexamples

Document History

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**	-	NOFL	06/05/2008	V1.0, First draft, HPi
*A	5090527	NOFL	04/12/2016	Converted Spansion Application Note “MCU-AN-300065-E-V10” to Cypress format
*B	5873413	AESATMP9	09/05/2017	Updated logo and copyright.

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