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FR, MB91460, External Interrupts

This application note describes the functionality of the External Interrupts and gives some examples.

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1 Introduction

This application note describes the functionality of the External Interrupts and gives some examples.

1.1 Key Features

The external interrupts have the following features:

- Edge rising and falling selectable
- Level low and high selectable
- A minimum pulse width of >50ns while waking up from STOP mode with edge detection
- A minimum pulse width of 3 peripheral clock cycle for detection of edge
- Up to 16 channels



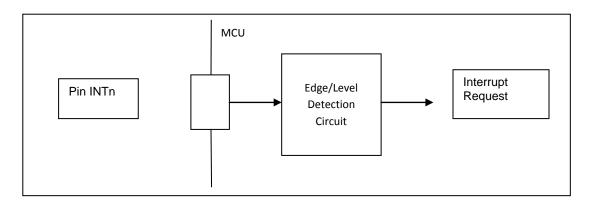
2 External Interrupts

The basic functionality of the external interrupt module

2.1 Block Diagram

Figure 1 shows the internal block diagram of an External Interrupt channel.

Figure 1. External Interrupts Block Diagram



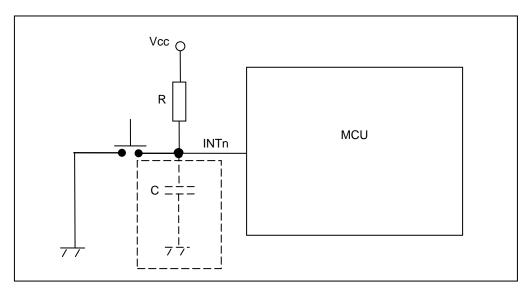
2.2 Connection Diagram

Figure 2 shows the connection diagram depicting how the external interrupt pin INTn is interfaced to the external circuitry.

The pull up resistor R is connected to limit the current when the key is pressed. The capacitor (hardware debounce) circuit shown with the dotted line is optional and is used to eliminate the bouncing of the switch. The RC time constant needs to be chosen according to the bouncing time or debounce delay of the switch. If such arrangement is not used then the bouncing needs to be taken care in the software and also vice a versa.

Here the INTn needs to be configured to detect a falling edge.

Figure 2. External Interrupts Connection Diagram





2.3 Register

2.3.1 External Interrupt Enable Register (ENIRO/1)

These 8 bit registers contain the interrupt enable bits for each external interrupt channel. Writing '1' to these bits enables the corresponding external interrupt requests.

2.3.2 External Interrupt Request Register (EIRR0/1)

These 8 bit registers contain the flag which is set if the specified interrupt event occurs at the corresponding external interrupt pin. Writing "0" to it clears the request. The interrupt request bit must be cleared by the ISR. These flags can also be used for polling if the corresponding Interrupt Enable bit is disabled.

2.3.3 Request Level Setting Register (ELVR0/1)

These 16 bit registers contain a pair of control bits LBx:LAx for each channel for the detection type. The following table shows the possible settings:

Table 1. ELVR

LBx	LAx	Functionality
0	0	"L" Level Input
0	1	"H" Level Input
1	0	Rising Edge Pin Input
1	1	Falling Edge Pin Input

Where x = 0 to 7 for ELVRO and 8 to 15 for ELVR1

3 External Interrupt Timing

The following figure shows timing of events for external interrupt. Here it is considered that external interrupt pin INTn is configured to detect falling edge.

INTn 2 CLKP cycles Minimum 6 External Time required for delay for noise CPU to finish CPU cycles interrupt ISR for context execution current instruction filterina saving **CPU** starts First falling External **CPU** finishes external edge at interrupt current interrupt external recognized by execution and starts interrupt ISR interrupt input CPU context saving execution

Figure 3. External Interrupt Timing

Time required for CPU to finish the current instruction execution is dependent on type of instruction being executed.

Time required for the context saving is dependent on various factors. Those are described in section 2.4.1 of Interrupts application note MCU-AN-300055. The above mentioned time of 6 cycles is the minimum timing required for context saving.

Time required to detect a valid edge depends on level of INT signal, the time window is two CLKP cycles before and two CLKP cycle after the falling edge. In case of STOP mode the trigger pulse must be > 50ns.



4 External Interrupt Examples

Examples for External Interrupts

4.1 Basic Functionality

The following example shows how to set up the External Interrupt Channel 0 of the MB91460 Series.

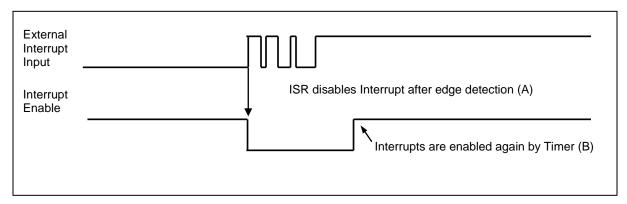
Please note, that the corresponding interrupt vector and level has to be defined in the *vectors.c* module of our standard template project.



4.2 Disturbed Signals

If signal on an External Interrupt input pin is disturbed (such as from a bouncing switch), it is recommended to use edge detection instead of level sensitivity. Also, if the bouncing of the switch needs to be taken care in the software (i.e. the optional capacitor as shown the Figure 4 is not used), then the external interrupt service routine should disable the interrupt for a time slot greater than the bouncing time. This can be done by a further interrupt using a timer (e.g. Reload Timer 0).

Figure 4. Interrupt Timing - Disturbed Input Signal



This mechanism prevents the application from multiple unwanted interrupts during "bouncing time". The same is accomplished using the software for the External Interrupt Channel 0 of the MB91460 Series in the example on the next page.

In the below example, at the first rising edge of the signal at External Interrupt input pin INT0, the interrupt service routine IRQHandler_EI0() will be executed and since the initial value of FLAG variable is TRUE, the Reload Timer RLT0 will be started (A in the above figure) and no further processing would happen.

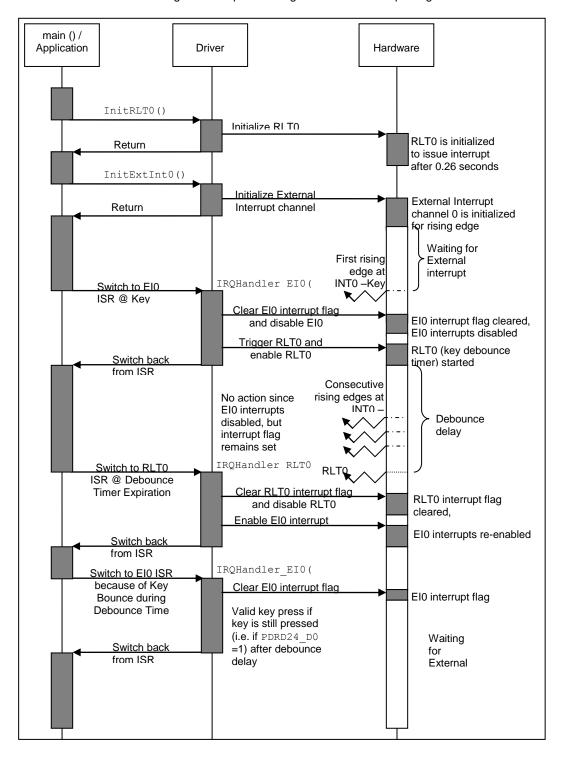
After 0.26 seconds (debouncing time, this can be chosen depending upon the type of key/switch) the interrupt service routine IRQHandle_RLT0() will be executed and it will enable External Interrupt request again and make value of FLAG variable FALSE. Now by this time (B in the above figure) since there are multiple edges already appeared at pin INT0, again interrupt service routine IRQHandler_EI0() will be executed. Within this interrupt service routine value of FLAG variable will be made TRUE for the next key press and then the user can do the desired processing considering a "valid" key press, if the key is still pressed (i.e. if PDRD24_D0 =1).

It should be noted that the above mentioned logic would work properly only when the key bounces a few times before settling at a position after a key press.



4.2.1 Sequence Diagram

Figure 5. Sequence Diagram - Disturbed Input Signal





```
/*
                                 SAMPLE CODE
/*----
#define TRUE
                 1
#define FALSE 0
volatile unsigned char FLAG = TRUE;
void InitExtInt0(void)
  DDR24_D0 = 0; // Port 24_0 Data direction as input
FR24_D0 = 1; // Enable Port 24_0 as an external interrupt input
ELVR0_LB0 = 1; // LB0, LA0 = 10 -> Rising edge
PFR24 D0 = 1;
   ELVR0_LA0 = 0;
   EIRRO_ERO = 0; // clear interrupt flag
ENIRO_ENO = 1; // enable interrupt request
      void InitRLT0(void)
{
   TMRLR0 = 0xFFFF; // Reload value (about 0.26 s @ 16 MHz)
   TMCSR0 = 0x0800; // Prescaler 1:64
void main(void)
{
   InitRLT0();  // initialize RLT0
InitExtInt0();  // initialize EXT0
   While (1);
 interrupt void IRQHandler EIO(void)
EIRRO ERO = 0;  // clear interrupt flag
  if (FLAG == TRUE)
TMCSR0_TRG = 1; // trigger Reload Timer 0
TMCSR0_INTE = 1;// enable Reload Timer 0 interrupt
else
{ FLAG = TRUE;
                       // for next key press
   if (1 == PDRD24 D0)// key still pressed?
                       // valid key press, take required action
}
  interrupt void IRQHandler RLT0 (void)
                      // clear Reload Timer 0
   TMCSR0 UF = 0;
   TMCSR0 INTE = 0;
                           // disable Reload Timer 0 interrupt
   ENIRO ENO = 1;
                           // enable External Interrupt request again,
                             // Figure 3-1:(B)
   FLAG = FALSE;
```



Please note, that the ISRs for the External Interrupts and the Reload Timer also has to be defined in vectors.c.

Also make sure that the RLT0 interrupt priority is higher than that of External Interrupt 0, in order to avoid nesting of interrupts.

4.2.2 External Interrupts and DMA

The user has to take special care when using DMA transfer triggered by an External Interrupt pin connected to disturbed signal source (as explained before in the section 4.2).

During the bouncing time of the switch, multiple DMA transfers can happen which is not desired. The DMA as such is not able to disable the interrupts during this bouncing time, so the software debounce mechanism discussed in section 4.2 cannot be realized in this case.

Hence it is required to use the capacitor (hardware debounce) circuit as shown in Figure 2. By using the same, the bouncing of the switch is eliminated at the hardware level itself and the clean signal (without noise) would appear at the external interrupt pin.



4.3 External Interrupts and Wake Up from Stop Mode

4.3.1 Example I

The following example shows, that External Interrupts can be used to request a stop mode and can wake up the MCU from this mode.

External Interrupt 0 is used to wake up the MCU and External Interrupt 1 is used to request a stop mode. Before stop mode "0x0F" is written to Port25, during run mode this Port is counting.



```
#define RUNMODE
#define STOPREQUEST 1
volatile unsigned int status, i;
void main (void)
 InitIrqLevels();
 __set_il(31);
                   // allow all levels
                   // globally enable interrupts
   EI();
 \overline{PORTEN} = 0x3;
                   /* enable I/O Ports */
                   /* This feature is not supported by MB91V460A */
                   /* For all other devices the I/O Ports must be enabled*/
                   // clear port data
 PDR25 = 0x00;
  DDR25 = 0xFF;
                   // set port 0 to output
 Init extint0();
  Init extint1();
 status = RUNMODE;
  while (1)
  \{ HWWD CL = 0;
   if (status == STOPREQUEST) // stop mode request
     PDR25 = 0x0F;
     STCR STOP = 1;
                               // goto stop mode
     STCR HIZ = 0;
                               // preserve output pin state
   else
                               // run mode
     for (i = 0; i < 50000; i++) // wait loop
       __asm(" NOP");
         _asm(" NOP");
       \overline{HWWD} CL = 0;
     PDR25++;
                              // show, that MCU is running
    }
 }
// ISR external Int 0
 interrupt void IRQ_extint0 (void)
   status = RUNMODE;
   EIRRO_ERO = 0;  // clear ext. int 0 request flag
                  // disable ext. int0
   ENIRO ENO = 0;
   EIRRO_ER1 = 0; // clear ext. int 1 request flag
   ENIRO EN1 = 1; // enable ext. int1
// ISR external Int 1
 interrupt void IRQ extint1 (void)
   status = STOPREQUEST;
   EIRRO_ERO = 0;  // clear ext. int 0 request flag
   ENIRO_ENO = 1;  // enable ext. int0
   EIRRO_ER1 = 0;  // clear ext. int 1 request flag
   ENIRO_EN1 = 0; // disable ext. int1
 }
```



Please note, that the corresponding interrupt vector and level has to be defined in the *vectors.c* module of our standard template project.



4.3.2 Example II

The following example shows to request a stop mode and to wake the MCU up from this mode using External Interrupt 0. After the MCU is in stop mode, if the falling edge appears at External Interrupt 0 pin, then the MCU wakes up and continues executing the program. There is no need to have an interrupt service routine in this case.

```
SAMPLE CODE
/*----
                                                             _ * /
// Initialise external int 0
void Init extint0 (void)
             // Port 24 0 Data direction as input
DDR24 D0 = 0;
PFR24 D0 = 1;
             // Enable Port 24 0 as an external interrupt input
ENIRO ENO = 0; // disable ext int 0
ELVR0 LA0 = 1;
// Request stop mode
void Request stop (void)
// globally disable interrupts
  DI();
              // globally disable interrupts
 EI();
void main (void)
 InitIrqLevels();
__set_il(7); // allow all levels
               // globally enable interrupt
 EI();
Init extint0();
Request_stop()
}
```



5 Additional Information

Information about Cypress Microcontrollers can be found on the following Internet page:

http://www.cypress.com/cypress-microcontrollers

The software examples related to this application note is:

91460_irq_ext

91460_irq_ext_stop_wakeup

It can be found on the following Internet page:

http://www.cypress.com/cypress-mcu-product-softwareexamples



Document History

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			04/23/2008	V1.1 MSt Chapter 3 External Interrupt Timing, Valid edge detection timing added
			09/30/2010	V1.2 RSchum Chapter 4: Typo in register naming corrected ELVRL0 -> ELVR0 Disclaimer changed Company name changed
*A	5085785	NOFL	04/06/2016	Converted Spansion Application Note "MCU-AN -300056-E-V12" to Cypress format
*B	5869301	AESATMP9	08/31/2017	Updated logo and copyright.



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