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AN205261

FR, MB91460, Reset

This application note describes the reset flow on MB91460.Depending on reset cause (Power ON, external reset pin input, Watchdog reset or software reset) the MCUs of MB91460 Series run through two different reset states: INIT reset state (Settings Initialization Reset) and RST reset state (Operation Initialization Reset).

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1 Introduction

This application note describes the reset flow on MB91460.

Depending on reset cause (Power ON, external reset pin input, Watchdog reset or software reset) the MCUs of MB91460 Series run through two different reset states: INIT reset state (Settings Initialization Reset) and RST reset state (Operation Initialization Reset).

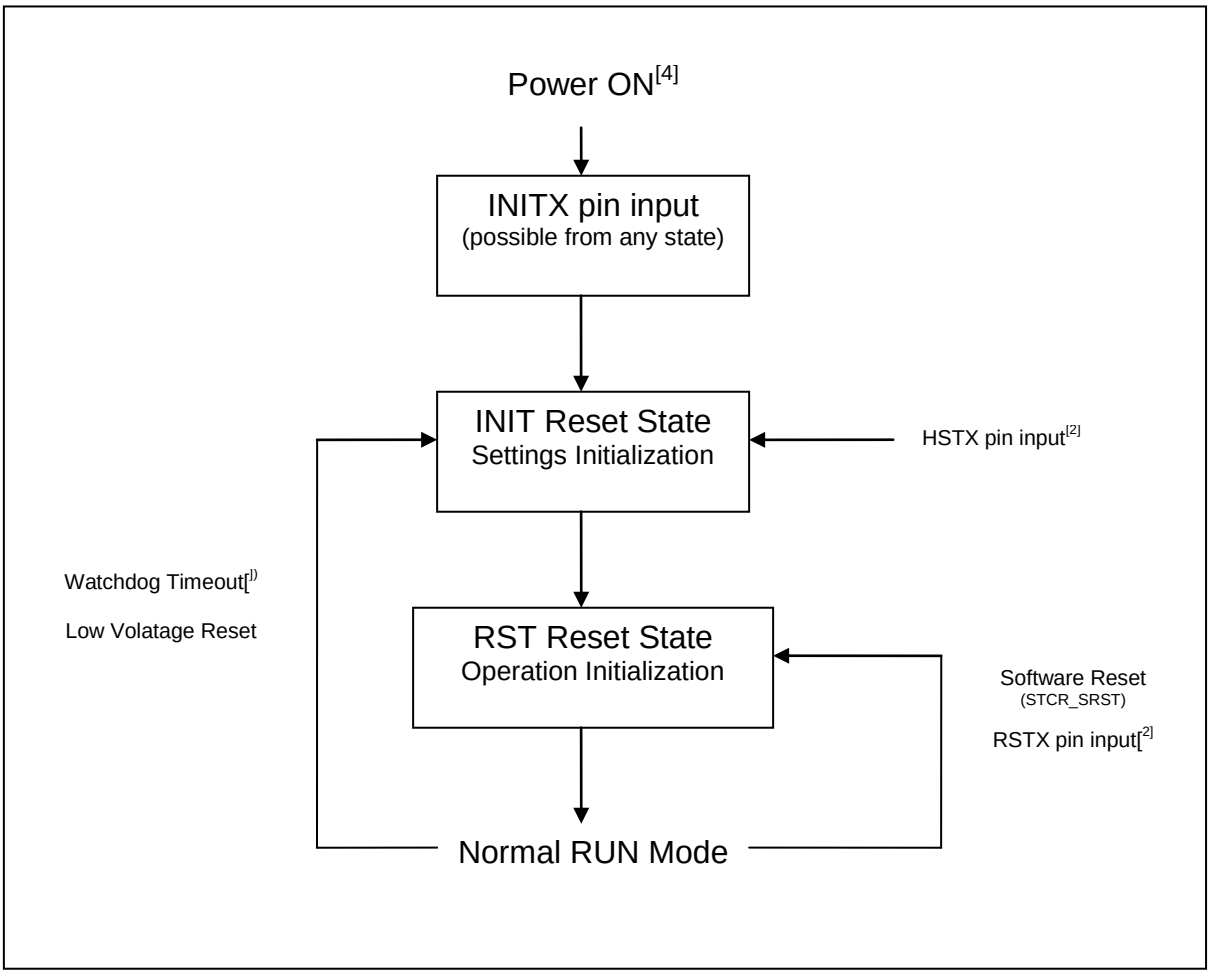
In the following the operations performed in the two above mentioned reset states are described and the flow through these states is explained. In addition information about how to determine the reset cause will be given.

2 Reset Flow and Reset Causes

This Chapter gives an overview about the flow through the different reset states and how these states can be invoked.

2.1 Reset Flow

Figure 1. Reset Flow



1. When INIT Reset State was entered due to Watchdog Timeout the setting of the oscillation stabilization time (STCR_OS[1:0]) are not changed
2. External RSTX pin is not supported by some of the MB91460 devices
3. External Hardware Standby input pin HSTX is not supported by some of the MB91460 devices. On devices supporting HSTX the setting of the oscillation stabilization wait time (STCR_OS[1:0]) depends on the order of releasing HSTX and INITX pin (for details please see of this document).
4. After power on the INITX input pin has to be kept low until the oscillation of the external oscillator has stabilized.

3 INIT Reset State

INIT Reset is used to initialize settings of the controller. In the following a description of the initialization steps is given.

3.1 How to enter INIT Reset State

The INIT Reset state is entered by:

- Pulling INTIX to low level a)
- Pulling HSTX to low level (when supported by the specific MB91460 Series MCU)
- Low Voltage Reset (for details about the setup of the Low Voltage Reset/Interrupt please refer to the Hardware Manual of MB91460 Series)
- Watchdog Reset generated by Hardware Watchdog (RC oscillator driven) or by Software Watchdog (Timebase Timer driven) (for details about the two Watchdog types please refer the Hardware Manual of MB91460 Series)

a) At Power on the INITX pin must be kept at low level until the external oscillator is started completely.

b) The oscillator start up time depends on the used oscillator, the circuit (e.g. the load capacities) and the PCB layout. The start up time has to be evaluated by the customer and the customer has to guarantee that the low level is supplied to the INITX input pin during this oscillator start up time.

3.2 Releasing the INIT Reset State request

The INIT Reset state request is released:

- Supply high level to INITX input pin c)
- Supply high level to HSTX input pin (when supported by the specific MB91460 Series MCU)

c) In case of Power On please keep the oscillator start up time in mind when releasing the INITX input pin to high level (please refer to the above remark added for the signal supplied to INITX while oscillator start up at Power On).

3.3 Operations performed in INIT Reset State (INIT reset cancellation sequence)

- Configuration of clock settings to default settings (clock source is Main Clock, PLL disabled)
- Oscillation Stabilization time is set to default value (STCR_OS[1:0] = b'00) d)
- Wait for oscillation stabilization wait time as specified by STCR_OS[1:0]
- Initialize Reset Cause Register RSRR e)
- Enter RST Reset State

d) Configuration of the oscillation stabilization wait time (STCR_OS[1:0]) to default settings is not done when INIT Reset State was entered due to Watchdog reset

e) A Watchdog Timeout will not initialize the Reset Cause Register.

4 RST Reset State

RST Reset is used to initialize the operation of the controller. In the following a description of the initialization steps is given.

4.1 How to enter RST Reset State

- Entered from previous INIT Reset State
- Apply low level to RSTX input pin
- Invoking a Software Reset by writing 0 to the SRST flag in the STCR register (for details about the Standby Control Register STCR please refer to the Hardware Manual of MB91460 Series)

4.2 Releasing the RST Reset State request

The RST Reset State request is released when the RST Reset state is entered.

4.3 Operations performed in RST Reset State (RST reset cancellation sequence)

- All MCU peripheral registers will be initialized to default values as described in the Hardware Manual of MB91460 Series. The clock setting registers will not be changed.
- Configuration of IO Ports to default values like all IO ports set to input, global port enable flag is cleared, … (for details refer to the Hardware Manual of MB91460)
- Evaluation of the setting of the Mode Pins MD[2:0] and setting up the device operating mode (bus mode and external bus width) correspondingly. Please find an overview of the device operation modes in the Hardware Manual of MB91460 Series.
- Set up of the CS0 Area to 0x00000000 – 0xFFFFFFFF (entire address range)
- Change to normal operation (RUN)
- Read Mode Vector from address 0x000FFFF8 (depending on the Mode Pin setting and the used MB91460 Series MCU the Mode Vector address might be in the internal ROM area or in the external ROM area)
- Write Mode Vector to Mode Register (MODR)
- Read Reset Vector from address 0x000FFFFC (depending on the Mode Pin setting and the used MB91460 Series MCU the Mode Vector address might be in the internal ROM area or in the external ROM area). The bus width which is used for the access to the Reset Vector is defined by the previously read Mode Vector.
- Write Reset Vector to PC (Program Counter) and start program execution

4.4 RST Reset Operation Modes

For the RST Reset operation two modes are possible: Normal (asynchronous) Reset Operation or Synchronous Reset Operation.

The RST Reset Operation mode is selected by the SYNCR-flag in the Timebase Timer Control Register TBCR.

Figure 2. Register TBCR

- **TBCR: Address 0482h (Access: Byte)**

7	6	5	4	3	2	1	0	bit
TBIF	TBIE	TBC2	TBC1	TBC0	---	SYNCR	SYNCS	
0	0	X	X	X	X	0	0	Initial value (INITX pin, watchdog)
0	0	X	X	X	X	X	X	Initial value (Software reset)
R(RM1),W	R/W	R/W	R1,W	R/W	RX/WX	RX/WX	R/W	Attribute

For details on the Timebase Timer Control Register TBCR please refer to the Hardware manual of the MB91460 Series.

4.4.1 Normal (Asynchronous) RST Reset Operation

Normal reset operation refers to the mode when the device goes to the operation reset (RST) state immediately after an operation reset (RST) request occurs. For a normal reset, the device changes to the reset (RST) state immediately after a reset (RST) request is received regardless of the current state of internal bus access.

In normal reset mode, the result on any bus operation that is in progress at the time the device changes state is not guaranteed. However, acceptance of the operation reset (RST) request is guaranteed.

4.4.2 Synchronous RST Reset Operation

Synchronous RST reset operation refers to the mode when the device does not go to the operation reset (RST) state after an operation reset (RST) request until all bus access has halted.

In synchronous RST reset mode, the device does not go to the RST reset state when a RST reset request is received if internal bus access is still in progress. When such a RST reset request is received, a sleep request is issued to the internal bus. The device does not change to the operation reset RST state until all buses have shutdown operation and changed to SLEEP state.

In synchronous reset mode, the results of bus operations are guaranteed because the device does not change state until all bus access has halted. However, if bus access should not halt for some reason, no requests can be received while bus operation continues. In such case, the settings initialization reset (INIT) remains available at any time.

The following lists cases in which bus access may not stop:

- If bus wait is enabled due to continuous input of RDY (ready request) to the external expansion bus interface.

5 Evaluation of the Reset Cause

The Reset Cause Register can be used by an application to keep track of the cause of last reset.

5.1 Reset Cause Register RSRR

Figure 3. Register RSRR

- **RSRR: Address 0480h (Access: Byte, Half-word)**

7	6	5	4	3	2	1	0	bit
INIT	HSTB	WDOG	ERST	SRST	LINIT	WT1	WT0	
1	0	0	0	0	0	0	0	Initial value (INITX pin input)
-	-	-	X	X	-	0	0	Initial value (Watchdog reset)
X	X	X	-	-	X	0	0	Initial value (Software reset)
R/WX	R/WX	R/WX	R/WX	R/WX	R/WX	R/W	R/W	Attribute

INIT: INIT Reset occurred due to INITX pin input or Hardware Watchdog Timeout[A)].

HSTB: INIT Reset occurred due to HSTX pin input.

WDOG: INIT Reset occurred due to Software Watchdog Timeout.

ERST: RST Reset occurred due to RSTX pin input.

SRST: RST Reset occurred due to Software Reset (STCR_SRST).

LINIT: INIT Reset occurred due to Low Voltage Reset.

A) When the INIT-flag in the RSRR register is set it is necessary to check the Hardware Watchdog control register HWWD also to distinguish between INITX pin input reset and Hardware Watchdog Timeout. For details on HWWD please refer to point 0 of this document and to the hardware manual of MB91460 Series.

The RSRR register is cleared after the first read. Since the RSRR is already evaluated by the BootROM when the MB91460 MCU is started in Single Chip Mode (pins MD[2:0]=b'000) the BootROM will provide the original content of RSRR in the CPU register R4 at application start and a copy of the original RSRR content can be found at a device specific RAM address. For the RAM address at which the RSRR content is stored please refer to the datasheet of the used MB91460 device.

For details on the Reset Cause Register RSRR please refer to the Hardware manual of the MB91460 Series

5.2 Hardware Watchdog Control Register HWWD

Figure 4. Register RSRR

- **HWWD: Address 04C7h (Access: Byte)**

7	6	5	4	3	2	1	0	bit
RESV0	RESV0	RESV0	RESV1	CL	RESV0	RESV0	CPUF	
0	0	0	1	1	0	0	0	Initial value (INITX pin input, watchdog reset)
0	0	0	1	1	0	0	X	Initial value (Software reset)
R/W0	R/W0	R/W0	R/W1	W	R/W0	R/W0	R/W	Attribute

CPUF: When the last reset occurred due to a Hardware Watchdog Timeout the CPUF-flag in the Hardware Watchdog control register is set while in the RSRR register (please refer to point 5.1) only the INIT-flag is set. The CPUF-flag has to be cleared by the application.

For details on the Hardware Watchdog control register HWWD please refer to the Hardware manual of the MB91460 Series.

6 Hardware Standby input HSTX

This chapter describes the function of the Hardware Standby input pin HSTX.

Hardware Standby is intended to halt the complete MCU including also the external oscillators.

6.1 Influence of HSTX/INITX on Oscillation Stabilization Wait Time

Releasing the Hardware Standby Mode also the signal input to the oscillation stabilization wait time STCR_OS[1:0] is configured depending on the state of the INTX input pin:

- OS[1:0]=b'00 when INITX input pin is at low level while releasing HSTX from low to high
- OS[1:0]=b'11 when INITX input pin is at high level while releasing HSTX from low to high

Please see the below table for the resulting oscillation stabilization wait times depending on the setting of STCR_OS[1:0]

Table 1. STCR: OS bits

OS[1:0]	The oscillation stabilization wait time after a reset (INIT) or on recovering from STOP state.		
	Oscillation stabilization wait time	When using Main clock (For a 4.0MHz Main clock)	When using Sub clock (For a 32.768kHz Sub clock)
00	$\Phi \times 2^{1}$	1.00µs	61µs
01	$\Phi \times 2^{11}$	1.0ms	62.5ms
10	$\Phi \times 2^{16}$	32ms	2.0s
11	$\Phi \times 2^{22}$	2s	128s

The Hardware Standby input pin HSTX is not supported by some of the MB91460 devices.

7 Register initialisation of different Resets type

This chapter describes the register initialisation of different Reset type.

Information about reset initialisation of the different types can be found also in MB91460 series Hardware Manual, Chapter 8 Device State Transition and Chapter 9 Reset.

7.1 Register not initialised by Reset type

Depending of Reset type occurrence some registers / bits are not initialised to default value.

The following table lists the register with are different initialled by reset types, refer to Hardware manual for more details.

Table 2. Register not initialised by different Reset types

Reset type	Register not set to default value
INITX (pin) Reset	--
Hardware Watchdog Reset (HWWD)	STCR.OS[1:0] CSVCR, CSCFG HWWDE, HWWD
Clock Supervisor Reset	CSVCR, CSCFG
Software Reset (RST)	CLKR DIVR0/1 CSFG OSCCR STCR.OSCD[2:1], STCR.OS[1:0] TBCR.SYNCR, .SYNCS PLLDIVM PLLDIVN PLLDIVG PLLMULG PLLCTRL CANPRE RSRR HWWDE, HWWD OSCRH WTCR.ST LVDET REGCTR FSCR0/1 CSVCR, CSCFG

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Document History

Document Title: AN205261 - FR, MB91460, Reset

Document Number: 002-05261

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	NOFL	11/02/2007	V1.0 RSchum First draft
			06/24/2008	V1.1 HPi, Corrected formatting
			08/26/2010	V1.2 MSt, Added chapter 7, Changed information to new Company name, exchanged Disclaimer
*A	5084073	NOFL	01/16/2016	Converted Spansion Application Note “MCU-AN-300052-E-V12” to Cypress format
*B	5873197	AESATMP9	09/05/2017	Updated logo and copyright.

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