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AN205260

FR, MB91460, External Bus Interface

This Application Note describes how to achieve the maximum performance for external connected memories and how to connect the different types with the MB91460 series MCUs.The Application note is also covering the constraints which have to be taken into account for maximum bus frequencies and the selection of suitable memories for optimized performance.

Contents

1 Introduction

High flexibility to adapt MCUs to different and fast external memories in a variety of voltage levels is a customer demand. To meet this requirement the MB91460 Series MCUs provide a external bus interface with the capabilities to connect Flash, SRAM and SDRAM with up to 8 different chip select lines.

This Application Note describes how to achieve the maximum performance for external connected memories and how to connect the different types with the MB91460 series MCUs. The Application note is also covering the constraints which have to be taken into account for maximum bus frequencies and the selection of suitable memories for optimized performance.

1.1 Key Features

- **The External Bus Interface has the following features**
  - Addresses of up to 32 bits (4 GB space) can be output.
  - Various kinds of external memory (8-bit/16-bit/32-bit modules) can be directly connected and multiple access timings can be mixed and controlled.
  - Asynchronous SRAM and asynchronous ROM/FLASH memory (multiple write strobe method or byte enable method)
  - Page mode ROM/FLASH memory (Page sizes 2, 4, and 8 can be used)

- Burst mode ROM/FLASH memory (such as MBM29BL160D/161D/162D)
- Address/data multiplex bus (8-bit/16-bit width only)
- SDRAM (FCRAM modules are also supported, including two - and four – bank types with CAS latency 1 to 8)
- Synchronous memory (such as ASIC built-in memory) (Synchronous SRAM cannot be directly connected)
- Eight independent banks (chip select areas) can be set, and chip select corresponding to each bank can be output.
- The size of each area can be set in multiples of 64 KB (64 KB to 2 GB for each chip select area).
- An area can be set at any location in the logical address space (Boundaries may be limited depending on the size of the area.)

- **In each chip select area, the following functions can be set independently**
  - Enabling and disabling of the chip select area (Disabled areas cannot be accessed)
  - Setting of the access timing type to support various kinds of memory
  - Detailed access timing setting (individual setting of the access type such as the wait cycle)
  - Setting of the data bus width (8-bit/16-bit)
  - Setting of the order of bytes (big or little endian) (Only big endian can be set for the CS0 area)
  - Setting of write disable (read-only area)
  - Enabling and disabling of fetches from the built-in cache
  - Enabling and disabling of the prefetch function
  - Maximum burst length setting (1, 2, 4, 8)

- **A different detailed timing can be set for each access timing type**
  - For the same type of access timing, a different setting can be made in each chip select area.
  - Auto-wait can be set to up to 15 cycles (asynchronous SRAM, ROM, Flash, and I/O area).
  - The bus cycle can be extended by external RDY input (asynchronous SRAM, ROM, Flash, and I/O area).
  - The first access wait and page wait can be set (burst, page mode, and ROM/FLASH area).
  - Various kinds of idle/recovery cycles and setting delays can be inserted.
  - Capable of setting timing values such as the CAS latency and RAS - CAS delay (SDRAM area)
  - Capable of controlling the distributed/centralized auto - refresh, self - refresh, and other refresh timings (SDRAM area)

- **Fly-by transfer by DMA can be performed**.
  - Transfer between memory and I/O can be performed in a single access operation.
  - The memory wait cycle can be synchronized with the I/O wait cycle in fly-by transfer.
  - The hold time can be secured by only extending transfer source access.
  - Idle/recovery cycles specific to fly-by transfer can be set.

- **External bus arbitration using BRQ and BGRNT can be performed.**
- **Pins that are not used by the external interface can be used as general-purpose I/O ports through settings**.

2 The External Bus Interface

The basic functionality of the external bus interface

2.1 Outline

The External Bus Interface allows the user to connect external peripherals or memory to the MCU. The Bus consists of data, address and control signals. Various settings are possible for several bus timings.

2.1.1 Bus modes and access modes

- **Bus modes**

The bus mode controls internal ROM operation and the external access function. The bus mode is specified by the mode setting pins (MD2, MD1, and MD0) and internal ROM enable bit.

The FR-family CPU has the following three bus modes.

- Single chip mode

  In this mode, internal I/O, internal RAM, and internal ROM are available but access to other areas is disabled. External pins are used either by the peripheral functions or as general-purpose ports. Pins cannot be used as bus pins. This mode cannot be used when using the fixed mode/reset vector as implemented on most of the MB91460 series devices.

- Internal ROM, external bus mode

  In this mode, internal I/O, internal RAM, and internal ROM are available, and access to areas for which external access is enabled results in access to the external area. Some external pins function as bus pins.

- External ROM, external bus mode

  In this mode, internal I/O and internal RAM are available but access to internal ROM is prohibited. Access to internal ROM areas and areas for which external access is enabled results in access to the external area. Some external pins function as bus pins.

- **Access mode**

The access mode controls the width of the external data bus.

2.1.2 Address Maps Of Bus Modes

Figure 2-1 shows the different address maps for the three MCU bus modes for MB91F467DA.

Figure 2-1. Address maps of MB91F467DA bus modes

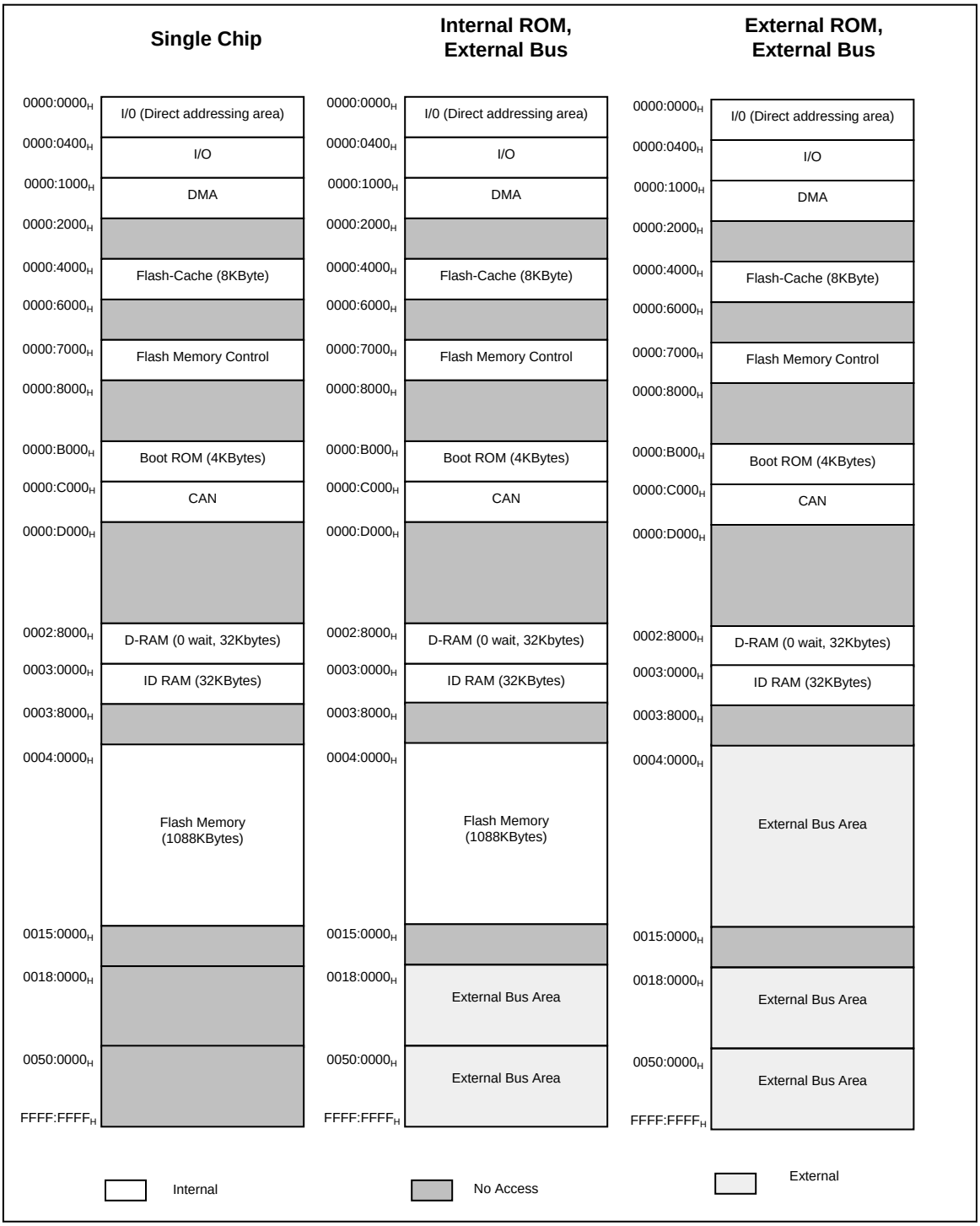
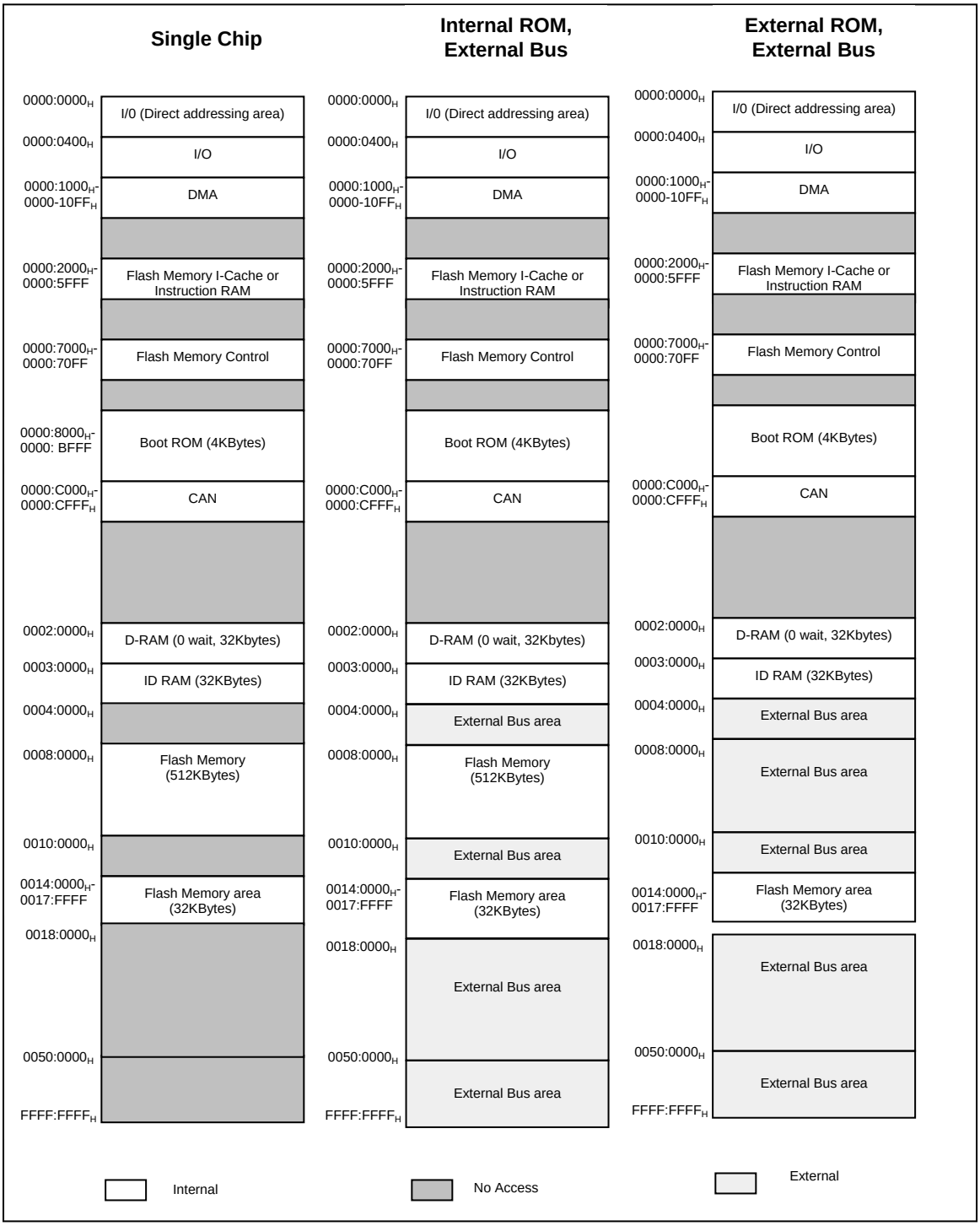


Figure 2-2. Address maps of MB91F467BA bus modes shows the different address maps for the three MCU bus modes for MB91F467BA.

Figure 2-2. Address maps of MB91F467BA bus modes



2.2 Registers

2.2.1 Area Select Registers (ASRn)

The Area Select Registers (ASR0-7) specifies the higher order bytes of start address of each chip select area of CSX0-CSX7.

Each chip select area starts with the address set in this register and covers the range set by the four bits ASZ3-0 of the Area Configuration Register (ACR0-7) registers.

Register	Initial Value
ASR0	0000_H
ASR1	$XXXX_H$
ASR2	$XXXX_H$
ASR3	$XXXX_H$
ASR4	$XXXX_H$
ASR5	$XXXX_H$
ASR6	$XXXX_H$
ASR7	$XXXX_H$

The ASR0 register is initialized to 0000_H by INIT and RST. ASR1-7 are not initialized by INIT and RST, and are therefore undefined. After starting chip operation, be sure to set the corresponding ASR register before enabling each chip select area with the CSER register.

Lets for example if we set ASR1 to 0x2000 than start address for CS1 will start from H’20000000

2.2.2 Area Configuration Registers 0-7 (ACRn)

Bit No.	Name	Explanation	Initial Value	Value	Operation
15-12	ASZ3:ASZ0	set area size	0000_B (ACR0) 1111_B (ACR1-7)	0000	64 KB (00010000H byte, ASR A[31:16] bits are valid)
				0001	128 KB (00020000H byte, ASR A[31:17] bits are valid)
				0010	256 KB (00040000H byte, ASR A[31:18] bits are valid)
				0011	512 KB (00080000H byte, ASR A[31:19] bits are valid)
				0100	1MB (00100000H byte, ASR A[31:20] bits are valid)
				0101	2 MB(00200000H byte, ASR A[31:21] bits are valid)
				0110	4 MB (00400000H byte, ASR A[31:22] bits are valid)
				0111	8 MB (00800000H byte, ASR A[31:23] bits are valid)
				1000	16 MB (01000000H byte, ASR A[31:24] bits are valid)
				1001	32 MB (02000000H byte, ASR A[31:25] bits are valid)
				1010	64 MB (04000000H byte, ASR A[31:26] bits are valid)
				1011	128 MB (08000000H byte, ASR A[31:27] bits are valid)
				1100	256 MB (10000000H byte, ASR A[31:28] bits are valid)
				1101	512 MB (20000000H byte, ASR A[31:29] bits are valid)
				1110	1024 MB (40000000H byte, ASR A[31:30] bits are valid)
				1111	2048 MB (80000000H byte, ASR A[31] bit isalid)
11-10	DBW1:0	set data bus width	XX_B	00	8 bits (byte access)
				01	16 bits (half word access)
				10	32 bits (word access)
				11	Reserved Setting
9-8	BST1:0	set the maximum burst length	XX_B	00	1 (single access)
				01	2 bursts (address boundary: 1 bit)
				10	4 bursts (address boundary: 2 bits)
				11	8 bursts (address boundary: 3 bits)
7	SREN	enable or disable sharing of chip select area by	X_B	0	Disable sharing by BRQ/BGRNTX

		RQ/BGRNTX		1	Enable sharing by BRQ/BGRNTX
6	PFEN	enable or disable pre fetching of chip select area	X_B	0	Disable pre fetch
				1	Enable pre fetch
5	WREN	enable or disable writing to each chip select area	X_B	0	Disable write
				1	Enable write
4	LEND*	sets endian	X_B	0	Big endian
				1	Little endian
3:0	TYP3:0**	set the access type	$XXXX_B$	00XX	Normal access
				01XX	Address data multiplex access
				0XX0	Disable WAIT insertion by the RDY pin
				0XX1	Enable WAIT insertion by the RDY pin
				0X0X	Use the WRX0-WRX3 pins as write strobes
				0X1X	Use the WEX pin as the write strobe
				1000	Memory type A: SDRAM/FCRAM
				1001	Memory type B: FCRAM
				1010	Setting disabled
				1011	Setting disabled
				1100	Setting disabled
				1101	Setting disabled
				1100	Setting disabled
				1111	Mask area setting

*CS0 supports only the big endian method

**Further information can be found in Appendix

2.2.3 Area Wait Register (AWRn)

The area wait registers (AWR0-7: Area Wait Register 0-7) specify various kinds of waits for each chip select area. The function of each bit changes according to the access type setting of the ACRn [TYP3:0] registers. More information about ACRn [TYP3:0] can be found in section 0

AWRn-register settings for ACRn [TYP3:0] is set to “SRAM” access type

TYP3	TYP2	TYP1	TYP0	Access Type
0	0	X	X	Normal access (asynchronous SRAM, I/O, and single/page/burst-ROM/FLASH)

Bit No.	Name	Explanation	Initial Value	Value	Operation
15-12	W15:12	set number of auto-wait cycles to be inserted into the first access cycle of each cycle.	0111_B (AWR0) $XXXX_B$ (AWR1-7)	0000_B	Auto-wait cycle 0
				0001_B	Auto-wait cycle 1
				.....	
				1111_B	Auto-wait cycle 15
11-8	W11:08	set the number of auto-wait cycles to be inserted into the in page access cycle during burst access	1111_B (AWR0) $XXXX_B$ (AWR1-7)	0000_B	Auto-wait cycle 0
				0001_B	Auto-wait cycle 1
				.....	
				1111_B	Auto-wait cycle 15
7:6	W07:06	The read -> write idle cycle is set to prevent collision of read data and write data on the data bus when a write cycle follows a read cycle.	11_B (AWR0) XX_B (AWR1-7)	00_B	0 Read -> write idle cycles
				01_B	1 Read -> write idle cycles
				10_B	2 Read -> write idle cycles
				11_B	3 Read -> write idle cycles
5:4	W05:04	The write recovery cycle is set if a device that limits the access period after write access is to be controlled	11_B (AWR0) XX_B (AWR1-7)	00_B	0 Write recovery cycles
				01_B	1 Write recovery cycles
				10_B	2 Write recovery cycles
				11_B	3 Write recovery cycles
3	W03	The WRX0-WRX3, WRXn output time setting selects whether to use write strobe output as an asynchronous strobe or synchronous write enable.	1_B (AWR0) X_B (AWR1-7)	0	MCLK synchronous write enable output (valid from ASX=L)
				1	Asynchronous write strobe output (normal operation)

2	W02	The address -> CSXn delay setting is made when a certain type of setup is required for the address when CSXn falls or CSXn edges are needed for successive accesses to the same chip select area.	0_B (AWR0) X_B (AWR1-7)	0	Assertion of CSX0-CSX7 starts at the same timing that ASX is asserted
				1	Assertion of CSX0-CSX7 starts when the external clock memory MCLK output rises
1	W01	The CSXn -> RDX/WRXn setup extension cycle is set to extend the period before the read/write strobe is asserted after CSXn is asserted.	1_B (AWR0) X_B (AWR1-7)	0	RDX/WRX0-WRX3/WRXn are output at the earliest when external clock MCLK output rises just after CSX is asserted
				1	RDX/WRX0-WRX3/WRXn are always output 1 cycle or more later
0	W00	The RDX/WRXn -> CSXn hold extension cycle is set to extend the period before negating CSXn after the read/write strobe is negated.	1_B (AWR0) X_B (AWR1-7)	0	CSX0-CSX7 are negated after the hold delay after it starts on the rising edge of external memory clock MCLK output after RDX/WRX0-WRX3/WRXn are negated.
				1	CSX0-CSX7 are negated one cycle later

AWRn-register settings for ACRn [TYP3:0] is set to “SDRAM” access type

TYP3	TYP2	TYP1	TYP0	Access Type
1	0	0	0	Memory type A: SDRAM/FCRAM (Auto - precharge is not used.)

Bit No.	Name	Explanation	Initial Value	Value	Operation
15	W15	Reserved			
14-12	W14:12	RAS - CAS delay Cycle	111_B (AWR0) XXX_B (AWR1-7)	000_B	1 RAS-CAS delay cycle
				001_B	2 RAS-CAS delay cycle
				.....	
				111_B	8 RAS-CAS delay cycle
11	W11	Reserved			
10:8	W10:08	Set CAS latency.	111_B (AWR0) XXX_B (AWR1-7)	000_B	1 cycles
				001_B	2 cycles
				.....	
				111_B	8 cycles
7-6	W07:06	Set minimum number of cycles from the last read data input cycle to the write command	11_B (AWR0) XX_B (AWR1-7)	00_B	1 cycles
				01_B	2 cycles
				10_B	3 cycles
				11_B	4 cycles
5:4	W05:04	Set minimum number of cycles from the last write data output to the next read command	11_B (AWR0) XX_B (AWR1-7)	00_B	Prohibited
				01_B	2 cycles
				10_B	3 cycles
				11_B	4 cycles
3:2	W03:02	Set minimum number of cycles for RAS active time	01_B (AWR0) XX_B (AWR1-7)	00_B	1 cycles
				01_B	2 cycles
				10_B	3 cycles
				11_B	4 cycles
1:0	W01:00	Set RAS pre charge cycles	11_B (AWR0) XX_B (AWR1-7)	00_B	1 cycles
				01_B	2 cycles
				10_B	3 cycles
				11_B	4 cycles

2.2.4 Memory Setting Register (MCRA)

The register serves as the area for making various settings for SDRAM/FCRAM connected to the chip select area for which the access type (TYP3 to TYP0 bits) in the ACR6 and ACR7 registers has been set as 1000_B

Bit No.	Name	Explanation	Initial Value	Value	Operation
31		Reserved			
30-28	PSZ2:0	sets page size of SDRAM	XXX_B	000_B	8-bit column address:A0 to A7(256 memory words)
				001_B	9-bit column address:A0 to A8(512 memory words)
				010_B	10-bit column address:A0 to A9(1024 memory words)
				011_B	11-bit column address:A0 to A9, A11(2048memory words)
				$1XX_B$	Prohibited
27	WBST	Select t burst - write or a single write access	X_B	0	Single write
				1	Burst write
26	BANK	Select number of SDRAM banks to be connected	X_B	0	2 banks
				1	4 banks
25-24	ABS1:0	Select maximum number of banks to be made active simultaneously	XX_B	00_B	1 banks
				01_B	2 banks
				10_B	3 banks
				11_B	4 banks

2.2.5 Memory Setting Register (MCRB)

The register serves as the area for making various settings for FCRAM connected to the chip select area for which the access type (TYP3 to TYP0 bits) in the ACR6 and ACR7 registers has been set as 1001_B

Bit No.	Name	Explanation	Initial Value	Value	Operation
23		Reserved			
22-20	PSZ2:0	sets page size of SDRAM	XXX_B	000_B	8-bit column address:A0 to A7(256 memory words)
				001_B	9-bit column address:A0 to A8(512 memory words)
				010_B	10-bit column address:A0 to A9(1024 memory words)
				011_B	11-bit column address:A0 to A9, A11(2048memory words)
				$1XX_B$	Prohibited
19	WBST*	Select t burst - write or a single write access	X_B	0	Single write
				1	Burst write
18	BANK	Select number of SDRAM banks to be connected	X_B	0	2 banks
				1	4 banks
17-16	ABS1:0	Select maximum number of banks to be made active simultaneously	XX_B	00_B	1 banks
				01_B	2 banks
				10_B	3 banks
				11_B	4 banks

*FCRAM supports neither burst read nor single write mode

2.2.6 I/O Wait Registers for DMAC (IOWRn)

The I/O wait registers for DMAC (IOWR0-3: I/O Wait Register for DMAC 0-3) set various kinds of waits during DMA fly-by access.

Bit No.	Name	Explanation	Initial Value	Value	Operation
31,23,15,7	RYEn	set wait control, using RDY, of channels 0-3 during DMAC fly-by access.	XB	0	Disable RDY input for I/O access
				1	Enable RDY input for I/O access
30,22,14,6	HLDn	control the hold cycle of the read strobe signal on the transfer source access side during DMA flyby access	XB	0	Do not insert a hold extension cycle.
				1	Insert a hold extension cycle to extend the read cycle by one cycle.
29-28, 21-20, 13-12, 5-4	WRn1:0	select burst - write or a single write access	XXB	00	0 cycle
				01	1 cycle
				10	2 cycle
				11	3 cycle
27-24, 19-16, 11-08, 03-00	IWn3:1	set number of auto-wait cycles for I/O access during DMA fly-by access	XXXXB	0000	0 cycle
				0001	1 cycle
				.....	
				1111	15 cycle

2.2.7 Chip Select Enable Register (CSER)

The chip select enable register (CSER: Chip Select Enable register) enables and disables each chip select area.

Bit No.	Name	Explanation	Initial Value	Value	Operation
31	CSE7	chip select enable bits for CSX0-CSX7	0	0	Disable
				1	Enable
30	CSE6		0	0	Disable
				1	Enable
29	CSE5		0	0	Disable
				1	Enable
28	CSE4		0	0	Disable
				1	Enable
27	CSE3		0	0	Disable
				1	Enable
26	CSE2		0	0	Disable
				1	Enable
25	CSE1		0	0	Disable
				1	Enable
24	CSE0		1	0	Disable
				1	Enable

2.2.8 Cache Enable Register (CHER)

The cache enable register (CHER: CacHe Enable Register) controls the transfer of data read from each chip select area.

Bit No.	Name	Explanation	Initial Value	Value	Operation
23	CHE7	enable or disable each chip select area for transfers to the built-in cache	1	0	Not a cache area (data read from the applicable area is not saved in the cache)
				1	Cache area (data read from the applicable area is saved in the cache)
22	CHE6		1	0	Not a cache area (data read from the applicable area is not saved in the cache)
				1	Cache area (data read from the applicable area is saved in the cache)
21	CHE5		1	0	Not a cache area (data read from the applicable area is not saved in the cache)
				1	Cache area (data read from the applicable area is saved in the cache)
20	CHE4		1	0	Not a cache area (data read from the applicable area is not saved in the cache)
				1	Cache area (data read from the applicable area is saved in the cache)
19	CHE3		1	0	Not a cache area (data read from the applicable area is not saved in the cache)
				1	Cache area (data read from the applicable area is saved in the cache)
18	CHE2		1	0	Not a cache area (data read from the applicable area is not saved in the cache)
				1	Cache area (data read from the applicable area is saved in the cache)
17	CHE1		1	0	Not a cache area (data read from the applicable area is not saved in the cache)
				1	Cache area (data read from the applicable area is saved in the cache)
16	CHE0		1	0	Not a cache area (data read from the applicable area is not saved in the cache)
				1	Cache area (data read from the applicable area is saved in the cache)

2.2.9 Pin/Timing Control Register (TCR)

The pin/timing control register (TCR: Terminal and Limiting Control Register) controls the functions related to the general external bus interface controller, such as the setting of common pin functions and timing control.

Bit No.	Name	Explanation	Initial Value	Value	Operation
7	BREN	enable BRQ pin input and external bus sharing	0	0	No bus sharing by BRQ/BGRNTX. BRQ input is disabled.
				1	Bus sharing by BRQ/BGRNTX. BRQ input is enabled.
6	PSUS	Control temporary stopping of pre-fetch	0	0	Enable pre-fetch

				1	Suspend pre-fetch
5	PCLR	completely clear the pre-fetch buffer	0	0	Normal state
				1	Clear the pre-fetch buffer
4-2	CHE4	Reserved			
1-0	RDW1:0	These bits instruct all chip select areas and fly-by I/O channels to reduce only the number of auto-wait cycles in the auto-access cycle wait settings uniformly while the AWR register settings are retained unchanged	00_B	00	Normal wait (AWR0-7 settings)
				01	1/2 (1-bit shift to the right) of the AWR0-7 settings
				10	1/4 (2-bit shift to the right) of the AWR0-7 settings
				11	1/8 (3-bit shift to the right) of the AWR0-7 settings

2.2.10 Refresh Control Register (RCR)

The refresh control register (RCR) is used to make various refresh control settings for SDRAM.

The setting of this register is meaningless as long as SDRAM control is not set for any area, in that case the register value must not be updated from the initial state.

When read by a Read - modify - Write instruction, the SELF, RRLD, and PON bits always return to 0.

Bit No.	Name	Explanation	Initial Value	Value	Operation
31	SELF	Control the self - refresh mode	0	0	Auto - refresh or power - down
				1	Transition to self-refresh mode
30	RRLD	Start and reload the fresh counter	0	0	Disable (no operation)
				1	Execute auto - refreshing once and reload the RFINT value.
29-24	RFINT5:0	Set interval for automatic refreshing	$XXXXXX_B$		The auto - refresh interval can be obtained for distributed refresh mode {(REFINT5 - REFINT0 value) x 32 x (external bus clock cycle)}
					The auto - refresh interval can be obtained for centralized refresh mode {(REFINT5 - REFINT0 value) x 32 x (RFC specified number of times) x (external bus clock cycle)}
23	BRST	control the operation mode for auto - refreshing	X	0	Distributed refresh (Auto - refresh is activated at intervals.)
				1	Burst refresh (Auto - refresh is activated repeatedly at one time.)
22-20	RFC2:0	Set these bits to the number of times a refresh must be performed to refresh all SDRAM	XXX_B	000	Refresh 256 times
				001	Refresh 512 times
				010	Refresh 1024 times
				011	Refresh 2048 times
				100	Refresh 4096 times
				101	Refresh 8192 times
				110	Setting prohibited
				111	Refresh prohibited
19	PON	control the SDRAM (FCRAM) power - on sequence	X	0	Disabled (no-operation)
				1	Start power-on sequence
18-16	TRC2:0	set the refresh cycle (tRC).	XXX_B	000	4 Refresh Cycle
				001	5 Refresh Cycle
				010	6 Refresh Cycle
				011	7 Refresh Cycle
				100	8 Refresh Cycle

				101	9 Refresh Cycle
				110	10 Refresh Cycle
				111	11 Refresh Cycle

2.2.11 Port Function Register (PFR7-0)

Register Name	Value	Operation
PFR00	11111111_B	Port 00 is in external bus data D[31:24] mode (if external bus is enabled otherwise general purpose port)
	00000000_B	Port 00 is in general purpose port mode
PFR01	11111111_B	Port 01 is in external bus data D[23:16] mode (if external bus is enabled otherwise general purpose port)
	00000000_B	Port 01 is in general purpose port mode
PFR02	11111111_B	Port 02 is in external bus data D[15:8] mode (if external bus is enabled otherwise general purpose port)
	00000000_B	Port 02 is in general purpose port mode
PFR03	11111111_B	Port 03 is in external bus data D[7:0] mode (if external bus is enabled otherwise general purpose port)
	00000000_B	Port 03 is in general purpose port mode
PFR04	11111111_B	Port 04 is in external bus address A[31:24] mode (if external bus is enabled otherwise general purpose port)
	00000000_B	Port 04 is in general purpose port mode
PFR05	11111111_B	Port 05 is in external bus data A[23:16] mode (if external bus is enabled otherwise general purpose port)
	00000000_B	Port 05 is in general purpose port mode
PFR06	11111111_B	Port 06 is in external bus data A[15:8] mode (if external bus is enabled otherwise general purpose port)
	00000000_B	Port 06 is in general purpose port mode
PFR07	11111111_B	Port 07 is in external bus data A[7:0] mode (if external bus is enabled otherwise general purpose port)
	00000000_B	Port 07 is in general purpose port mode

2.2.12 Port Function Register (PFR6)

Bit No.	Name	Explanation	Value	Operation
7	PFR08.7	External bus control signal RDY	0	General purpose I/O mode.
			1	External bus RDY enable
6	PFR08.6	External bus control signal BRQ	0	General purpose I/O mode.
			1	External bus BRQ enable
5	PFR08.5	External bus control signal BGRNTX	0	General purpose I/O mode.
			1	External bus BGRNTX enable
4	PFR08.4	External bus control signal RDX	0	General purpose I/O mode.
			1	External bus RDX enable

3	PFR08.3	External bus control signal WRX3	0	General purpose I/O mode.
			1	External bus WRX3enable
2	PFR08.2	External bus control signal WRX2	0	General purpose I/O mode.
			1	External bus WRX2enable
1	PFR08.1	External bus control signal WRX1	0	General purpose I/O mode.
			1	External bus WRX1enable
0	PFR08.0	External bus control signal WRX0	0	General purpose I/O mode.
			1	External bus WRX0 enable

2.2.13 Port Function Register (PFR9)

Register Name	Value	Operation
PFR09	11111111B	Port 09 is in external bus data CSX [7:0] mode (if external bus is enabled otherwise general purpose port)
	00000000B	Port 09 is in general purpose port mode

2.2.14 Port Function Register (PFR10)

Bit No.	Name	Explanation	Value	Operation
7	PFR10.7			
6	PFR10.6	External bus control signal MCLKE	0	General purpose I/O mode.
			1	External bus MCLKE enable
5	PFR10.5	External bus control signal MCLKI/ MCLKIX	0	General purpose I/O mode.
			1	External bus MCLKI if EPFR10.5 is 0B External bus MCLKIX if EPFR10.5 is 1B
7	PFR10.4	External bus control signal MCLKO/ MCLKOX	0	General purpose I/O mode.
			1	External bus MCLKO if EPFR10.4 is 0B External bus MCLKOX if EPFR10.4 is 1B
6	PFR10.3	External bus control signal WEX	0	General purpose I/O mode.
			1	External bus WEX enable
5	PFR10.2	External bus control signal BAAX	0	General purpose I/O mode.
			1	External bus BAAX enable
7	PFR10.1	External bus control signal ASX	0	General purpose I/O mode.
			1	External bus ASX enable
7	PFR10.0	External bus control signal SYSCLK/ SYSCLKX	0	General purpose I/O mode.
			1	External bus SYSCLK if EPFR10.4 is 0B External bus SYSCLKX if EPFR10.4 is 1B

3 Initialization in Start.asm

Initialization of the external bus inerface in start.asm

3.1 Start.asm

In the start up file *Start.asm*, which is included in our template project, the External Bus Interface can be initialized before branching to the application. Therefore the application itself does not need to set up the External Bus Interface, but use it from the beginning on.

The user can adjust the setting in the lines with a "<<<" in the comments on the right side.

3.1.1 Enabling the External Bus Interface

```
;===============================================================================
; 4.8 External Bus Interface
;      The rest of the configuration is only applicable for devices with an external bus
;      interface.
;      If the device does not offer an external bus interface, the configuration can be
;      stopped at this point.
;===============================================================================
;
#set    EXTBUS          ON                  ; <<< Ext. Bus on/off
;
;                       ON      - The ext. bus interface is enabled and is configured as
;                                 set below.
;                       OFF     - The ext. bus interface is disabled.  The port function
;                                 Registers are set to general I/O.  The registers of
;                                 ext. bus interface will not be touched by the start-up
;                                 file.
;                                 Be aware, that the device might be configured in ext.
;                                 bus mode by default after reset.
;                       DEFAULT - Neither the register nor the respective port function
;                                 Registers are touched by the start-up file.
;                                 Be aware, that the device might be configured in ext.
;                                 Bus mode by default after reset.
;
; Note: This feature is not supported by every device. Please check the data sheet.
TheFollowing devices for example do not offer an external bus interface:  MB91464A,
;       MB91467C, MB91465K, MB91463N, MB91465X.
;
;===============================================================================
```

3.1.2 Enabling Chip Select

```
; 4.8.1 Select Chip select (Only EXTBUS == ON)
;================================================================================
=====
;
#set    CS0             OFF                     ; <<< select CS (ON/OFF)
#set    CS1             ON                      ; <<< select CS (ON/OFF)
#set    CS2             OFF                     ; <<< select CS (ON/OFF)
#set    CS3             OFF                     ; <<< select CS (ON/OFF)
#set    CS4             OFF                     ; <<< select CS (ON/OFF)
#set    CS5             OFF                     ; <<< select CS (ON/OFF)
#set    CS6             OFF                     ; <<< select CS (ON/OFF)
#set    CS7             ON                      ; <<< select CS (ON/OFF)
#set    SDRAM           ON                      ; <<< select if a SDRAM is connected
;
#set    ENACSX          B'01000010              ; <<< set CS, ENACSX
;                         ||||||||
;                         ||||||||__ CS0 bit, enable/disable CS0 (1/0)
;                         |||||||___ CS1 bit, enable/disable CS1 (1/0)
;                         ||||||____ CS2 bit, enable/disable CS2 (1/0)
;                         |||||_____ CS3 bit, enable/disable CS3 (1/0)
;                         ||||______ CS4 bit, enable/disable CS4 (1/0)
;                         |||_______ CS5 bit, enable/disable CS5 (1/0)
;                         ||________ CS6 bit, enable/disable CS6 (1/0)
;                         |_________ CS7 bit, enable/disable CS7 (1/0)
;
; Note: If the SWB Monitor Debugger is used, set the CS1 (external RAM only) or CS0
and
;       CS 1 (external RAM and flash) to off.
; Note: Not all Chip selects are supported by the different devices.  Please check
the
;       data sheet.
```

3.1.3 Set Memory Addressing

```
;================================================================================
===
; 4.8.2 Set memory addressing for Chip selects (only EXTBUS == ON)
;================================================================================
===
#set    AREASEL0        0x0000                  ; <<< set start add. for CS0, ASR0
#set    AREASEL1        0x2000                  ; <<< set start add. for CS1, ASR1
#set    AREASEL2        0x0000                  ; <<< set start add. for CS2, ASR2
#set    AREASEL3        0x0000                  ; <<< set start add. for CS3, ASR3
#set    AREASEL4        0x0000                  ; <<< set start add. for CS4, ASR4
#set    AREASEL5        0x0000                  ; <<< set start add. for CS5, ASR5
#set    AREASEL6        0x3000                  ; <<< set start add. for CS6, ASR6
#set    AREASEL7        0x0000                  ; <<< set start add. for CS7, ASR7

; Configure the starting address of each used Chip select. Chip selects which are not
used
; (not set to ON in "Select Chip select") need not be set (setting ignored).
;
; NOTE: Just the upper 16-bit of the start address must be set, e.g. when using start
; address 0x00080000 set 0x0008.
```

3.1.4 Configure Chip Select Area

```
;=============================================================================================
===
; 4.8.3 Configure Chip select Area (only EXTBUS == ON)
;=============================================================================================
===
#set   CONFIGCS0     B'0000000000000000      ; <<< Config. CS0, ACR0
#set   CONFIGCS1     B'0110100000100010      ; <<< Config. CS1, ACR1
#set   CONFIGCS2     B'0000000000000000      ; <<< Config. CS2, ACR2
#set   CONFIGCS3     B'0000000000000000      ; <<< Config. CS3, ACR3
#set   CONFIGCS4     B'0000000000000000      ; <<< Config. CS4, ACR4
#set   CONFIGCS5     B'0000000000000000      ; <<< Config. CS5, ACR5
#set   CONFIGCS6     B'0111100001101000      ; <<< Config. CS6, ACR6
#set   CONFIGCS7     B'0000000000000000      ; <<< Config. CS7, ACR7
;                       |||||||||||||||
;                       |||||||||||||||__ TYP0 bit, TYP0-4 bits select access type
;                       ||||||||||||||___ TYP1 bit
;                       |||||||||||||____ TYP2 bit
;                       ||||||||||||_____ TYP3 bit
;                       |||||||||||______ LEND bit, select little '1' or big endian '0'
;                       ||||||||||_______ WREN bit, en-/disable (1/0) Write access
;                       |||||||||________ PFEN bit, en-/disable (1/0) pre-fetch
;                       ||||||||_________ SREN bit, en-/disable (1/0)
;                       |||||||__________ BST0 bit, BSTx bits select burst size
;                       ||||||___________ BST1 bit
;                       |||||____________ DBW0 bit, DBWx select data bus width
;                       ||||_____________ DBW1 bit
;                       |||______________ ASZ0 bit, ASZx bits select address size of CS
;                       ||_______________ ASZ1 bit
;                       |________________ ASZ2 bit
;                       _________________ ASZ3 bit
```

3.1.5 Set Wait Cycles

```
; 4.8.4 Set Wait cycles for Chip selects for ordinary bus interface (only EXTBUS ON)
;=============================================================================================
; Ordinary bus interface (w/o SDRAM and FRAM) (ACRx_Type = 0xxx)
#set    WAITREG0      B'0000000000000000      ; <<< CS0 Wait states, AWR0
#set    WAITREG1      B'0011001101111000      ; <<< CS1 Wait states, AWR1
#set    WAITREG2      B'0000000000000000      ; <<< CS2 Wait states, AWR2
#set    WAITREG3      B'0000000000000000      ; <<< CS3 Wait states, AWR3
#set    WAITREG4      B'0000000000000000      ; <<< CS4 Wait states, AWR4
#set    WAITREG5      B'0000000000000000      ; <<< CS5 Wait states, AWR5
 ;                       ||||||||||||||||__ W00 bit, RDY/WRY-> CSX hold cycle
 ;                       |||||||||||||||___ W01 bit, CSX->RDX/WRX setup extensioncycle
 ;                       ||||||||||||||____ W02 bit, Address -> CSX Delay selection
 ;                       |||||||||||||_____ W03 bit, WR0X to WR3X/WRX output timing
 ;                       ||||||||||||______ W04 bit, W04/W05 Write recovery cycle
 ;                       |||||||||||_______ W05 bit
 ;                       ||||||||||________ W06 bit, W06/07 Read -> Write idle cycle
 ;                       |||||||||_________ W07 bit          selection
 ;                       ||||||||__________ W08 bit, W08-W11 Intra-page access cycle
 ;                       |||||||___________ W09 bit          select (0-15 cycles)
 ;                       ||||||____________ W10 bit
 ;                       |||||_____________ W11 bit
 ;                       ||||______________ W12 bit, W12-W15 First access wait cycle
 ;                       |||_______________ W13 bit select (0-15 cycles)
 ;                       ||________________ W14 bit
 ;                       |_________________ W15 bit
 ;
 ; SDRAM and FRAM bus interface (ACRx_Type = 100x)
 #set    WAITREG6        B'0001000101011001      ; <<< CS6 Wait states, AWR6
 #set    WAITREG7        B'0000000000000000      ; <<< CS7 Wait states, AWR7
 ;                         ||||||||||||||||__ W00 bit, W0-W1 RAS pre charge cycles
 ;                         |||||||||||||||___ W01 bit
 ;                         ||||||||||||||____ W02 bit, W2-W3 RAS active Time
 ;                         |||||||||||||_____ W03 bit
 ;                         ||||||||||||______ W04 bit, W4-W5 Write recovery cycle
 ;                         |||||||||||_______ W05 bit
 ;                         ||||||||||________ W06 bit, W6-W7 Read->Write idle cycle
 ;                         |||||||||_________ W07 bit
 ;                         ||||||||__________ W08 bit, W8-W10 CAS latency
 ;                         |||||||___________ W09 bit
 ;                         ||||||____________ W10 bit
 ;                         |||||_____________ W11 bit, reserved
 ;                         ||||______________ W12 bit, W12-W16 RAS-CAS delay
 ;                         |||_______________ W13 bit
 ;                         ||________________ W14 bit
 ;                         |_________________ W15 bit, reserved
 ;
 ; The bit meaning depends on the configured bus interface type. The bus interface can
 be configured for different memory types. Depending on the memory type, the wait
 registers
 ; bits have a different meaning.  CS0-5 should be configurable as ordinary bus
 interface
 ; (w/o SDRAM and FRAM) and CS6-7 should be configurable as SDRAM and FRAM.  It is
```

3.1.6 Configure Chip Select For SDRAM

```
;=============================================================================================
 =
; 4.8.5 Configure Chipselects for SDRAM memory only (only EXTBUS == ON and SDRAM)
;=============================================================================================
 =
;
#set    MEMCON       B'00000111             ; <<< set special SDRAM register, MCRA
;                         ||||||||
;                         ||||||||__ ABS0 bit, set max. active banks (ABS1,0)
;                         |||||||___ ABS1 bit
;                         ||||||____ BANK bit, set number of banks connected to CS
;                         |||||_____ WBST bit, Write burst enable/disable
;                         ||||______ PSZ0 bit, Set page size (PSZ2-0)
;                         |||_______ PSZ1 bit
;                         ||________ PSZ2 bit
;                         |_________ reserved, always write 0
;
; When connecting SDRAM/FCRAM TYP3-0=1000 in ACRx register the following register must
; be setup.
```

3.1.7 Set Refresh Control Register

```
;=============================================================================================
; 4.8.6 Refresh Control Register RCR (only EXTBUS == ON and SDRAM)
;=============================================================================================
;
#set    REFRESH     B'1110001001000111      ; <<< set Refresh Control Register, RCR
;                        ||||||||||||||||
;                        ||||||||||||||||__ TRC0 bit, set refresh cycle (TRC2-0)
;                        |||||||||||||||___ TRC1 bit
;                        ||||||||||||||____ TRC2 bit
;                        |||||||||||||_____ PON bit, set power-on control
;                        ||||||||||||_______ RFC0 bit, set refresh count (RFC2-0)
;                        |||||||||||________ RFC1 bit
;                        ||||||||||_________ RFC2 bit
;                        |||||||||__________ BRST bit, set burst refresh control
;                        ||||||||___________ RFINT0 bit, set auto refresh interval
;                        |||||||____________ RFINT1 bit, (RFINT5-0)
;                        ||||||_____________ RFINT2 bit
;                        |||||______________ RFINT3 bit
;                        ||||_______________ RFINT4 bit
;                        |||________________ RFINT5 bit
;                        ||_________________ RRLD bit, counter refresh start control
;                        |__________________ SELF bit, self refresh control
;
;
; This register sets various SDRAM refresh controls.  When SDRAM control is not set
 for
; any area, the setting of this register is meaningless,  but do not change the
 register
; value at  initial   state.   When a read is performed   using a read-modify-write
; instruction, 0 always returns from the SELF, RRLD, and PON bits.
```

3.1.8 Timing Control Register

```
;================================================================================
; 4.8.7 Terminal and Timing Control Register (only EXTBUS == ON)
;================================================================================
;
#set    TIMECONTR        B'00000000             ; <<< set TCR register, TCR
;                          ||||||||
;                          ||||||||__ RDW0 bit, set wait cycle reduction (RDW0,1)
;                          |||||||___ RDW1 bit
;                          ||||||____ OHT0 bit, set output hold delay (OHT1,0)
;                          |||||_____ OHT1 bit
;                          ||||______ reserved, always write 0
;                          |||_______ PCLR bit, pre fetch buffer clear
;                          ||________ PSUS bit, pre fetch suspend
;                          |_________ BREN bit, BRQ input enable
;
; This register controls the general functions of the external bus interface
 controller
; such as the common-pin function setting and timing control.
```

3.1.9 Set Cache

```
;================================================================================
 ===
; 4.8.8 Enable/Disable I-CACHE (only EXTBUS == ON)
;================================================================================
 ===
;
#set    C1024           1                      ; CACHE Size: 1024 BYTE
#set    C2048           2                      ; CACHE Size: 2048 BYTE
#set    C4096           3                      ; CACHE Size: 4096 BYTE
;
#set    CACHE           OFF                    ; <<< Select use of cache
#set    CACHE_SIZE      C4096                  ; <<< Select size of cache, ISIZE
;
;It is possible to use cache functionality on the I-Bus on several devices.  Please
;check the  corresponding data sheet  if this feature is  available on a certain
 device ;and for the size of the cache. This is the general cache configuration. It
 is possible ;to configure for each CS area, if the cache should be used.
;
; Note: This feature is not supported by every device. Please check the data sheet.
 The
;       feature is for example supported by MB91461R, MB91469G.
;================================================================================
 ===
; 4.8.9 Enable CACHE for chip select (only EXTBUS == ON)
;================================================================================
 ===
;
#set    CHEENA          B'11111111             ; <<< en-/disable cache, CHER
;                         ||||||||
;                         ||||||||__ CHE0 bit, CS0 area
;                         |||||||___ CHE1 bit, CS1 area
;                         ||||||____ CHE2 bit, CS2 area
;                         |||||_____ CHE3 bit, CS3 area
;                         ||||______ CHE4 bit, CS4 area
;                         |||_______ CHE5 bit, CS5 area
```

3.1.10 Set External Bus Mode Data Pin

```
;=============================================================================
===
; 4.8.10 Select External bus mode (Data lines) (only EXTBUS == ON)
;=============================================================================
===
;
#set    PFUNC0          B'11111111              ;<<< Data lines or GIO, PFR00
;                         ||||||||
;                         ||||||||__ D24 / P00_0
;                         |||||||___ D25 / P00_1
;                         ||||||____ D26 / P00_2
;                         |||||_____ D27 / P00_3
;                         ||||______ D28 / P00_4
;                         |||_______ D29 / P00_5
;                         ||________ D30 / P00_6
;                         |_________ D31 / P00_7
;
#set    PFUNC1          B'11111111              ;<<< Data lines or GIO, PFR01
;                         ||||||||
;                         ||||||||__ D16 / P01_0
;                         |||||||___ D17 / P01_1
;                         ||||||____ D18 / P01_2
;                         |||||_____ D19 / P01_3
;                         ||||______ D20 / P01_4
;                         |||_______ D21 / P01_5
;                         ||________ D22 / P01_6
;                         |_________ D23 / P01_7
;
#set    PFUNC2          B'11111111              ;<<< Data lines or GIO, PFR02
;                         ||||||||
;                         ||||||||__ D8 / P02_0
;                         |||||||___ D9 / P02_1
;                         ||||||____ D10 / P02_2
;                         |||||_____ D11 / P02_3
;                         ||||______ D12 / P02_4
;                         |||_______ D13 / P02_5
;                         ||________ D14 / P02_6
;                         |_________ D15 / P02_7
;
#set    PFUNC3          B'11111111              ;<<< Data lines or GIO, PFR03
;                         ||||||||
;                         ||||||||__ D0 / P03_0
;                         |||||||___ D1 / P03_1
;                         ||||||____ D2 / P03_2
;                         |||||_____ D3 / P03_3
;                         ||||______ D4 / P03_4
;                         |||_______ D5 / P03_5
;                         ||________ D6 / P03_6
;                         |_________ D7 / P03_7
;
; Select if the ports are set to
;                   1   : External bus mode, I/O for data lines or
;                   0   : General I/O port (GIO)
;
; Note: Not all data-lines are supported by the different devices. Please check the
datasheet.
```

3.1.11 Set External Bus Mode Address Pin

```
;=============================================================================
; 4.8.11 Select External bus mode (Address lines) (only EXTBUS == ON)
;=============================================================================
;
#set    PFUNC4          B'11111111              ;<<< Address lines or GIO, PFR04
;                         ||||||||
;                         ||||||||__ A24 / P04_0
;                         |||||||___ A25 / P04_1
;                         ||||||____ A26 / P04_2
;                         |||||_____ A27 / P04_3
;                         ||||______ A28 / P04_4
;                         |||_______ A29 / P04_5
;                         ||________ A30 / P04_6
;                         |_________ A31 / P04_7
;
#set    PFUNC5          B'11111111              ;<<< Address lines or GIO, PFR05
;                         ||||||||
;                         ||||||||__ A16 / P05_0
;                         |||||||___ A17 / P05_1
;                         ||||||____ A18 / P05_2
;                         |||||_____ A19 / P05_3
;                         ||||______ A20 / P05_4
;                         |||_______ A21 / P05_5
;                         ||________ A22 / P05_6
;                         |_________ A23 / P05_7
;
#set    PFUNC6          B'11111111              ;<<< Address lines or GIO, PFR06
;                         ||||||||
;                         ||||||||__ A8 / P06_0
;                         |||||||___ A9 / P06_1
;                         ||||||____ A10 / P06_2
;                         |||||_____ A11 / P06_3
;                         ||||______ A12 / P06_4
;                         |||_______ A13 / P06_5
;                         ||________ A14 / P06_6
;                         |_________ A15 / P06_7
;
#set    PFUNC7          B'11111111              ;<<< Address lines or GIO, PFR07
;                         ||||||||
;                         ||||||||__ A0 / P07_0
;                         |||||||___ A1 / P07_1
;                         ||||||____ A2 / P07_2
;                         |||||_____ A3 / P07_3
;                         ||||______ A4 / P07_4
;                         |||_______ A5 / P07_5
;                         ||________ A6 / P07_6
;                         |_________ A7 / P07_7
;
; Select if the ports are set to
;                   1   : External bus mode, I/O for address lines or
;                   0   : General I/O port (GIO)
;
; Note: Not all address-lines are supported by the different devices.  Please check
 the data sheet.
```

3.1.12 Set External Bus Mode Control Pin

```
;=============================================================================
; 4.8.12 Select External bus mode (Control signals) (only EXTBUS == ON)
;=============================================================================
;
#set    PFUNC8          B'11111111              ;<<< Control signals or GIO, PFR08
;                         ||||||||
;                         ||||||||__ WRX0 / P08_0
;                         |||||||___ WRX1 / P08_1
;                         ||||||____ WRX2 / P08_2
;                         |||||_____ WRX3 / P08_3
;                         ||||______ RDX / P08_4
;                         |||_______ BGRNTX / P08_5
;                         ||________ BRQ / P08_6
;                         |_________ RDY / P08_7
;
#set    PFUNC9          B'11111111              ;<<< Control signals or GIO, PFR09
;                         ||||||||
;                         ||||||||__ CSX0 / P09_0
;                         |||||||___ CSX1 / P09_1
;                         ||||||____ CSX2 / P09_2
;                         |||||_____ CSX3 / P09_3
;                         ||||______ CSX4 / P09_4
;                         |||_______ CSX5 / P09_5
;                         ||________ CSX6 / P09_6
;                         |_________ CSX7 / P09_7
;
#set    PFUNC10         B'01011111              ;<<< Control signals or GIO, PFR10
;                         ||||||||
;                         ||||||||__ SYSCLK or !SYSCLK / P10_0
;                         |||||||___ ASX / P10_1
;                         ||||||____ BAAX / P10_2
;                         |||||_____ WEX / P10_3
;                         ||||______ MCLKO or !MCLKO / P10_4
;                         |||_______ MCLKI or !MCLKI/ P10_5
;                         ||________ MCLKE / P10_6
;                         |_________ -
;
#set    EPFUNC10        B'00000000              ;<<< Control signals or GIO, EPFR10
;                         ||||||||
;                         ||||||||__ 0:SYSCLK / 1:!SYSCLK
;                         |||||||___ -
;                         ||||||____ -
;                         |||||_____ -
;                         ||||______ 0:MCLKO / 1:!MCLKO
;                         |||_______ 0:MCLKI / 1:!MCLKI
;                         ||________ 0:MCLKI / 1:!MCLKI
;                         |_________ -
;
;
; Select if the ports are set to
;                 1   : External bus mode, I/O for control lines or
;                 0   : General I/O port (GIO)
;
; Note: Not all control-lines are supported by the different devices.  Please check
the data sheet.
;
```

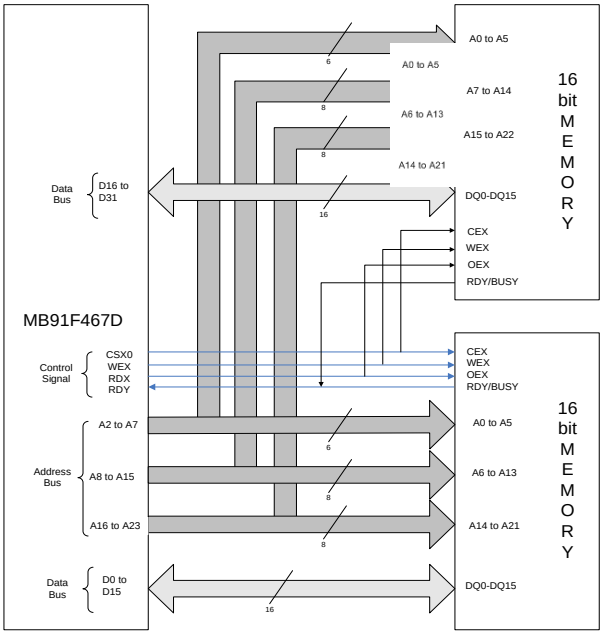
4 External Bus Interface examples

Examples for the external bus interface

4.1 Hardware example for 32-bit Bus Interfacing to memory

Following Diagram shows that two 16-bit memory are connected to MCU MB91F467D to make 32-bit data access. Further A2 of MCU is connected to A0 of external memory device. Also note that WEX strobe is enabled and RDY of MCU is connected to RDY pin of memory hence MCU will wait for RDY signal from memory to go active before completing read or write access.

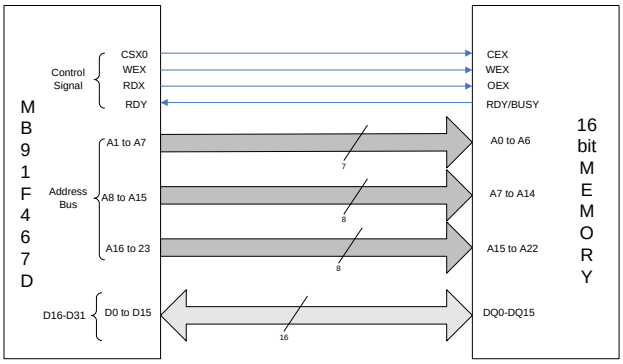
Figure 4-1. 32-bit bus interfacing to memory



4.2 Hardware example for 16-bit Bus Interfacing to memory

Following Diagram shows that 16-bit memory is connected to MCU MB91F467D to make 16-bit data access. Further A1 of MCU is connected to A0 of external memory device. Also note that WEX strobe is enabled and RDY of MCU is connected to RDY pin of memory hence MCU will wait for RDY signal from memory to go active before completing read or write access.

Figure 4-2. 16-bit bus interfacing to memory



5 Timing analysis

Timing consideration for interfacing flash and SRAM

5.1 Flash Read AC characteristics

Figure 5-1 below shows timing diagram of Flash read cycle.

Figure 5-1. Flash read timing diagram

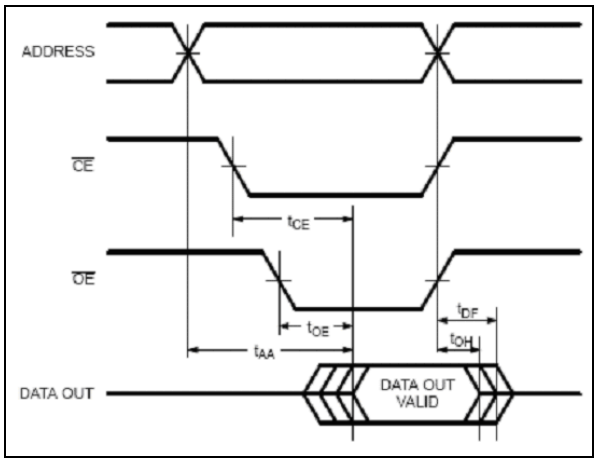


Table 5-1. Flash read characteristics

Parameter	Symbol	Value						Unit
		80		90		12		
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	tRC	80	-	90		120		ns
Address to Output Delay	tAA	-	80	-	90	-	120	ns
Chip Enable to Output Delay	tCE	-	80	-	90	-	120	ns
Output Enable to Output Delay	tOE	-	30	-	35	-	50	ns
Chip Enable to Output High-Z	tDF	-	25	-	30	-	30	ns
Output Enable to Output High-Z	tDF	-	25	-	30	-	30	ns
Output Hold Time From Addresses, CEX or OEX, whichever Occurs First	tOH	0	-	0	-	0	-	ns

Here, t_{AA}, defines the maximum time after the address stabilizes that the Flash will return valid data. This parameter is commonly referred to as the ‘access time’ of the device

Similarly, t_{CE} defines the maximum time after the CEX input is asserted that the Flash will return data. This spec is typically, though not always, the same as t_{AA}. t_{OE} defines the maximum time from OEX assertion to valid data output much like t_{CE}. t_{OH} indicates the minimum time the data is guaranteed to remain valid after CEX/OEX de assertion. t_{DF}, defines the maximum time after which the output is guaranteed to completely float

5.2 RAM Read AC characteristics

Figure 5-2.RAM read timing diagram

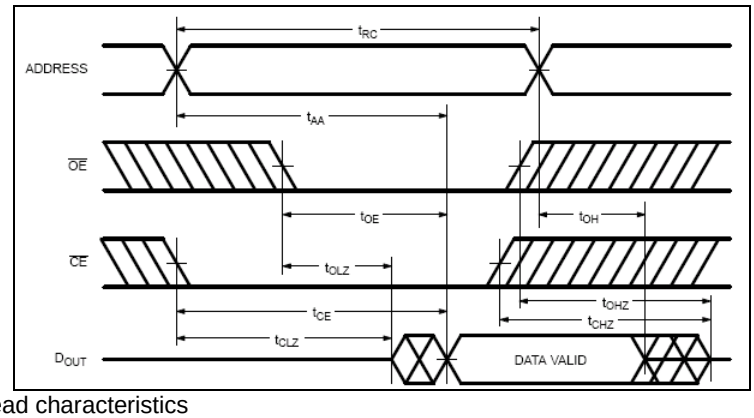


Table 5-2. RAM read characteristics

Parameter	Symbol	Value				Unit
		15		20		
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	15	-	20	-	ns
Address Access Time	t_{ACC}	-	15	-	20	ns
Chip Enable Access Time	t_{CE}	-	15	-	20	ns
Output Enable Access Time	t_{OE}	-	8	-	10	ns
Chip Enable Low to Output Active	t_{CLZ}	3	-	3	-	ns
Output Enable Low to Output Active	t_{OLZ}	1	-	1	-	ns
Chip Enable High to Output High-Z	t_{CHZ}	-	7	-	7	ns
Output Enable High to Output High-Z	t_{OHZ}	-	7	-	7	ns
Output Data Hold Time	t_{OH}	5	-	5	-	ns

Figure 5-2 shows the read cycle timing for a RAM which is quite similar to that of a Flash.

Here separate CEX and OEX data float specs (t_{CHZ}, t_{OHZ}) are defined instead of a single t_{DF}. Since the SRAM (unlike the EPROM/Flash) can be written. It also specifies the other side of the data float (i.e., enable to output driven) with t_{CLZ} and t_{OLZ}.

5.3 RAM Write AC characteristics

Figure 5-3.RAM write timing diagram

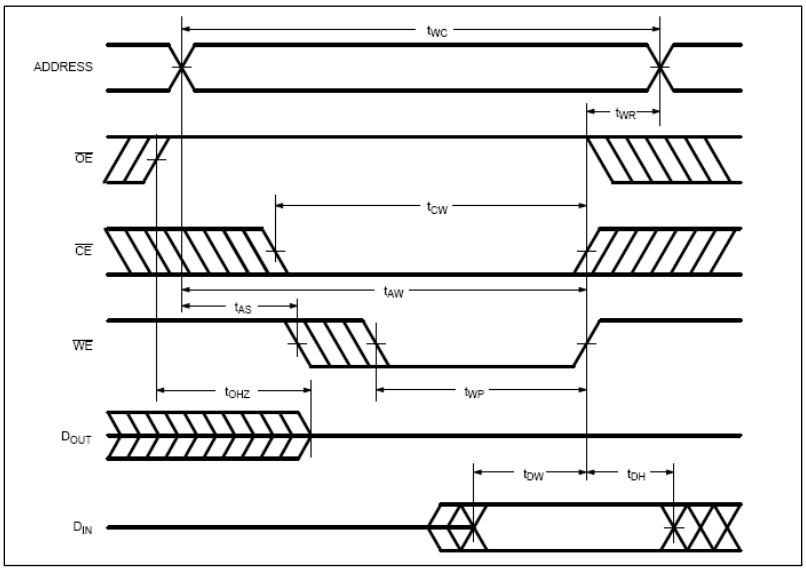


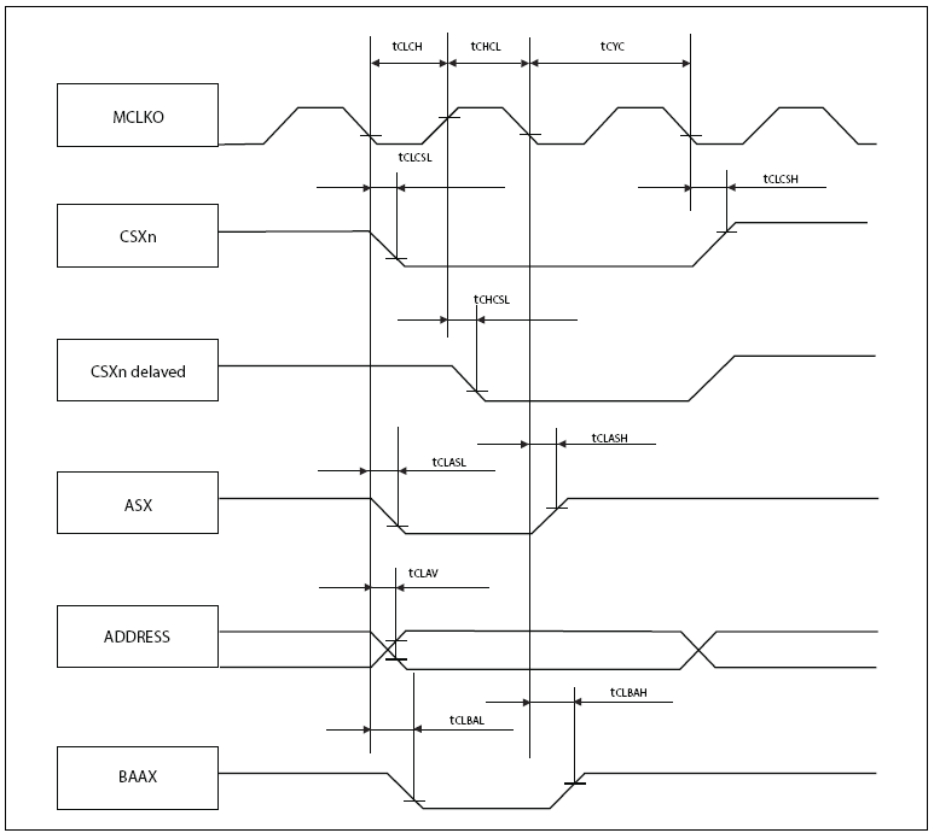
Table 5-3. RAM write Characteristics

Parameter	Symbol	Value				Unit
		15		20		
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	15	-	20	-	ns
Write Pulse Width	t_{WP}	10	-	15	-	ns
Chip Enable to End of Write	t_{CW}	10	-	12	-	ns
Address Setup Time	t_{AS}	0	-	0	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Output Enable High to Output High-Z	t_{OHZ}	-	7	-	7	ns
Data Setup Time	t_{DW}	8	-	10	-	ns
Data Hold Time	t_{DH}	0	-	0	-	ns

Figure 5-3 shows the write cycle timing. Write time (tWP) is defined as the time during which both CEX and WE are asserted. tWC simply defines the write cycle time which, along with tRC, is the same as the ‘access time’. tCW and tAW specify the minimum time from valid CEX and address inputs to the end of the write cycle. tAS defines an address setup to the beginning of the write cycle. tWP simply specifies the minimum write pulse (the overlap of CEX and WE) width. tWR specifies a minimum write ‘recovery’ time, essentially an address hold time after the end of write. tDW and tDH specify the input data setup and hold times relative to the end of write. tOHZ defines time duration that must be elapsed before a new write cycle begin to allow previous read data to disappear and to avoid bus contention.

5.4 MCU External Bus Basic Timings

Figure 5-4. External bus basic timings



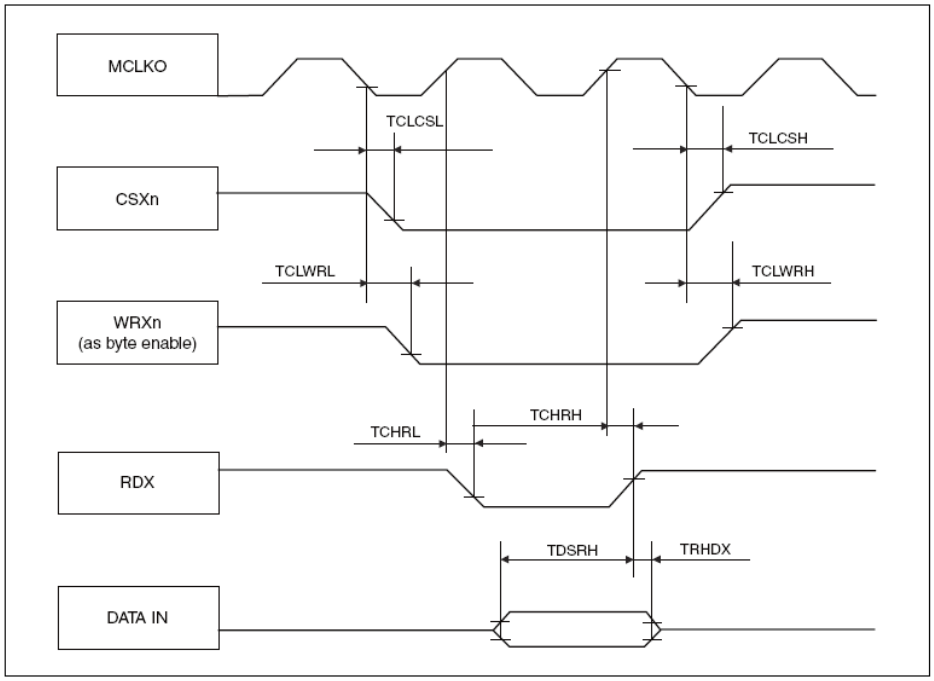
($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = −40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO	t_{CLCH}	MCLKO	1/2 × t_{CYC} − 7	1/2 × t_{CYC} + 7	ns
	t_{CHCL}		1/2 × t_{CYC} − 7	1/2 × t_{CYC} + 7	ns
MCLKO ↓ to CSXn delay time	t_{CLCSL}	MCLKO CSXn	—	9	ns
	t_{CLCSH}		—	8	ns
MCLKO ↑ to CSXn delay time (Addr → CS delay)	t_{CHCSL}		− 5	+ 2	ns
MCLKO ↓ to ASX delay time	t_{CLASL}	MCLKO ASX	—	8	ns
	t_{CLASH}		—	8	ns
MCLKO ↓ to BAAX delay time	t_{CLBAL}	MCLKO BAAX	—	5	ns
	t_{CLBAH}		1	—	ns
MCLKO ↓ to Address valid delay time	t_{CLAV}	MCLKO A25 to A0	—	11	ns

Note : t_{CYC} is the frequency of clock cycle.

5.5 MCU External Bus Synchronous/Asynchronous Read Access

Figure 5-5. External Memory Read Cycle

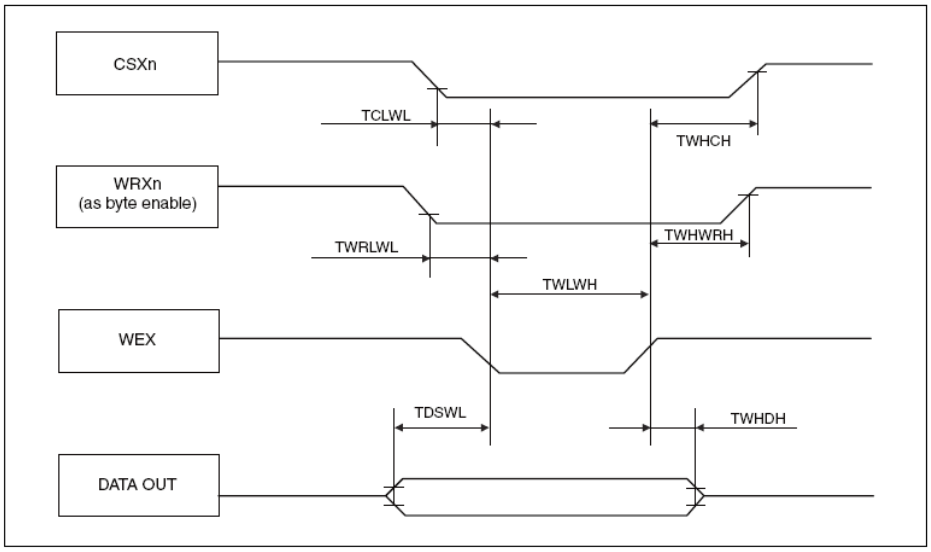


($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = −40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↑ to RDX delay time	TCHRL	MCLKO RDX	− 5	2	ns
	TCHRH		− 5	2	ns
Data valid to RDX ↑ setup time	TDSRH	RDX D31 to D0	20	—	ns
RDX ↑ to Data valid hold time (internal MCLKO → MCLKI MCLKI feedback)	TRHDX	RDX D31 to D0	0	—	ns
MCLKO ↓ to WRXn (as byte enable) delay time	TCLWRL	MCLKO WRXn	—	9	ns
	TCLWRH		− 1	—	ns
MCLKO ↓ to CSXn delay time	TCLCSL	MCLKO CSXn	—	9	ns
	TCLCSH		—	8	ns

5.6 MCU External Bus Asynchronous Write Access - Byte Control Type

Figure 5-6. External Memory Asynchronous Write Cycle

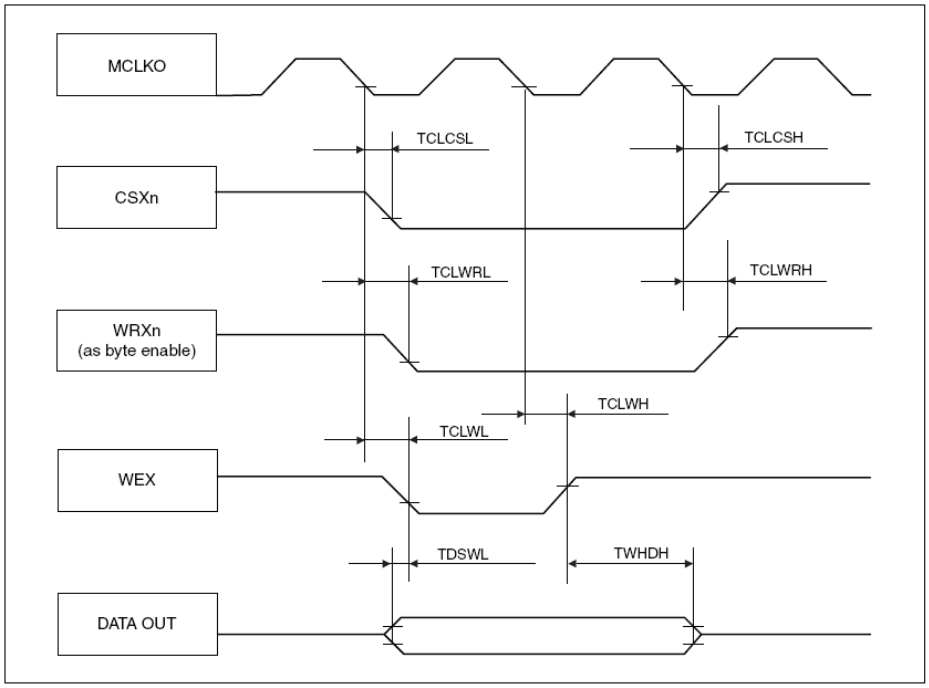


($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = −40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WEX ↓ to WEX ↑ pulse width	TWLWH	WEX	t_{CYC} − 2	—	ns
Data valid to WEX ↓ setup time	TDSWL	WEX D31 to D0	1/2 × t_{CYC} − 13	—	ns
WEX ↑ to Data valid hold time	TWHDH	WEX D31 to D0	1/2 × t_{CYC} − 10	—	ns
WEX to WRXn delay time	TWRLWL	WEX WRXn	—	1/2 × t_{CYC} + 2	ns
	TWHWRH		1/2 × t_{CYC} − 4	—	ns
WEX to CSXn delay time	TCLWL	WEX CSXn	—	1/2 × t_{CYC}	ns
	TWHCH		1/2 × t_{CYC} − 5	—	ns

5.7 MCU External Bus Synchronous Write Access - Byte Control Type

Figure 5-7. External Memory Synchronous Write Cycle



($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = –40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
MCLKO ↓ to WEX delay time	TCLWL	MCLKO WEX	—	9	ns
	TCLWH		2	—	ns
Data valid to WEX ↓ setup time	TDSWL	WEX D31 to D0	– 11	—	ns
WEX ↑ to Data valid hold time	TWHDH	WEX D31 to D0	t_{CYC} – 10	—	ns
MCLKO ↓ to WRXn (as byte enable) delay time	TCLWRL	MCLKO WRXn	—	9	ns
	TCLWRH		– 1	—	ns
MCLKO ↓ to CSXn delay time	TCLCSL	MCLKO CSXn	—	9	ns
	TCLCSH		—	8	ns

5.8 Timing analysis

5.8.1 Constraint for maximum Bus Frequency

In the following the constraints caused by internal technology shows the settings for maximum achievable frequency and performance on the external bus

Check the MB91460 Series Hardware Manual, Datasheets and the MB91F460 series external bus AC spec of the corresponding MB91460 Series MCUs for details on these constraints.

Figure 5-8. CLKT = 50MHz, wait cycles = 0

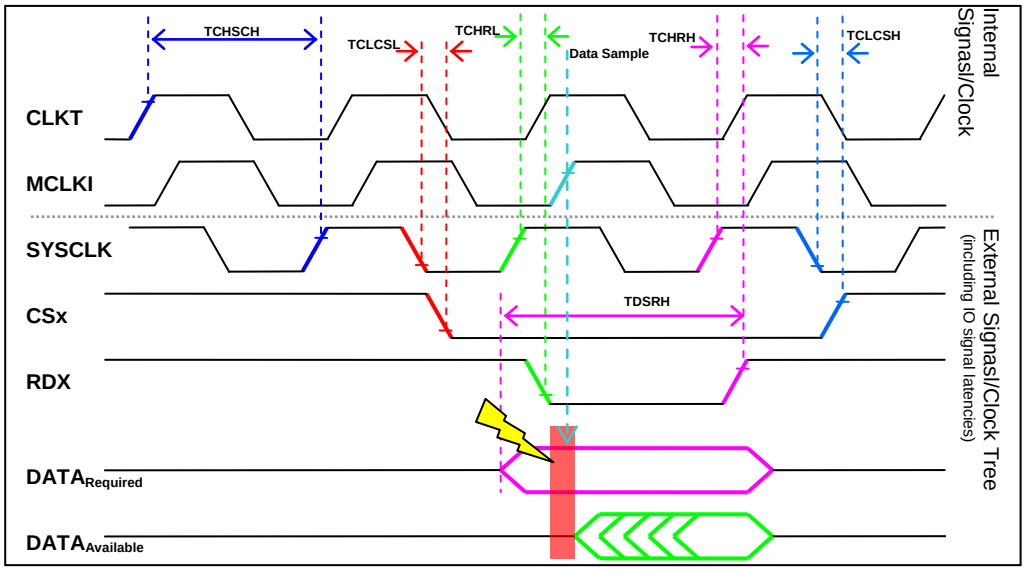


Figure 5.8 shows the non applicable bus timing for an external bus frequency of 50MHz.

The maximum applicable bus frequency (or minimum cyle duration) can be calculated with the following formula:

$$t_{cycle\ -\ min} = \frac{MEM_{DataSetup} - (TCHRH_{Min} - TDSRH_{Min} - }{(1 + Nbr_{Wait\ Cycles})}$$

The following calculations show an exemplary maximum frequency for a different number of wait cycles! Expected Memory data setup time $MEM_{DataSetup}$ = 5ns!

$Nbr_{Wait\ Cycles}$ = 0

$$t_{cycle\ -\ min\ (0WS)} = \frac{MEM_{DataSetup} - (TCHRH_{Min} - TDSRH_{Min} - }{(1 + Nbr_{Wait\ Cycles})}$$

$$\frac{5ns - (-5ns - 20ns - 2ns)}{1}$$

$t_{cycle\ -\ min\ (0WS)}$ 32ns

$CLKT_{max\ (0WS)}$ 31.25MHz

The following calculations show an exemplary maximum frequency for a different number of wait cycles! Expected Memory data setup time $MEM_{DataSetup}$ = 5ns!

$Nbr_{Wait\ Cycles}$ = 1

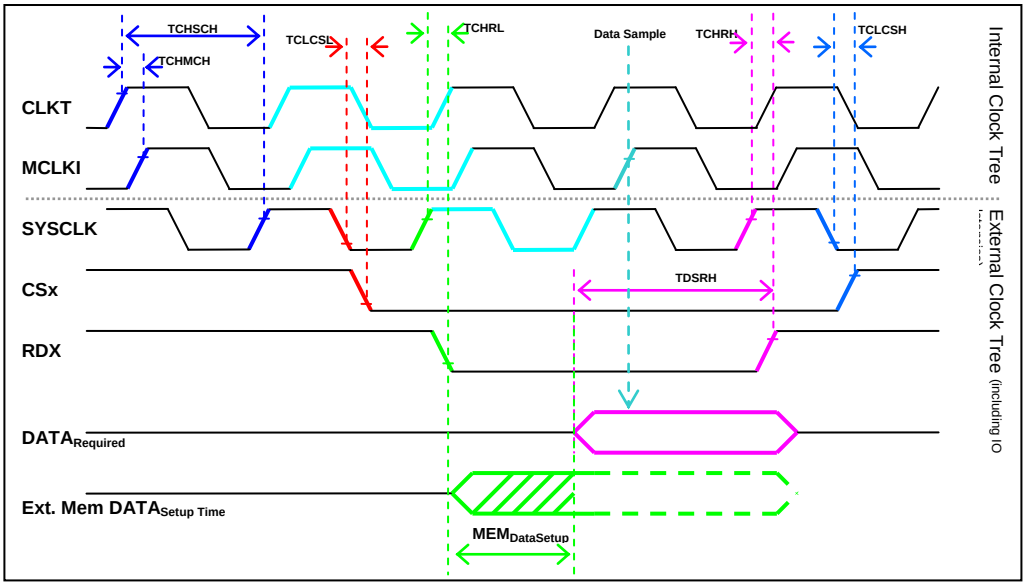
$$t_{cycle\ -\ min\ (1WS)} = \frac{MEM_{DataSetup} - (TCHRH_{Min} - TDSRH_{Min} - }{(1 + Nbr_{Wait\ Cycles})}$$

$$\frac{5ns - (-5ns - 20ns - 2ns)}{2}$$

$t_{cycle\ -\ min\ (1WS)}$ = 16ns

$CLKT_{max\ (1WS)}$ = 62.5MHz

Figure 5-9. CLKT = 50MHz, wait cycles = 1



The figure 5.9 above shows the maximum available data setup time for an external connected memory!

$Nbr_{Wait\ Cycles}$ = 1

$MEM_{DataSetup(MAX)}$ = CLKT + ($Nbr_{Wait\ Cycles}$ * CLKT) + $TCHRH_{Min}$ – $TDSRH_{Min}$ – $TCHRL_{Max}$

= 20ns + 20ns + -5ns – 20ns – 2ns

$MEM_{DataSetup(MAX)}$ = 13ns

5.8.2 Flash Timing Analysis

The procedure is simply to step through each Flash spec one by one to identify a speed grade that meets all the relevant MCU timing requirements.

Lets us for the calculation assume that External bus frequency is 32Mhz i.e. t_{CYC} is equal to 31.25ns and there number of wait cycles are three.

Starting with t_{AA}, this parameter represents the time required for the memory device to decode the address and place the data on the data bus, it is apparent that address access time for the Flash must be less than the MCU t_{ADVDV} (address to valid data in).

t_{AA} (Flash) < t_{ADVDV} (MCU)
t_{AA} (Flash) < (($Nbr_{Wait\ Cycles}$* t_{CYC}) + t_{CYC} + $t_{CLCHmin}$ + $t_{CHRHmin}$ –$t_{DSRHmin}$) - $t_{CLAVmax}$
t_{AA}(Flash) < ((3*31.25ns) +31.25ns + (½(t_{CYC}) -7) +(-5ns) – (20ns)) – 11ns
t_{AA}(Flash) < (93.75ns + 31.25ns + 8.625ns -5ns – 20ns) – 11ns = 97.625ns

Which can be met by either 80ns or 90ns Flash.

$t_{OE,}$ this parameter represents the time required for the chip to activate its outputs from a disabled state, should be less than t_{RLDV} (RDX low to valid data in)

t_{OE}(Flash) < t_{RLDV} (MCU)
t_{OE}(Flash) < (($Nbr_{Wait\ Cycles}$* t_{CYC})+ t_{CYC} + $t_{CHRHmin}$ –$t_{DSRHmin}$) - $t_{CHRLmax}$
t_{OE} (Flash) < ((3*31.25ns)+ 31.25ns + (-5ns) – 20ns) – 2ns
t_{OE} (Flash) < (93.75ns + 31.25ns - 5ns– 20ns) – 2ns = 98ns

Which can be met by either 80ns or 90ns Flash.

t_{OH}, this parameter represents the amount of time that the memory device will continue to drive the bus after the output enable signal has been de-asserted The Flash t_{OH} spec is 0ns. On the MCU side, the corresponding spec is t_{RHDX} (RDX high to Data hold time) which is also 0ns. This spec is also met as per the requirement because MCU will see RDX going high before the Flash and also in fact Flash will take some time to clear its output.

5.8.3 RAM Timing Analysis

The process of evaluating SRAM interface is similar to that for the Flash

Lets us for the calculation assume that External bus frequency is 32Mhz i.e. t_{CYC} is equal to 31.25ns and there number of wait cycles are one.

For a data read, the SRAM t_{AA} is compared with the MCU t_{ADVDV} (address to valid data in).

t_{AA} (RAM) < t_{ADVDV} (MCU)
t_{AA} (RAM) < (($Nbr_{Wait\ Cycles}$* t_{CYC}) + t_{CYC} + $t_{CLCHmin}$ + $t_{CHRHmin}$ –$t_{DSRHmin}$) - $t_{CLAVmax}$
t_{AA}(RAM) < ((1*31.25ns) + 31.25ns + (½(t_{CYC}) -7) +(-5ns) – (20ns)) – 11ns
t_{AA}(RAM) < (31.25ns + 31.25ns + 8.625ns -5ns – 20ns) – 11ns = 35.125ns

Which is met by either 15ns or 20ns SRAM

$t_{OE,}$ should be less than t_{RLDV} (RDX low to valid data in)

t_{OE}(RAM) < t_{RLDV} (MCU)
t_{OE}(RAM) < (($Nbr_{Wait\ Cycles}$* t_{CYC}) + t_{CYC} + $t_{CHRHmin}$ –$t_{DSRHmin}$) - $t_{CHRLmax}$
t_{OE} (RAM) < ((1*31.25ns) + 31.25ns + (-5ns) – 20ns) – 2ns
t_{OE} (RAM) < (62.5ns – 5ns – 20ns) – 2ns = 35.5ns

Which is met by either 15ns or 20ns SRAM

$t_{OHZ,}$ should be less than t_{RHDX} (RDX high to data hold time)

$$t_{OHZ}(RAM) < t_{RHDX}$$
$$t_{OHZ}(RAM) < 0$$

Unfortunately, either SRAM can not meet this spec. We need to use faster RAM. However we can use 15ns or 20ns SRAM ignoring this problem because this situation will arise quite rarely. In real life application this problem will be taken care by the processing time required by application in between two transfers.

$t_{WP,}$ This parameter represents the amount of time that the active-low RD and active-low WR strobes are asserted.

$$t_{WP}(RAM) < t_{WLWH}(MCU)$$
$$t_{WP}(RAM) < t_{CYC} - 2$$
$$t_{WP}(RAM) < 29.25ns$$

Which is met by either 15ns or 20ns SRAM

$t_{DH,}$ This parameter represents the amount of time that the memory device will continue to drive the bus after the output enable signal has been de-asserted.

$$t_{DH}(RAM) < t_{WHDH}(MCU)$$
$$t_{DH}(RAM) < ½\ t_{CYC} – 10$$
$$t_{DH}(RAM) < 5.625ns$$

Which is met by either 15ns or 20ns SRAM

6 Appendix

Miscellaneous information

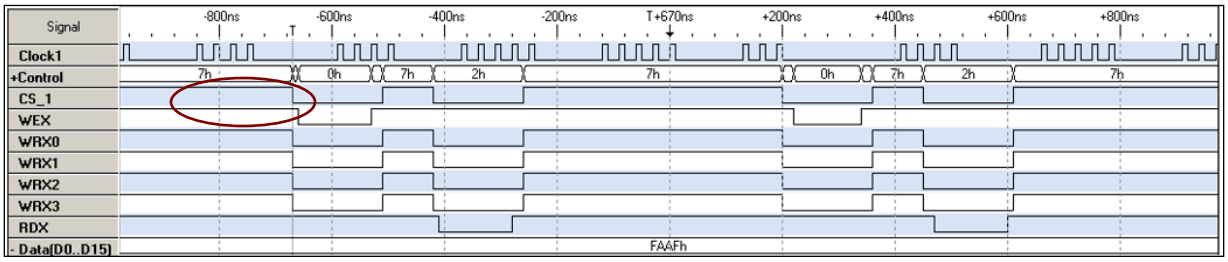
Following sections 6.1 to 6.3 depicts timing diagram of external bus interface showing the behaviour of WRX and WRnX control signal for different settings of bits `TYP3:0[ACRn]`.

Further note that when `TYP3:0[ACRn]` is set as `B'0X0X` WEX output is not strobe and hence WRX pin of external memory device should be connected to available WRnX pin of MCU.

6.1 32-bit Write- and Read Access to External Asynchronous SRAM

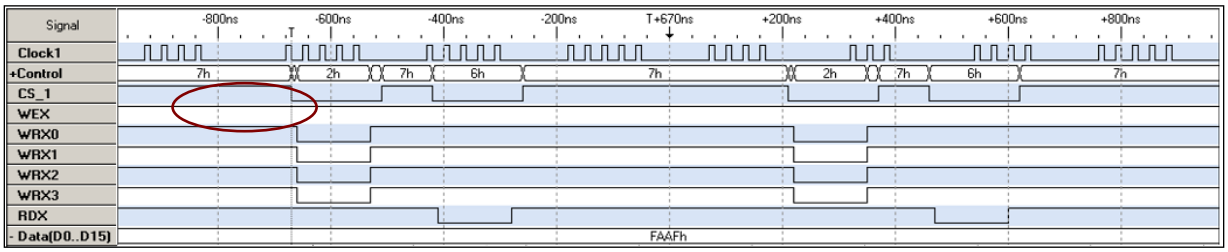
- Setting: The WEX pin is used as write strobe; WRnX can be used for byte-selection

  Setting: ACR1 = B' 0110100000100010



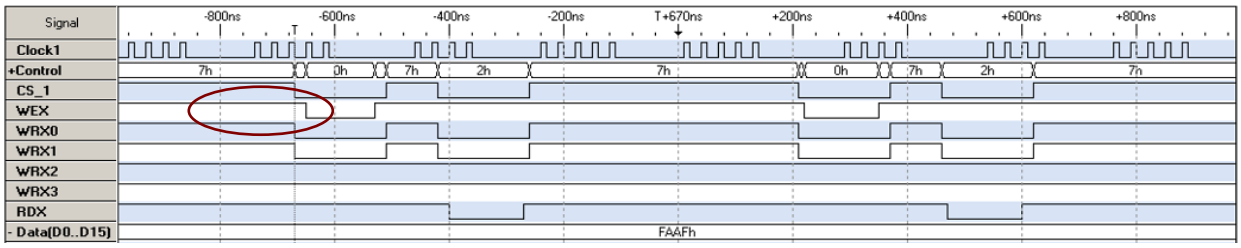
- Setting: The WR0X pin to WR3X pin is used as write strobe

  Setting: ACR1 = B'0110100000100000

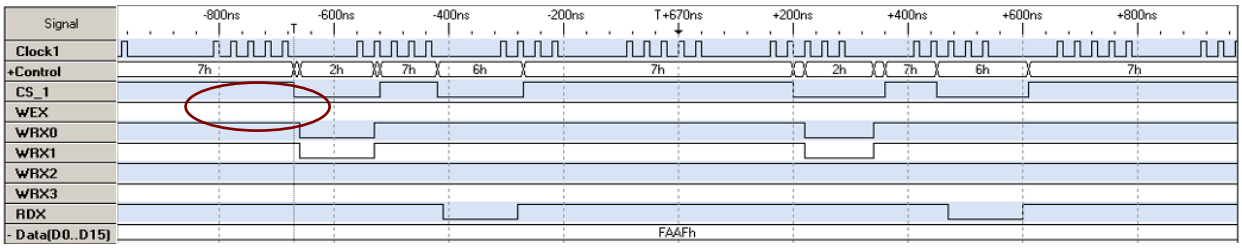


6.2 16-bit Write- and Read Access is tested on External Asynchronous SRAM

- Setting: The WEX pin is used as write strobe; WRnX can be used for byte-selection
  Setting: ACR1 = B’ 0110010000100010

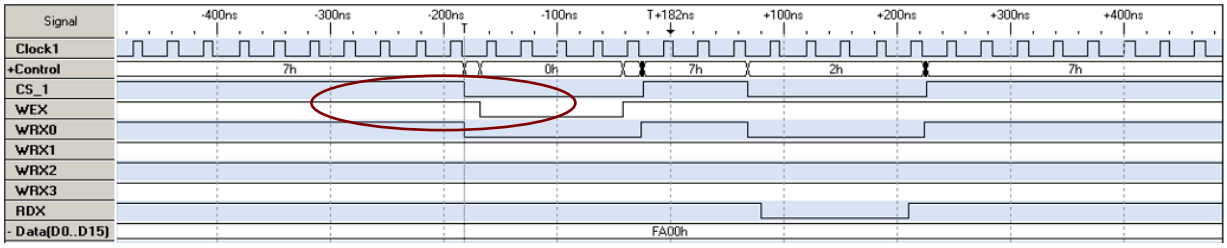


- Setting: The WR0X pin to WR3X pin is used as write strobe
  Setting: ACR1 = B’ 0110010000100000

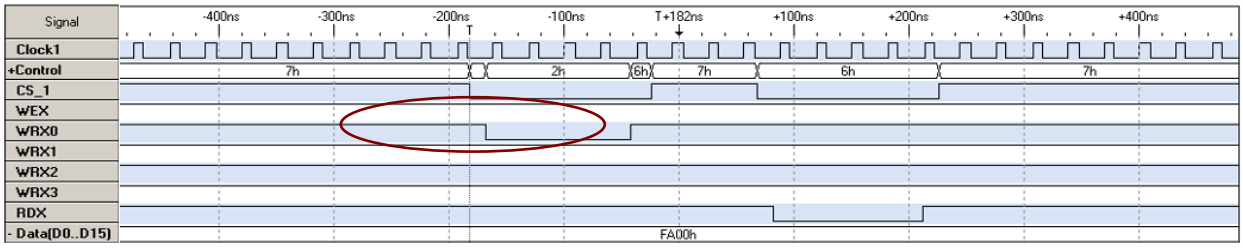


6.3 8-bit Write- and Read Access is tested on External Asynchronous SRAM

- Setting: The WEX pin is used as write strobe
  Setting: ACR1 = B’ 0110000000100010



- Setting: The WR0X pin to WR3X pin is used as write strobe
  Setting: ACR1 = B’ 0110000000100000



7 Additional information

Information about CYPRESS Microcontrollers can be found on the following Internet page:

http://www.cypress.com/cypress-microcontrollers

Document History

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**	-	NOFL	01/15/2008	V1.0 First Version; HPi
*A	5083955	NOFL	01/14/2016	Converted Spansion Application Note “MCU-AN-300051-E-V10” to Cypress format
*B	5843432	AESATP12	08/03/2017	Updated logo and copyright.

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