



The following document contains information on Cypress products. The document has the series name, product name, and ordering part numbering with the prefix “MB”. However, Cypress will offer these products to new and existing customers with the series name, product name, and ordering part number with the prefix “CY”.

How to Check the Ordering Part Number

1. Go to www.cypress.com/pcn.
2. Enter the keyword (for example, ordering part number) in the **SEARCH PCNS** field and click **Apply**.
3. Click the corresponding title from the search results.
4. Download the Affected Parts List file, which has details of all changes

For More Information

Please contact your local sales office for additional information about Cypress products and solutions.

About Cypress

Cypress is the leader in advanced embedded system solutions for the world's most innovative automotive, industrial, smart home appliances, consumer electronics and medical products. Cypress' microcontrollers, analog ICs, wireless and USB-based connectivity solutions and reliable, high-performance memories help engineers design differentiated products and get them to market first. Cypress is committed to providing customers with the best support and development resources on the planet enabling them to disrupt markets by creating new product categories in record time. To learn more, go to www.cypress.com.

SPI on SK-91F467-FlexRay

This application note describes the necessary hardware modification at SK-91F467-FLEXRAY V1.1 to enable the SPI(Serial Peripheral Interface) communication mode between MB91F467D and MB88121B (FlexRay Communication Controller).

Contents

1	Introduction.....	1	3.2	Switch S1 and Jumper JP10, JP11, JP12	7
2	General description	1	3.3	Jumper JP3, JP4, JP5	10
2.1	Pin assignment of CC in SPI mode.....	1	3.4	Jumper JP1, JP2, JP14, JP17, JP20.....	10
2.2	Modification Summary	4	3.5	CC Pin 60 (INT4)	11
3	Detailed description	6	4	Document History.....	14
3.1	Switch S2.....	6			

1 Introduction

This application note describes the necessary hardware modification at SK-91F467-FLEXRAY V1.1 to enable the SPI(Serial Peripheral Interface) communication mode between MB91F467D and MB88121B (FlexRay Communication Controller). The modification on PCB of the SK-91F467-FLEXRAY starter kit is necessary to free one data line (D19) of the external bus interface. Otherwise the external SRAM on the starter kit cannot be used.

2 General description

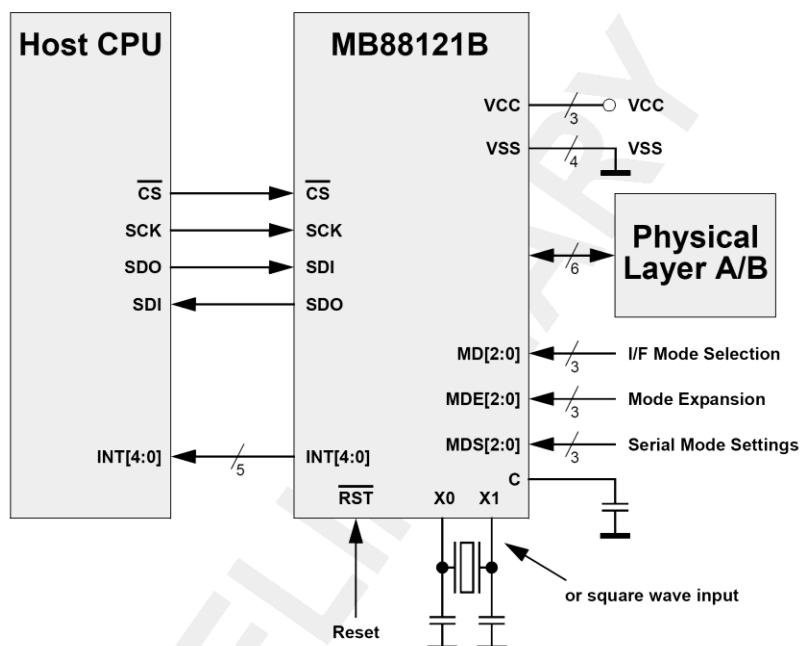
This chapter gives an overview of the modification.

2.1 Pin assignment of CC in SPI mode

The evaluation board SK-91F467-FLEXRAY provides three communication modes between MCU and CC (communication controller). They are 16bit multiplexed parallel mode, 16bit non-multiplexed parallel mode and SPI serial mode.

The communication controller MB88121B has different pin assignment for each mode. For SPI mode the communication block diagram is shown below.

Figure 1. SPI communication mode



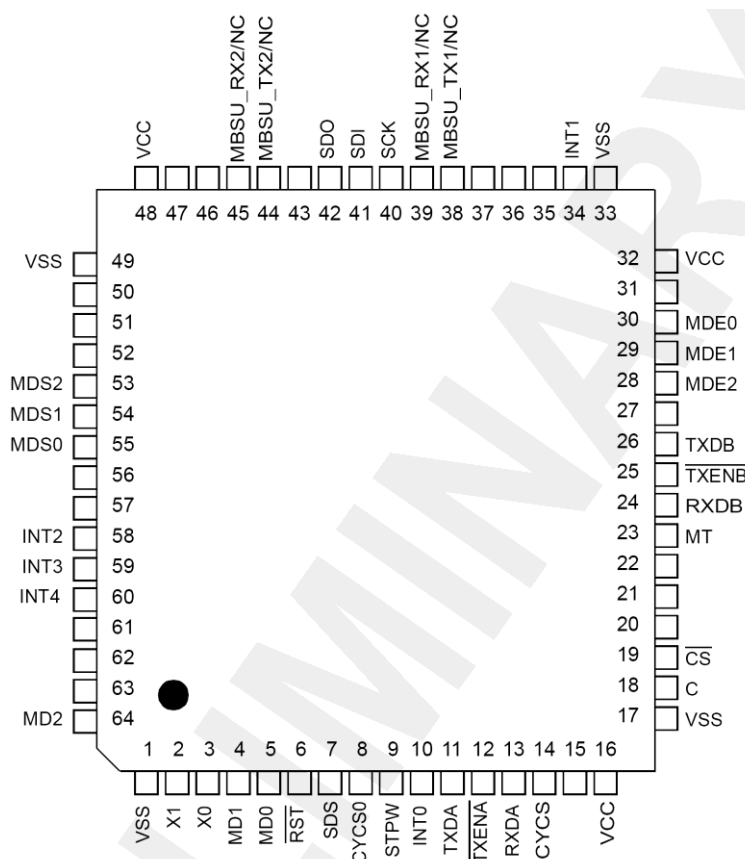
The pin usage of the communication controller is summarized in the following table.

Table 1. CC pin usage in SPI mode

Pin No	Pin name	Description
1,17,33,49	VSS	Ground (0 V)
16,32,48	VCC	Power supply
2,3	X1,X0	Oscillation input/output pin
4,5	MD1,MD0	Mode selection
6	\overline{RST}	Reset input
7	SDS	Start of dynamic segment (debug pin)
8	CYCS0	Cycle 0 start output (debug pin)
9	STPWT	Stop watch trigger input
10	INT0	Interrupt 0 output
11	TXDA	Data output of channel A
12	\overline{TXENA}	Enable output of channel A
13	RXDA	Data input of channel A
14	CYCS	Cycle start output (debug pin)
18	C	Power supply stabilization capacitor pin
19	\overline{CS}	Chip select input
23	MT	Macrotick start output (debug pin)
24	RXDB	Data input of channel B

Pin No	Pin name	Description
25	\overline{TXENB}	Enable output of channel B
26	TXDB	Data output of channel B
28,29,30	MDE2,MDE1,MDE0	Extended mode selection
34	INT1	Interrupt 1 output
38	MBSU_TX1	Debug pin
39	MBSU_RX1	Debug pin
40	SCK	Serial clock input
41	SDI	Serial data input
42	SDO	Serial data output
44	MBSU_TX2	Debug pin
45	MBSU_RX2	Debug pin
53,54,55	MDS2,MDS1,MDS0	Specific settings for SPI mode
58,59,60	INT2,INT3,INT4	Interrupt 2,3,4 output
64	MD2	Mode selection

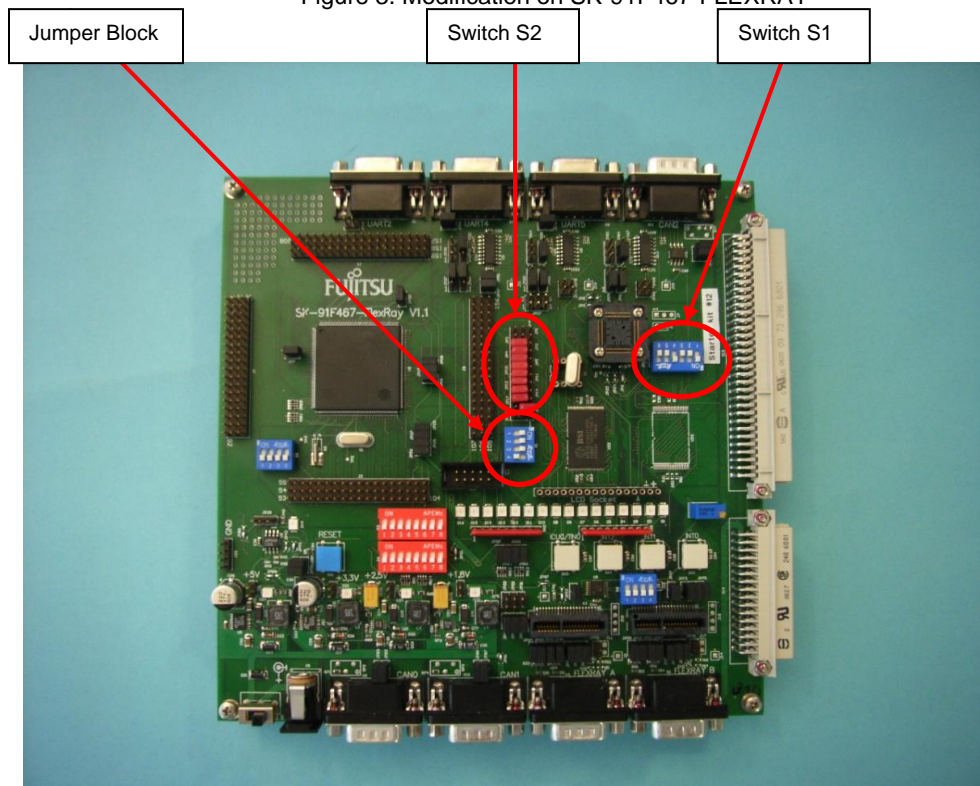
Figure 2. CC pin overview in SPI mode



2.2 Modification Summary

By default the evaluation board SK-91F467-FLEXRAY V1.1 is configured to realize 16bit non-multiplexed communication mode. To use the SPI mode **jumper block**, **switch S2** and **S1** need to be modified.

Figure 3. Modification on SK-91F467-FLEXRAY



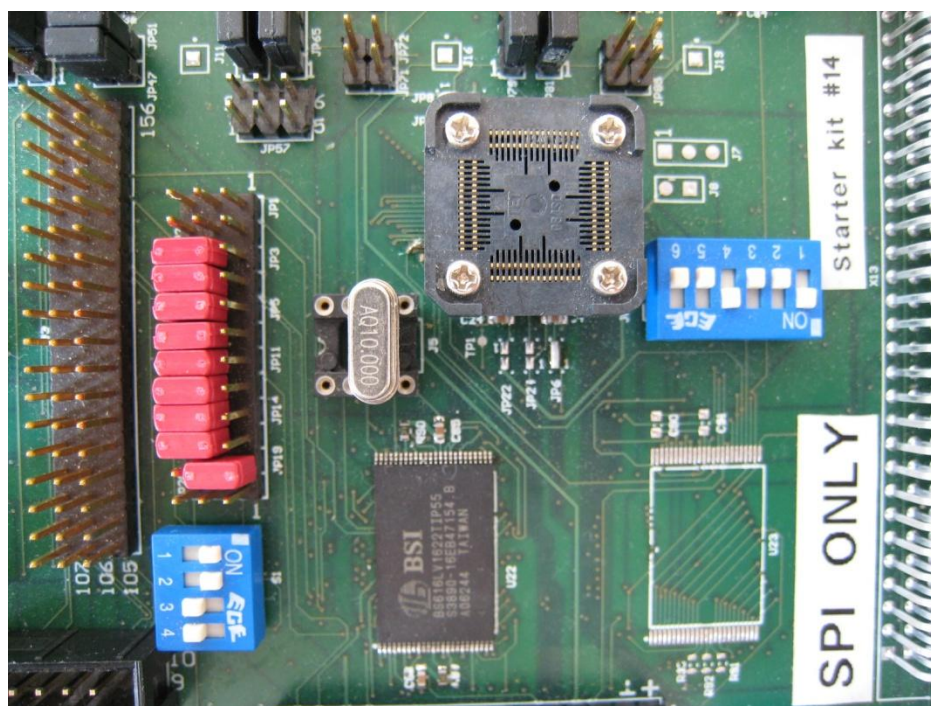
The necessary modification is summarized in the following table. For details please see the next chapter.

Table 2. Modification Summary

Jumper	Setting
JP1	OPEN
JP2	OPEN
JP3	2-3
JP4	2-3
JP5	2-3
JP10	2-3
JP11	2-3
JP12	2-3
JP14	2-3
JP17	2-3
JP19	1-2
JP20	OPEN

Switch	Setting
S2-1	ON
S2-2	OFF
S2-3	OFF
S2-4	ON
S2-5	OFF
S2-6	OFF
S1	Application-specific settings
CC Pin No	setting
60	Manually remove its connection to SRAM

Figure 4. Modification details



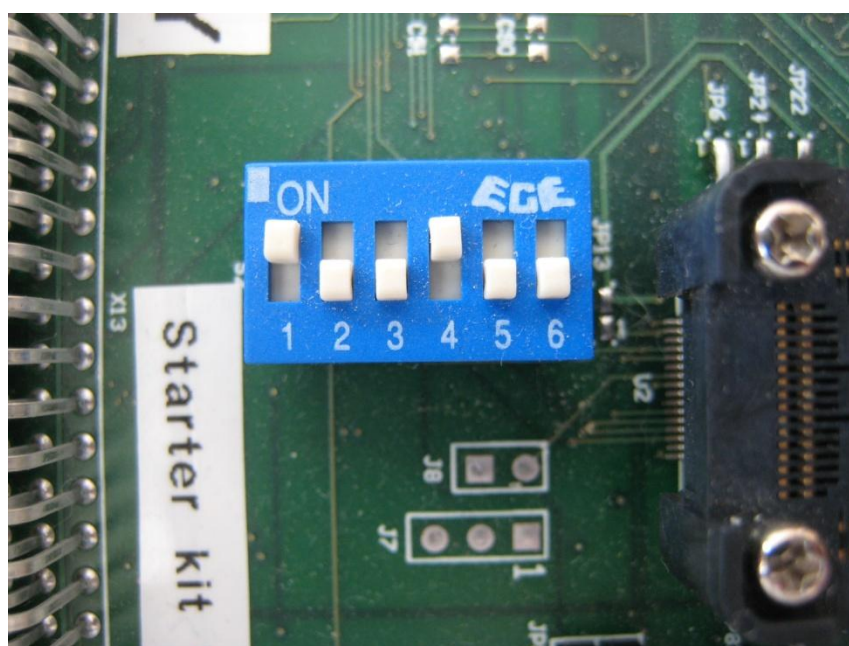
This chapter explains each individual modification.

Switch S2 specifies the operation mode of the communication controller. Its configuration in SPI mode is fixed for the evaluation board SK-91F467-FLEXRAY.

Table 3. Switch S2 settings

Switch	Setting	Function	Description
S2-1	ON	MD0 = 0	Serial communication mode selected
S2-2	OFF	MD1 = 1	
S2-3	OFF	MD2 = 1	
S2-4	ON	MDE0 = 0	SPI interface
S2-5	OFF	MDE1 = 1	10MHz external clock
S2-6	OFF	MDE2 = 1	

Figure 6. Switch S2 overview



3.2 Switch S1 and Jumper JP10, JP11, JP12

Switch S1 is responsible for the application specific settings in SPI mode. All functions are listed in the following table. An example of switch S1-3 for the bit direction is also provided. User should set the switch according to the application.

Table 4. Switch S1 settings

Switch	Setting	Function	Description
S1-1	ON	MDS0=0	Sample data at odd edges of SCK
	OFF	MDS0=1	Sample data at even edges of SCK
S1-2	ON	MDS1=0	SCK is active-high
	OFF	MDS1=1	SCK is active-low
S1-3	ON	MDS2=0	Most significant bit first (MSB)
	OFF	MDS2=1	Least significant bit first (LSB)
S1-4	ON	\	Not used
	OFF	\	Not used

Figure 7. Least Significant Bit First By Data Transfer

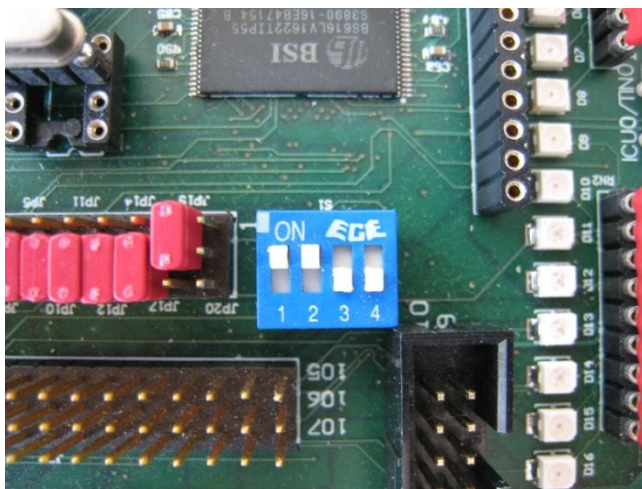
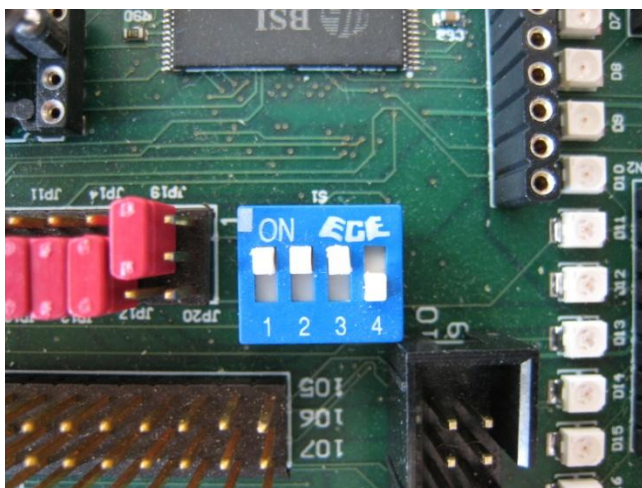


Figure 8. Most Significant Bit First By Data Transfer



By default jumper JP10, JP11 and JP12 connect pin1 and pin2 for parallel communication mode between MCU and CC. Therefore switch S1 is separated from CC MDS[2:0] pins. To use the switch S1 in SPI mode it is necessary to connect pin2 and pin3 of the jumpers.

Figure 9. Pin Jumper With Label '1' For The Pin One On The PCB

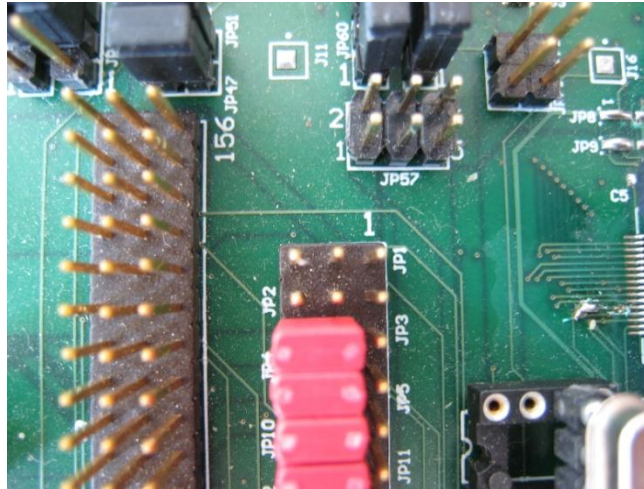
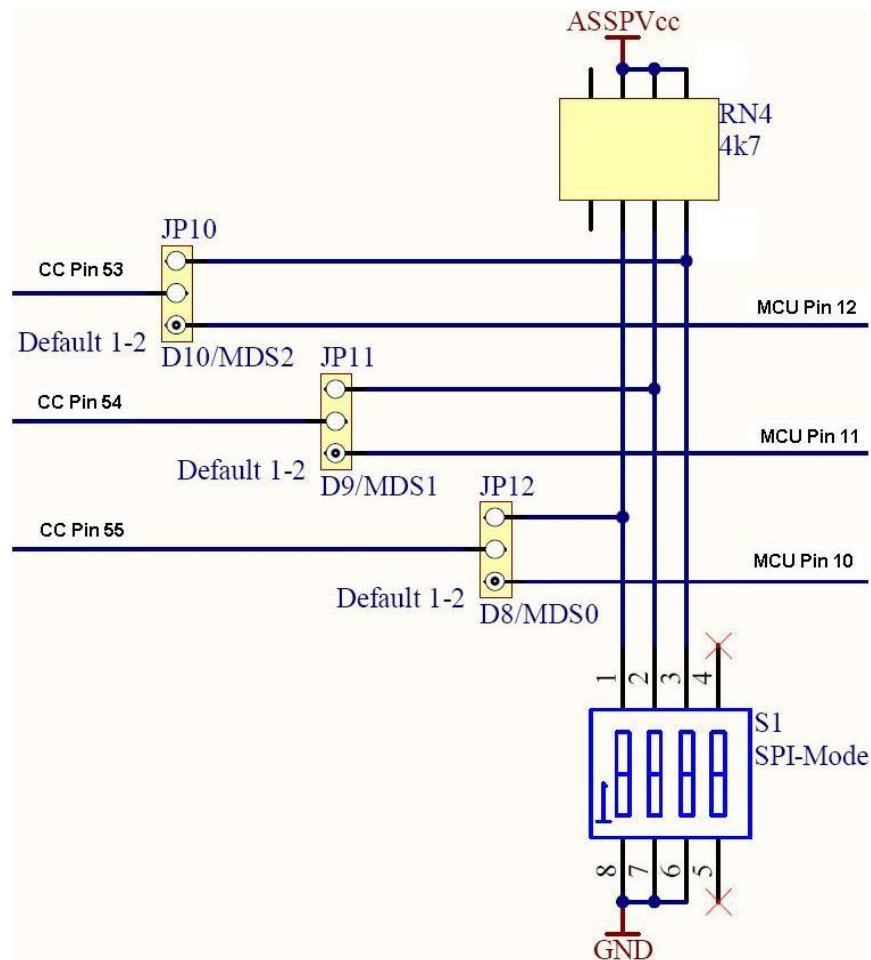


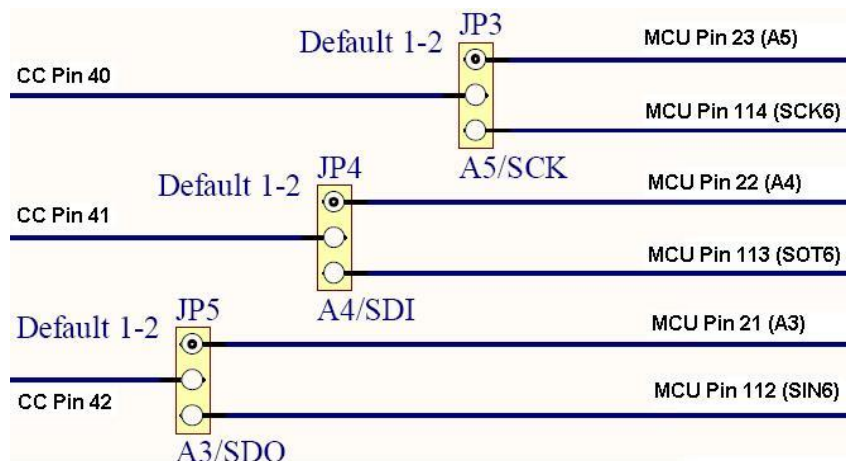
Figure 10. Schematic view of S1, JP10, JP11 and JP12



3.3 Jumper JP3, JP4, JP5

CC pin 40, 41 and 42 have different function for parallel mode and SPI mode. In SPI mode they are the clock and data lines. Jumper JP3, JP4 and JP5 connect pin2 and pin3 to select SPI function.

Figure 11. Schematic View Of Jumper 3,4,5



3.4 Jumper JP1, JP2, JP14, JP17, JP20

The communication controller has five interrupt outputs INT[4:0]. Among them INT0 and INT1 have fixed connection to MCU pin87 and pin88. Other interrupts however have different pin assignment for parallel mode and SPI mode. Therefore jumpers should be configured properly.

Table 5. Jumpers for CC interrupt output in SPI mode

Jumper	Settings for SPI mode	Description
JP1	OPEN	CC pin35 is unused in SPI mode
JP2	OPEN	CC pin36 is unused in SPI mode
JP14	2-3	CC pin58 is INT2 in SPI mode connected to MCU pin 89 and
JP17	2-3	CC pin59 is INT3 in SPI mode connected to MCU pin 90 and
JP20	OPEN	CC pin22 is unused in SPI mode

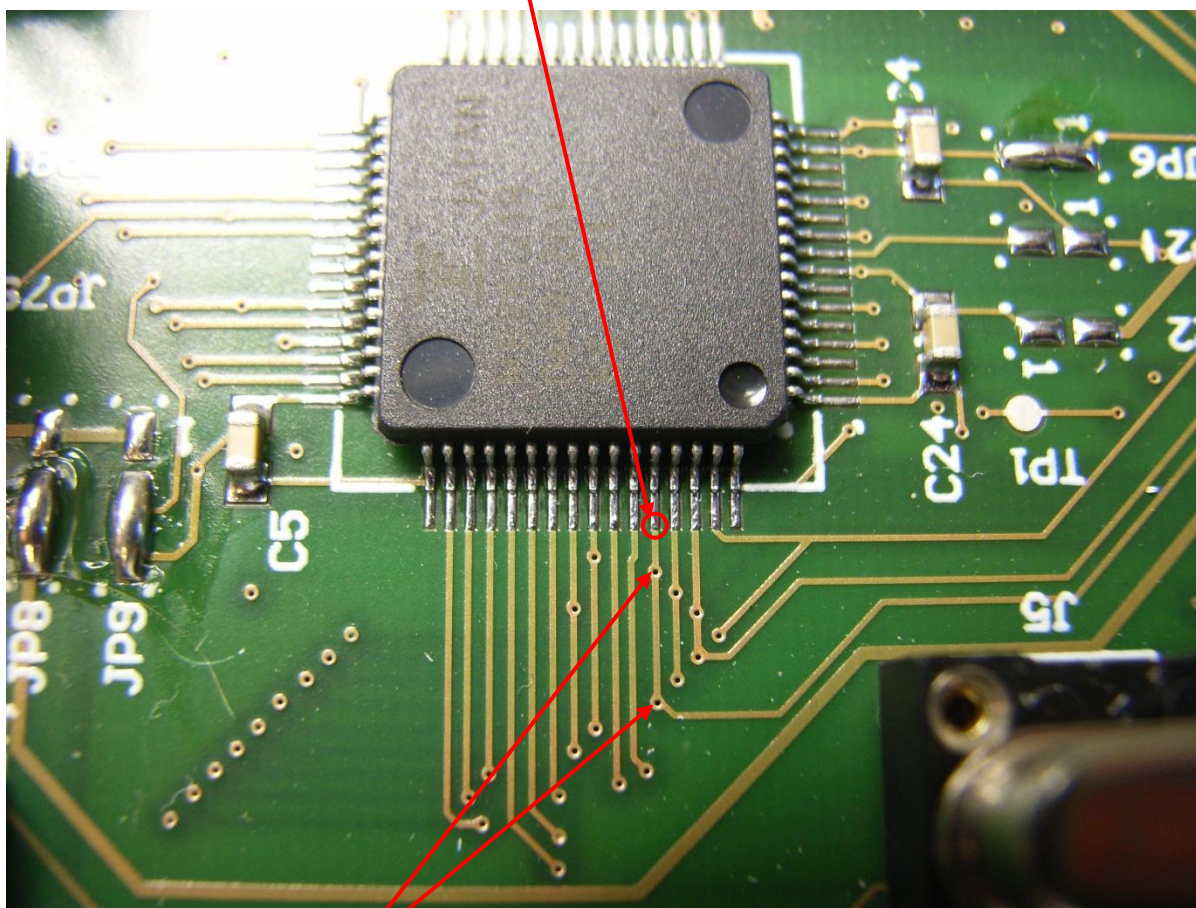
Modification for interrupt INT4 is special and will be introduced in the next chapter.

3.5 CC Pin 60 (INT4)

In SPI mode CC pin60 is assigned to interrupt output INT4 and should be connected to MCU pin91. However in the current PCB version (v1.1) of the evaluation board there is no dedicated jumper for this pin. Instead CC pin60 has a fixed connection to the MCU pin5 and SRAM pin10 (with label U22 on PCB). This connection prevents the monitor debugger in SPI mode, so that the evaluation board is only suitable for STANDALONE mode in SOFTUNE workbench.

To overcome this defect user should manually cut off this connection between CC pin60 and SRAM.

Figure 12. CC Pin60 before Modification for SPI Mode



It is noticed that there are two **via** in connection with CC pin60. In order to cut off the connection the opening must be located between the CC pin and the first via. Please see the following figures.

Figure 13. In Modification

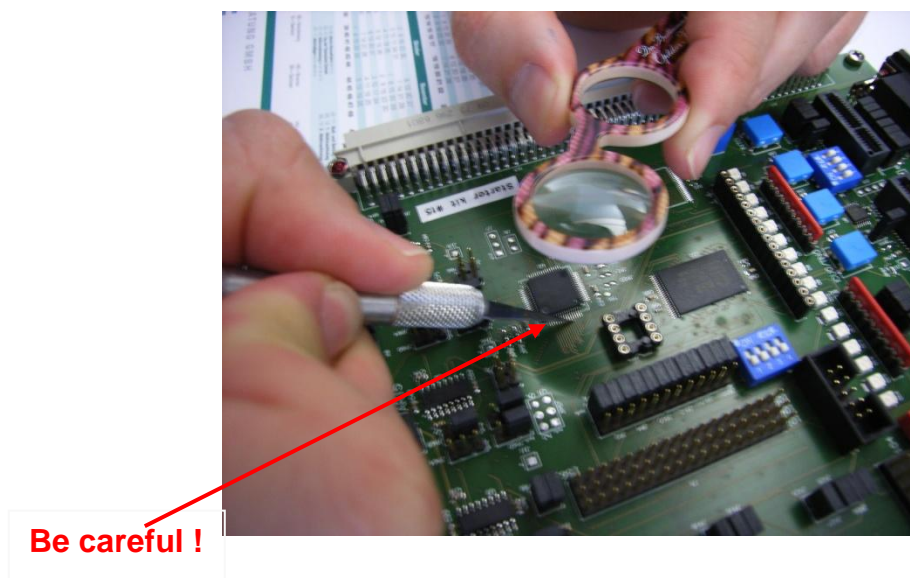


Figure 14. CC Pin60 after Modification

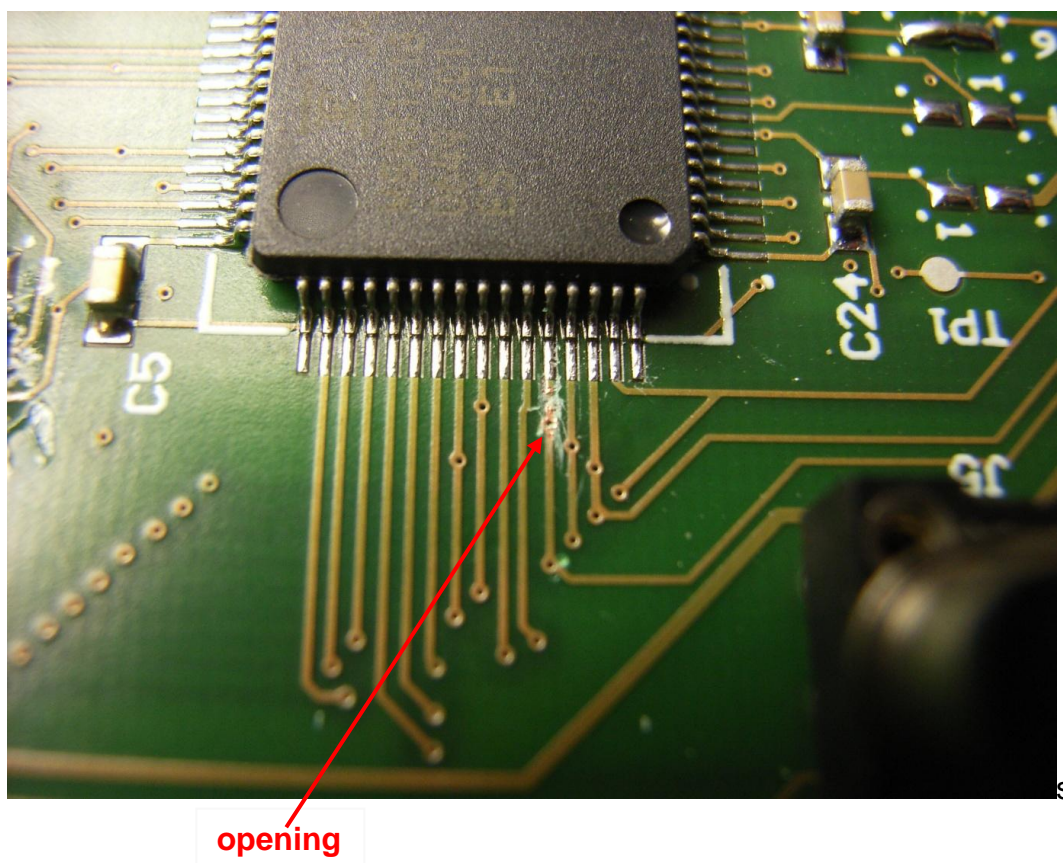


Figure 15. SRAM (U22) for Monitor Debugger



Note: User should realize that if this connection is physically removed, then the evaluation board can only be used for SPI communication mode, respectively, the evaluation board cannot be reconfigured to parallel mode.

To use the INT4 function an additional cable is required to connect CC pin60 and MCU pin91.

4 Document History

Document Title: AN205154 - SPI on SK-91F467-FlexRay

Document Number: 002-05154

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	NOFL	08/31/2007	Initial Release
			02/19/2008	Description in chapter introduction added
*A	5082278	NOFL	01/12/2016	Migrated Spansion Application Note from MCU-AN-300014-E-V11 to Cypress format
*B	5844614	AESATP12	08/30/2017	Updated logo and copyright.

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

[PSoC 1](#) | [PSoC 3](#) | [PSoC 4](#) | [PSoC 5LP](#) | [PSoC 6](#)

Cypress Developer Community

[Forums](#) | [WICED IOT Forums](#) | [Projects](#) | [Videos](#) | [Blogs](#) | [Training](#) | [Components](#)

Technical Support

cypress.com/support

All other trademarks or registered trademarks referenced herein are the property of their respective owners.



Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709

© Cypress Semiconductor Corporation, 2007-2017. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. Cypress products are not designed, intended, or authorized for use as critical components in systems designed or intended for the operation of weapons, weapons systems, nuclear installations, life-support devices or systems, other medical devices or systems (including resuscitation equipment and surgical implants), pollution control or hazardous substances management, or other uses where the failure of the device or system could cause personal injury, death, or property damage ("Unintended Uses"). A critical component is any component of a device or system whose failure to perform can be reasonably expected to cause the failure of the device or system, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from or related to all Unintended Uses of Cypress products. You shall indemnify and hold Cypress harmless from and against all claims, costs, damages, and other liabilities, including claims for personal injury or death, arising from or related to any Unintended Uses of Cypress products.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.