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Spec Title: AN204942 - F2MC - 8L FAMILY, EMC DESIGN GUIDE

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AN204942

F²MC - 8L Family, EMC Design Guide

In the following description, the EMC design guide of 8-bit Cypress microcontroller will be discussed. It describes how external power supply should be connected to the Vcc and Vss pins and offers some suggestions. An overview of internal supply of MCU is made as well to have a better understanding of the design. The EMI measurements in the following described tests are just example measurements. The measured emissions are no data, which are specified in the DS of the microcontroller series.

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Contents

1 Introduction

In the following description, the EMC design guide of 8-bit Cypress microcontroller will be discussed. It describes how external power supply should be connected to the Vcc and Vss pins and offers some suggestions. An overview of internal supply of MCU is made as well to have a better understanding of the design. The EMI measurements in the following described tests are just example measurements. The measured emissions are no data, which are specified in the DS of the microcontroller series.

During the last designs the EMI of the Cypress F²MC-8L microcontroller series could be reduced step by step. The PLL multiplier circuit allows the usage of low crystal frequency to reduce high-frequency noise from the oscillator circuit.

The clock tree is mostly the cause of the noise. Therefore the driver capability of clock buffers is optimized and for one big buffer are used several small clock buffers.

The integration of On-chip bypass capacitors reduces the noise ripple on the internal power supply net so that the broadband noise on the IO pins is improved.

The following description is based on the MB89530 series, but the same situation exists for all current devices of the F²MC-8L family, with or without an external bus interface.

2 Rules to create a good Layout

1. Use max. trace-width and min. length to connect VSS and VDD µC-pins to decoupling capacitors (DeCap)
2. Don’t use stub line to connect the DeCap to µC-pins, let flows the noise current direct through pads of DeCap
3. Use close ground plane direct below MCU package as shield
4. Use different ground systems for analogue, digital, power-driver and connector ground
5. Avoid loop current in the ground system, check for ground loops.
6. Use a star point ground below MCU for analogue and digital ground, use a second star point ground below 5V regulator for MCU, power-driver and connector ground
7. Don't create signal loop on the PCB, minimize trace length
8. Partitioned system into analogue, digital and power-driver section
9. Place series resistor or RC-block for the IO-circuit nearby MCU-pin to reduce the noise on the signal line.
10. Use a capacitor for each connector pin to reduce the noise of external lines, place this capacitor close to connector pin

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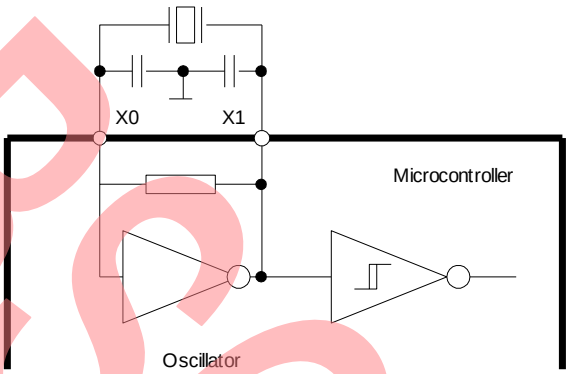
3 Crystal Oscillator Circuit

Error! Reference source not found. shows the oscillator for the 8-bit family. For best performance, the PCB layout of this circuit should cover only a very small area. For the layout is recommended a PCB with two or more layers. Make sure to provide bypass capacitors via shortest distance from X0, X1 pins, crystal oscillator, and ground lines. The lines of the oscillation circuit should not cross lines of other circuits.

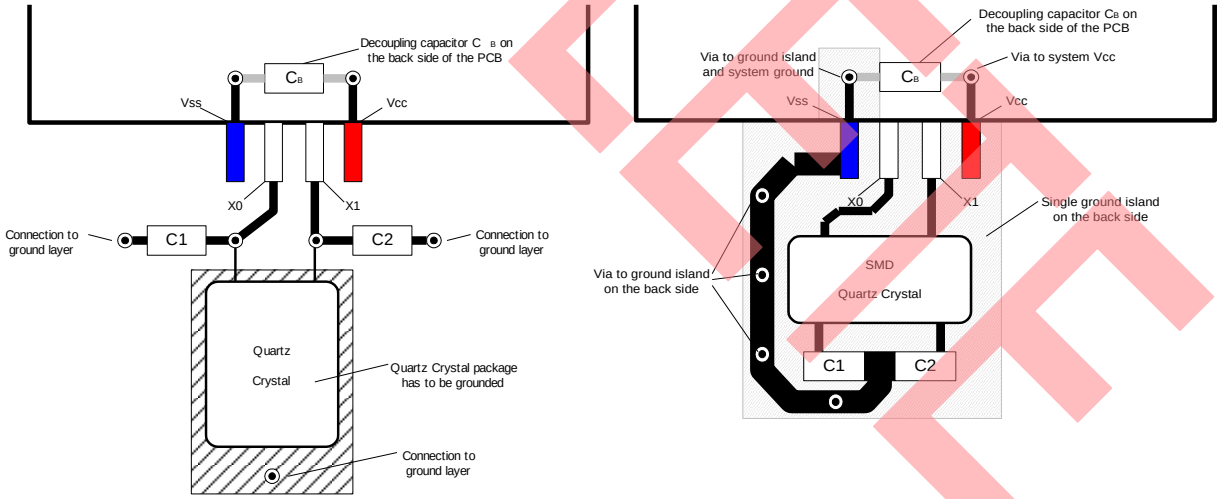
Figure 1. Principle of the Oscillator circuit



It is necessary to avoid coupling noise into the power supply (pin 81/84) of the clock circuit.

The crystal oscillator has to be connected with short lines to X0/X1 and Vss. Note that pin X1 is the output of inverter. Particularly this track should have a short length.

Figure 2. Layout example for oscillator circuit



a) Layout example for a leaded quartz crystal worse layout design, because C1 and C2 are wrong connected to VSS

b) Layout example for a SMD quartz crystal better layout design, because C1 and C2 are connected to Vss and than after with the system ground

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4 Power supply routing

One topic our noise reduction technology is the bypass capacitors. By placing of modules inside the chip, it is possible to connect a bypass capacitor with low impedance where power supply lines are short, effectively reducing the noise to very low flow levels. These bypass capacitors are place into power supply of IO and logic.

Figure 3. Structure of power supply for MCU core and IO-Port

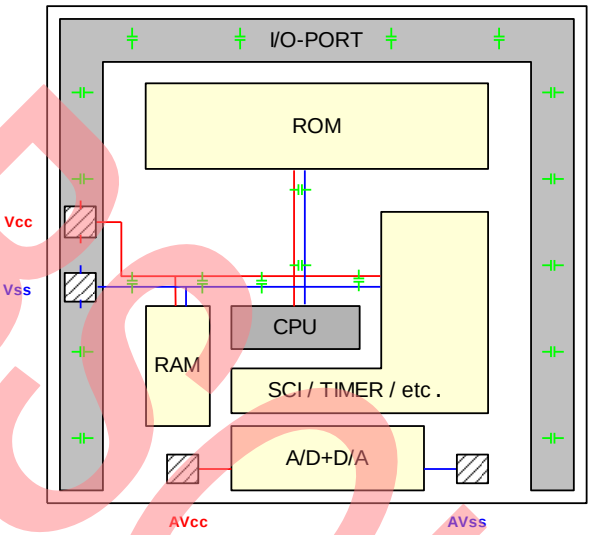

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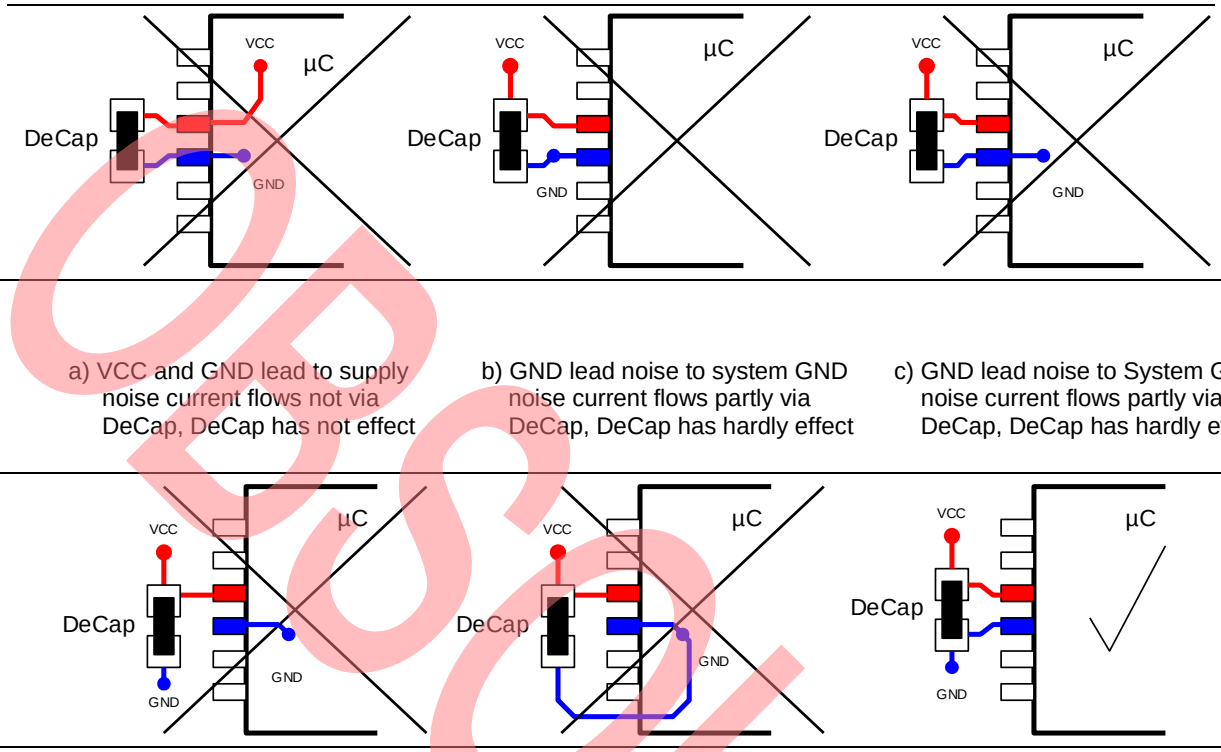
Figure 4.The exactly use of the DeCap (decoupling capacitor)



a) VCC and GND lead to supply noise current flows not via DeCap, DeCap has not effect

b) GND lead noise to system GND noise current flows partly via DeCap, DeCap has hardly effect

c) GND lead noise to System GND noise current flows partly via DeCap, DeCap has hardly effect

d) VCC and GND lead to supply noise current flows not via DeCap, DeCap has not effect

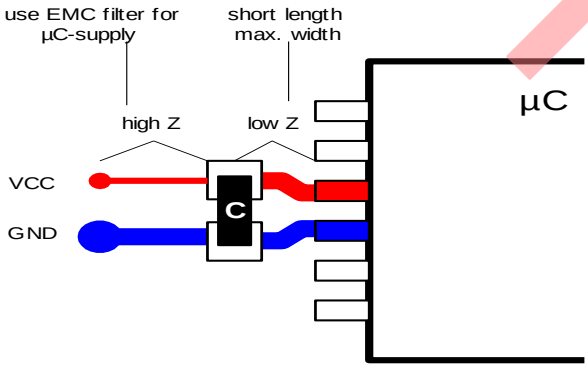
e) GND is not short connected to DeCap. between GND and DeCap flows a loop current DeCap has hardly effect

f) DeCap correct connected to µC and power supply. high speed current will be supported from DeCap

The high-speed current (di/dt) will be supported from the decoupling capacitor only.

Therefore use traces with max. width and min. length between Vss/Vcc pin and DeCap. After DeCap use thin traces to route the trace to the power supply system.

Figure 5. The noise current flows return over the ground line



The exactly use of decoupling capacitors for the Vcc and Vss pins is the basis to reduce the noise, but also the return way between load and MCU ground is not neglect.

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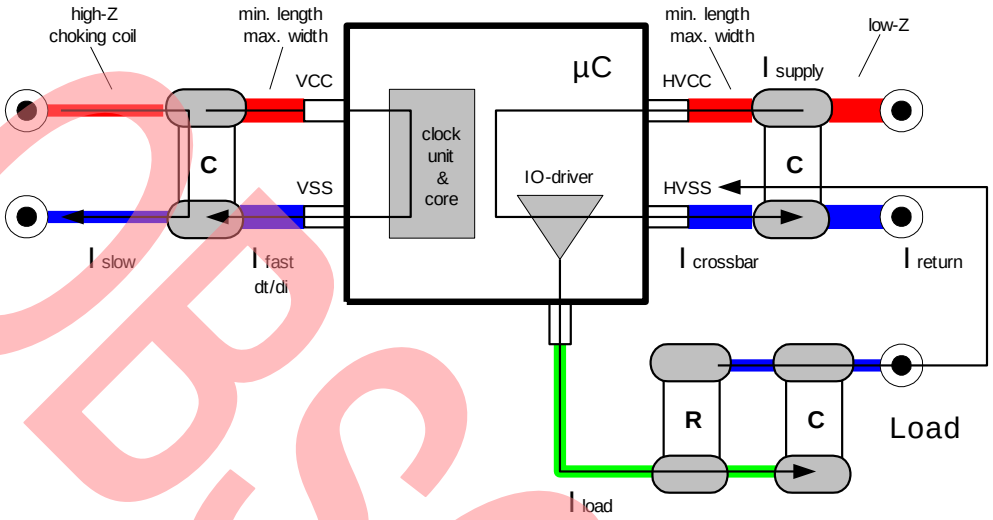
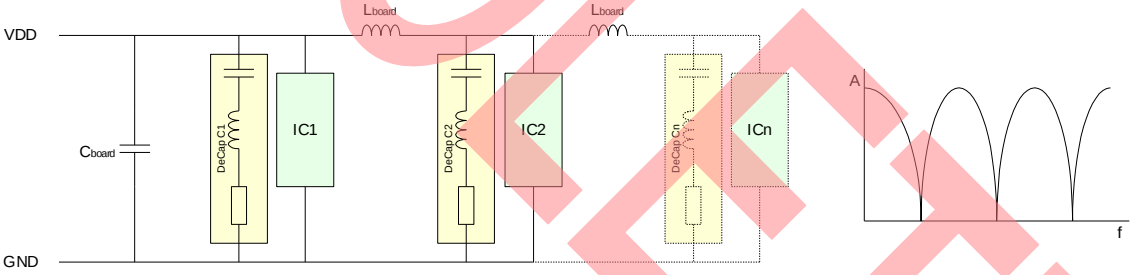
Figure 6. The noise current flows return over the ground line



To ensure an efficient decoupling of the power supply, two capacitors should be placed close on each Vcc pin. The values of both capacitors should have a relationship of about 1:100. Typical values are e.g. 100nF (XR7) and 1nF (COG). The accurate value is depended on the application board, e.g. impedance of PCB or the length of supply lines. However, all of the DeCaps on the PCB should have the same value.

Figure 7. The use of several values of DeCaps lead to undefined resonance frequencies, that's why all DeCaps should have the same value.



For 2-layer boards should be used a closed ground plane (located directly below the MCU). The Vcc supplies should be taken from the bottom layer.

For 4-layer boards should be used the inside layers for GND and Vcc supplies. In this case, both layers form additional capacitor (broadband behaviour) for the power supply.

Figure 8 shows a layout example for the connection of powers supply on the MCU.

This method of Vcc connection reduces the loop of the Vcc lines around the MCU, thus reducing noise emission. A variation of this circuit may be needed, if separate filtered supply voltages are routed to the A/D supplies (pin AVCC/AVSS).

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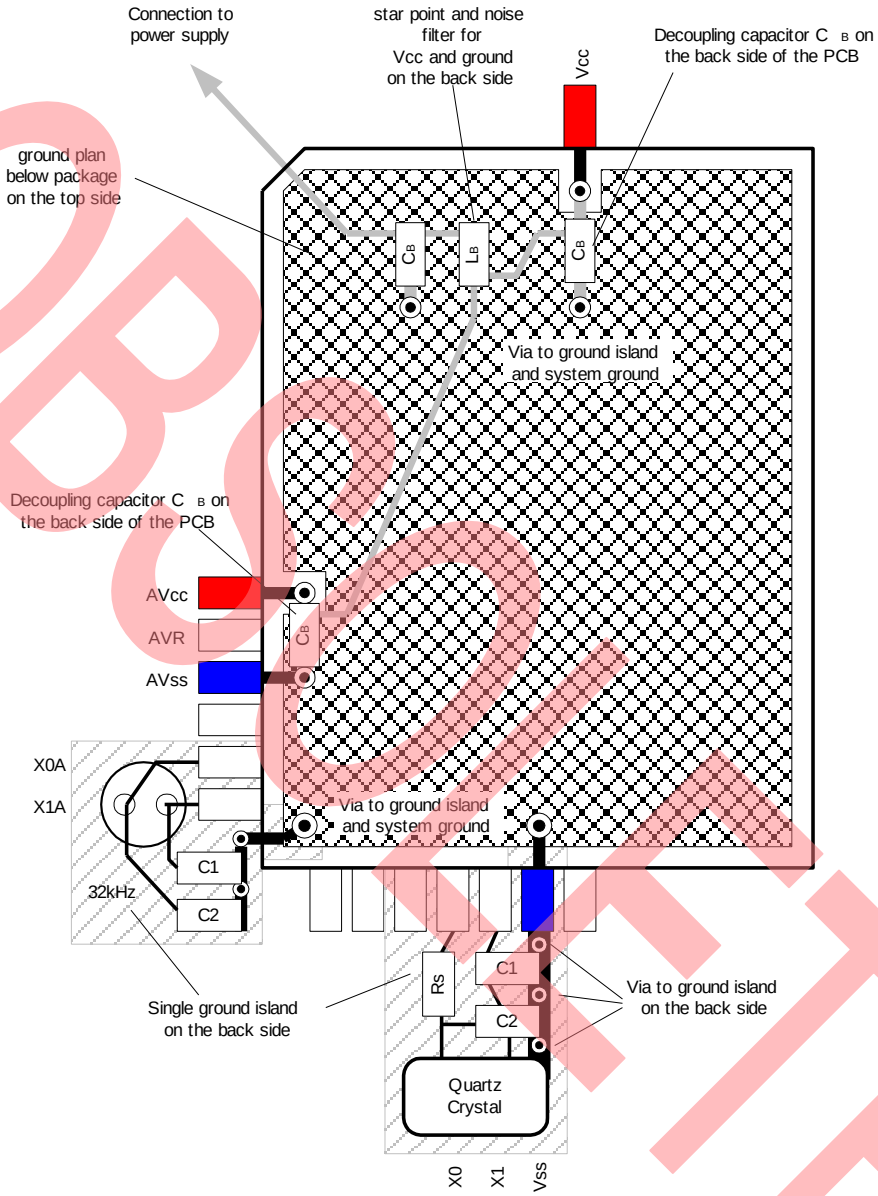
Figure 8. F²MC-8L family with main- and subclock, recommended layout for multiple layers PCB



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Note:

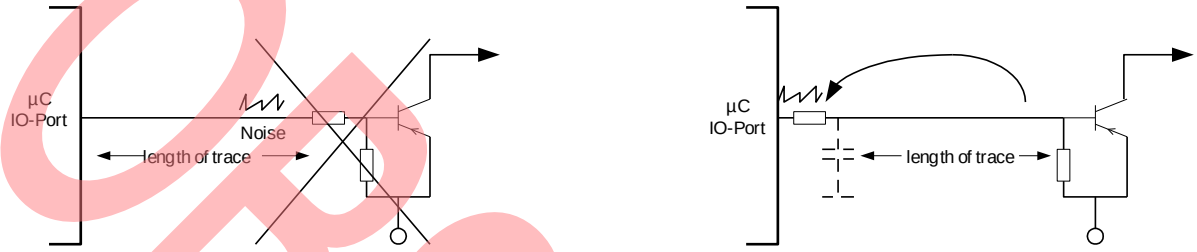
All decoupling capacitors on the Vcc pins should have the same value.

These capacitors should be placed close to the Vcc pin. The Vcc/Vss current should flows through the pad of the capacitor.

5 Noise reduction for general IO pins

To reduce noise, make sure to connect the Vss or Vcc with smoothed power supply, because the noise on the power supply will also distributed via IO-pin, which is configured as static low or high output. **Error! Reference source not found.** shows an example to reduce the noise on output lines.

Figure 9. Place the series resistor close to IO pin because so will be reduced the noise of output



Note: To reduce noise, make sure to connect unused input pins to Vss or Vcc (Use pull-down or pull-up resistor, please check the DS of the microcontroller series).

Also, especially if CMOS Logic is used, floating gates could generate problems regarding high input currents and latch up.

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6 Function of certain MCU pins

Pin name	Function
VDD	Main supply for IO buffer and MCU core
VSS	Main supply for IO buffer and MCU core close to crystal oscillator
AVCC	Power supply for the A/D converter
AVR	Reference voltage input for the A/D converter
AVSS	Power supply for the A/D converter
X0 X0A	Oscillator input, if not used so shall be connected with pull-up or pull-down resistor (see please DS)
X1 X1A	Oscillator output, the crystal and bypass capacitor must be connected via shortest distance with X1 pin, if not used so shall be open

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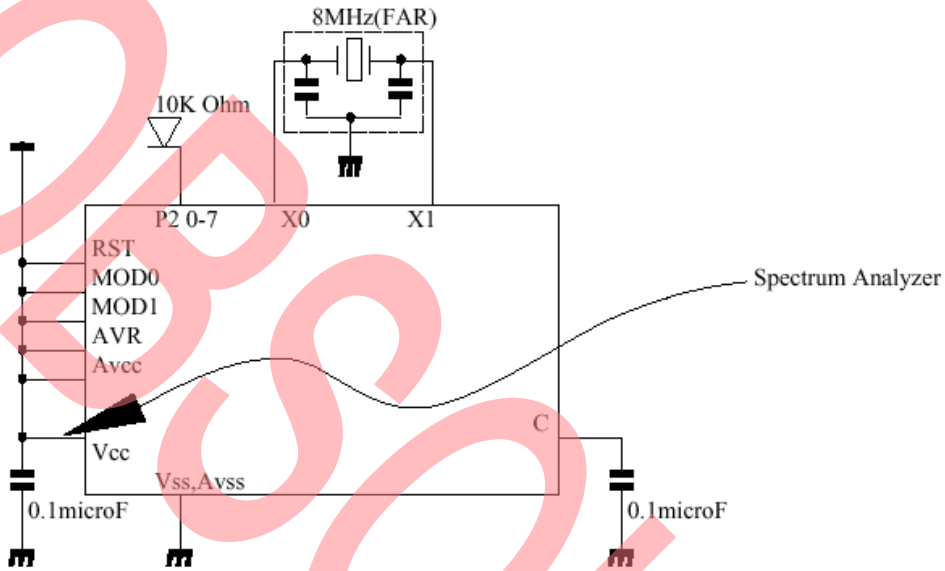
7 EMI Measurement for F²MC-8L family

7.1 Measurement setup

Figure 10. Set-up for noise measurement on power supply



7.2 Measurement procedure

- RF- voltage, measured on VCC power supply by BI mode RUN
- RF- voltage, measured on VCC power supply by BI mode RESET

7.3 Measurements

Sample: MB89538A, MB89538AL, MB89535A

Measurement condition: Ta = 25 deg.C

Power supply: Vcc = 5.0V / 3.0V

Crystal: 8MHz (FAR)

Frequency range: 0MHz to 120MHz, BW: 120kHz

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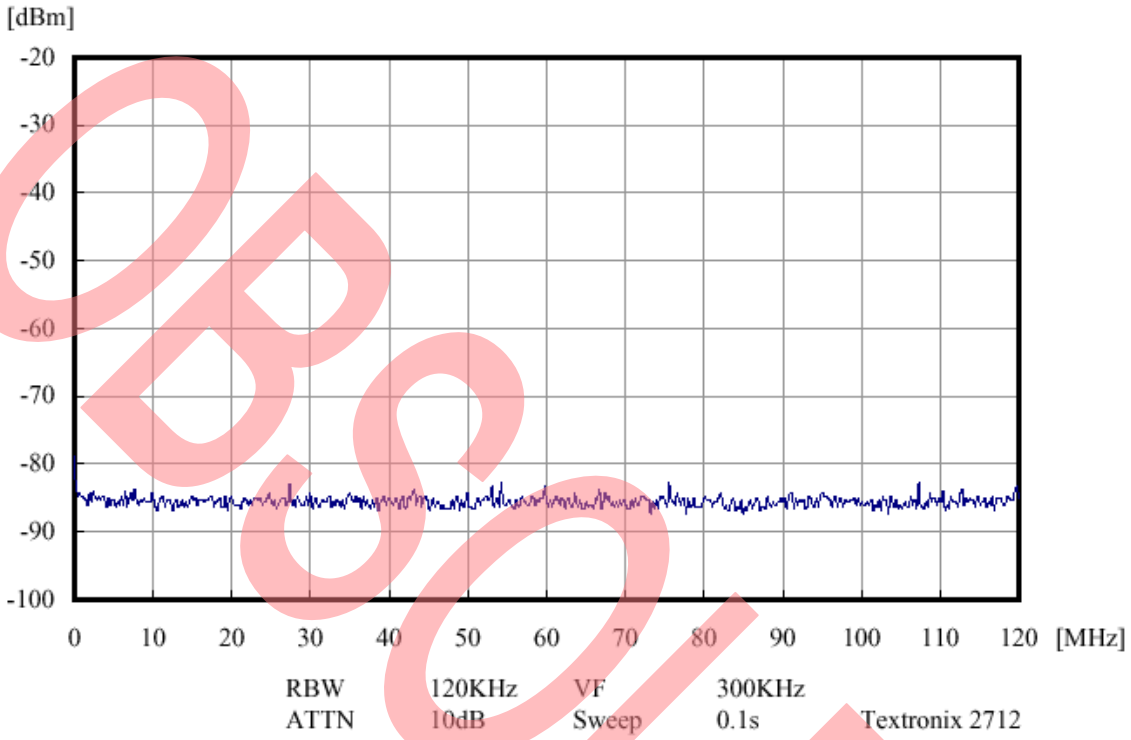
7.4 Blank check

Figure 11. Noise measured on VCC power supply, blank check



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7.5 Noise measurements on VCC

Figure 12. MB89538A - Noise measured on VCC power supply, BI-mode RUN

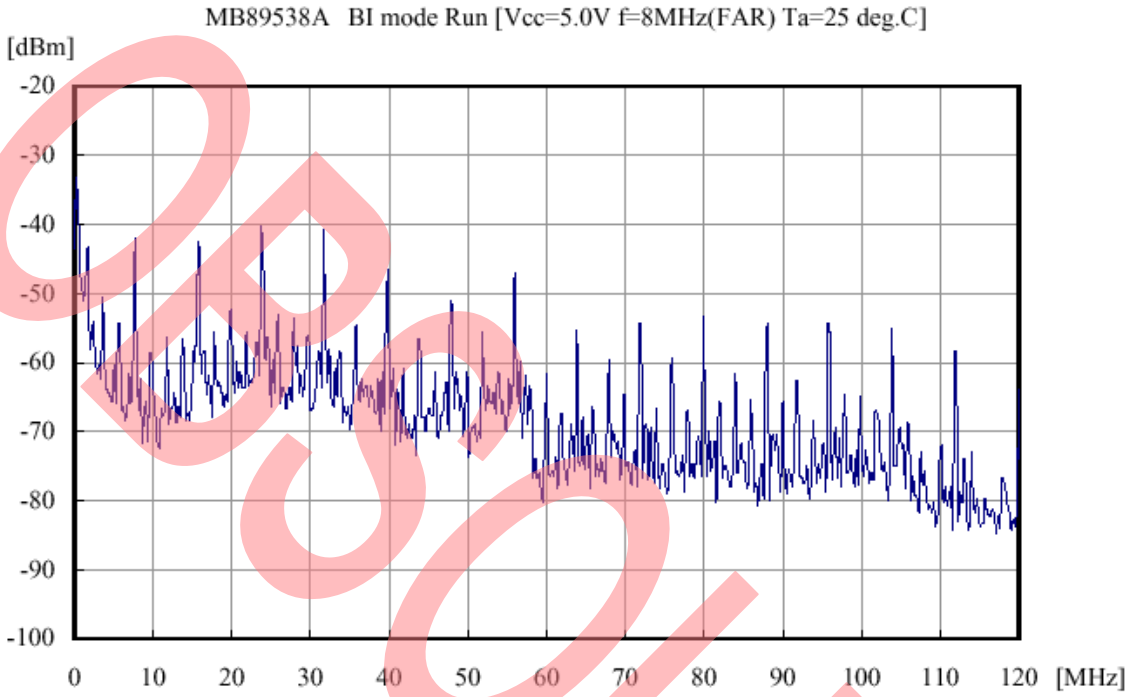

Figure 13: . MB89538AL - Noise measured on VCC power supply, BI-mode RUN

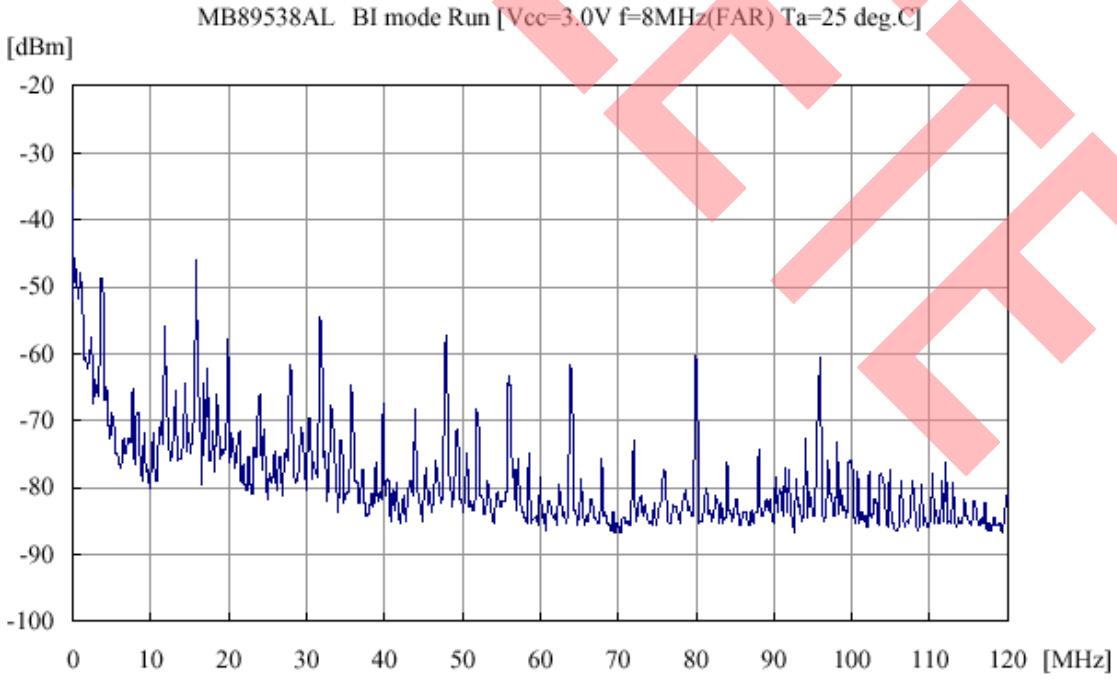

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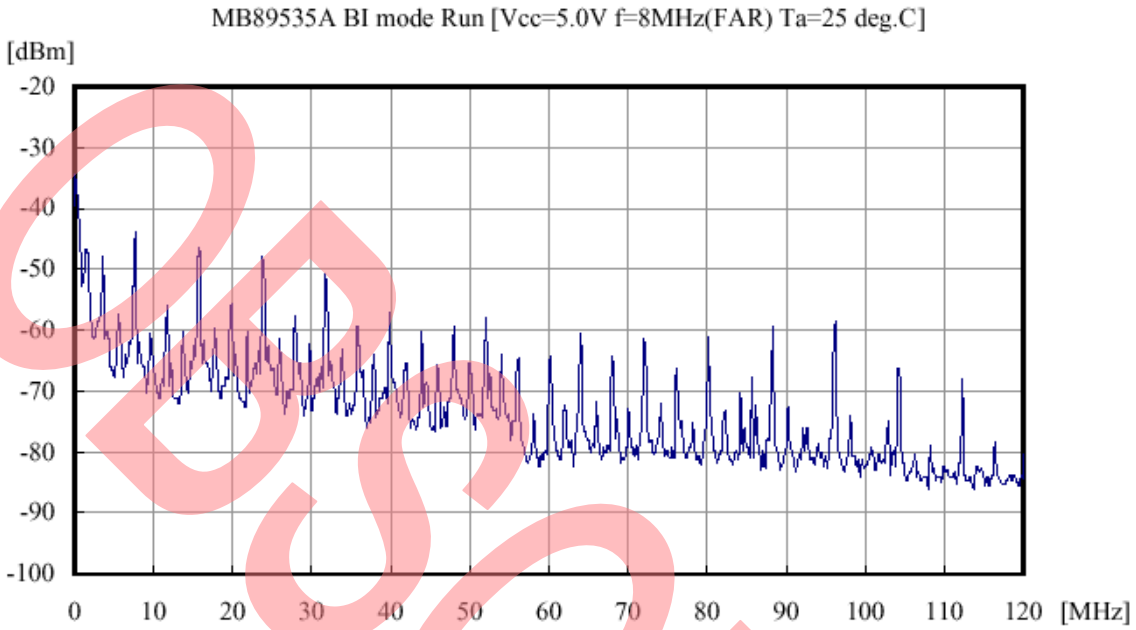
Figure 14. MB89535A - Noise measured on VCC power supply, BI-mode RUN



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Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	NFL.	07/04/2002	V1.0, Initial draft
		NFL	07/18/2002	V1.1, Description DeCap added
*A	5278888	WOFR	05/20/2016	Migrated Spansion Application Note “MCU-AN-389024-E-V11” to Cypress format.
*B	5612332	WOFR	01/31/2017	Spec obsoleted, no further updates planned.

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