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AN204888

FR81S, MB91520 Series, Power Consumption Control

This application note describes the functionality of FR81S Power Consumption Control (PCC). It explains several low power modes and how to enter it and gives some example codes. In addition several results of current consumptions for different LPC (low power consumption) modes are introduced.

Contents

1 Introduction

This application note describes the functionality of FR81S Power Consumption Control (PCC). It explains several low power modes and how to enter it and gives some example codes. In addition several results of current consumptions for different LPC (low power consumption) modes are introduced.

1.1 Low Power Modes

- CPU Sleep Mode
- Bus Sleep Mode
- Standby Watch Mode
- Standby Stop Mode
- Standby Watch mode with power-shutdown
- Standby Stop mode with power-shutdown

Please be referred also to the corresponding hardware manual of FR81S devices.

2 Introduction of Low-Power modes

This Chapter Explains Different Low-Power Modes

The FR81S provides a dedicated Power Management concept which allows to disable different areas on the microcontroller by demand. Especially the clock paths are configurable in that way for reducing the current consumption for different application purposes.

The power consumption of the MCU is dependent on which parts of the MCU are powered and how fast they are clocked. Each clock cycle on a gate, flip-flop and at least on a transistor causes a process where capacities are charged or discharged. This will result into a current consumption and it is greater the higher the clock frequency. Therefore the power consumption reduction will be done by reducing the clock speed or to disable it.

The FR81S series includes several low power modes which will care about different power reduction options.

Power consumption relationship between the several low-power modes:

CPU Sleep Mode > Bus Sleep Mode > Stand-by Watch Mode > Stand-by Stop Mode > Standby Watch Mode with power-shutdown > Standby Stop Mode with power-shutdown

The configuration of all low power modes is done by using "`LPM_InitLPM`" which is located in "lpm.c". There are several parameters for dedicated low power mode configurations. In the following chapters each configuration will be introduced.

2.1 Sleep Modes

There are two different sleep modes available:

- CPU sleep mode: Only CPU is stopped
- Bus sleep mode: CPU and on-chip bus are stopped

In both cases the Hardware Watchdog Timer 1 (HWWDT) stops.

Following wake-up resources for leaving the sleep modes are available for Sleep Modes:

- Reset
- Generation of interrupt requests
- Generation of NMI requests
- Generation of tool break while connected to ICE

For the Normal Run mode to Sleep Mode transition there is a dedicated sequence necessary.

- Set the corresponding SLEEP bit in Standby Control Register STBCR
- Read the written data back from STBCR register
- Perform a dummy process for pipeline adjustment

Example:

```
void LPM_EnterSleepMode()
{
volatile unsigned int ui8Dummy;
                                    /* activation of sleep mode */

STBCR_SLEEP = 1;
/* read back STBCR */
ui8Dummy = STBCR;
/* clean pipeline */
__wait_nop();
/* >>>>> CPU in sleep mode here <<<<< */
}
```

The function '`LPM_EnterSleepMode`' is located in '`lpm.c`'

2.1.1 CPU Sleep Mode

The CPU Sleep Mode is a low power mode with less power savings.

Only the CPU is stopped and no code will be executed. All other MCU modules are still active including the on-chip bus, all peripherals (PCLK1 and PCLK2) and DMA support. The I/O ports are maintained.

List of clock signals which are disabled in sleep modes:

CPU clock (CCLK)

Configuration of CPU Sleep Mode:

The initialization of Power Consumption Control module for CPU Sleep Mode is done by using of following parameters:

```
// configuration of Low Power Mode CPU Sleep Mode
LPM_InitLPM( STOP_EXTERNAL_BUS_CLOCK_ENABLE,
             // Bus Sleep mode
             GPIO_KEEP_STATE_BUS_SLEEP_DISABLE,
             POWER_OFF_DISABLED,
             HARDWARE_CONTROLLED_GPIO_AFTER_WAKEUP,
             POWER_ON_TIMING_9CLK );
```

- No external bus clock
- CPU Sleep Mode configuration
- No power-shutdown
- I/O ports controlled by hardware
- Power on Timing set to 9 Clks

The two different sleep modes are configured in the Standby Control Register "STBCR". For CPU Sleep mode "SLVL" has to be set to "1x".

Example:

```
// Set CPU Sleep mode configuration
STBCR_SLVL = 2;
```

In Addition the external bus clock (TCLK) can also disable in sleep mode dependent on the setting in 'DIVR1_TSTP'.

- 0 → External Bus Clock does not stop
- 1 → External Bus Clock stops

2.1.2 Bus Sleep Mode

Compared to the CPU Sleep mode the Bus Sleep mode is deactivating also the on-chip bus using the HCLK clock.

The on-chip bus is a 32-bit width, high-speed internal bus. It has a 2-layer structure for XBS and DMA, and they can operate simultaneously. The bus master of the XBS layer is accessed from the XBS. The bus master of the DMA layer is accessed from the DMA.
The bus slave of both layers has an external bus interface, CAN, 16/32-bit peripheral bus bridge and others. The bus slave of only DMA layer has an access to the XBS.

In addition also the CPU will be stopped and no code will be fetched. But the peripherals using the PCLK1 and PCLK2 are still running.

In case of a DMA transfer request the on-chip bus clock resumes temporarily and stops after the DMA transfer is completed.

List of clock signals which are disabled in sleep modes:

- CPU clock (CCLK)
- On-chip bus clock (HCLK)
- CAN Prescaler clock is stopped in case on-chip bus clock is selected as CAN prescaler clock.

Configuration of Bus Sleep Mode:

The initialization of Power Consumption Control module for Bus Sleep Mode is done by using of following parameters:

```
// configuration of Low Power Mode (lpm)
LPM_InitLPM( STOP_EXTERNAL_BUS_CLOCK_ENABLE,
             // Bus Sleep Mode
             GPIO_HIZ_BUS_SLEEP_ENABLE,
             POWER_OFF_DISABLED,
             HARDWARE_CONTROLLED_GPIO_AFTER_WAKEUP,
             POWER_ON_TIMING_9CLK );
```

- No external bus clock
- Bus Sleep Mode configuration
- No power-shutdown
- I/O ports controlled by hardware
- Power on Timing set to 9 Clks

The configuration of Bus Sleep mode is done in Standby Control Register "`STBCR`". For Bus Sleep mode "`SLVL`" has to be set to "0x".

Example:

```
// Set Bus Sleep mode configuration
STBCR_SLVL = 0;
```

2.2 Stand-by Watch Mode

In Stand-by Watch Mode all operations are stopped except some clock oscillations and the clock timer. The interrupt of the still running watch timer can be used to wake-up the system periodically after determined time slots.

Following clocks are deactivated in stand-by watch mode:

- CPU clock (CCLK)
- CAN Prescaler Clock
- On-chip bus clock (HCLK)
- Peripheral clock (PCLK)
- Extended bus I/F clock (TCLK)
- PLL clock (PLLCLK)

Important Note:
The stand-by mode must only be entered when main RUN or sub RUN mode is active. In case of a PLL RUN state to stand-by mode transition an illegal stand-by mode transition will be detected and dependent on 'CPUAR_PSTRE' setting a reset will be generated.
A transition into stand-by mode is prohibit while FLASH programming or erasing.

In all Stand-by modes the port pins can be configured as for maintaining the port pin level while entering the low-power mode or to set the port pin to high impedance. This is configurable in Standby Control Register '`STBCR_SLVL`'. Please be referred to chapter 2.5 for further information.

Preparation of Stand-by Watch Mode:

As the shutdown mode must not be enabled in this mode '`PUMCTRL_SHDE`' has to set to '0'

In case PLL RUN mode is active CPU must go into main RUN state first.

In the given example program *91520_ppc_91526* the main clock is entered by following command:

```
SYSCLOCK_SelectMainClock(DIVIDE_BY_1 , DIVIDE_BY_1, DIVIDE_BY_1);
// >>>>> CPU is running on main clock now <<<<<
```

'SYSCLOCK_SelectMainClock' is located in 'sysclock.c'

All wake-up relevant pending interrupts have to be cleared before entering the low power mode.

The stand-by watch mode will be activating by a dedicated procedure:

- Set the corresponding TIMER bit in Stand-by Control Register STBCR
- Read the written data back from STBCR register
- Perform a dummy process for pipeline adjustment

Example:

```
void LPM_EnterTimerMode()
{
    volatile unsigned int ui8Dummy;

    // activation of timer mode
    STBCR_TIMER = 1;

    // read back STBCR
    ui8Dummy = STBCR;

    // clean pipeline
    __wait_nop();

    // >>>>> CPU in timer mode here <<<<<
}
```

The function '`LPM_EnterTimerMode`' is located in '`lpm.c`'

Wake-up resources for leaving the standby watch mode:

- Reset
- Generation of interrupt requests
- Generation of NMI requests
- Generation of tool break while connected to ICE

2.3 Stand-by Stop Mode

In Stand-by Stop Mode all operations and clocks of the whole microcontroller are stopped which results into a minimum of power consumption of the device.

Following clocks are deactivated in Stand-by Stop mode:

- CPU clock (CCLK)
- CAN Prescaler Clock
- On-chip bus clock (HCLK)
- Peripheral clock (PCLK)
- Extended bus I/F clock (TCLK)
- PLL clock (PLLCLK)
- Main clock (MCLK)
- Sub clock (SBCLK)
- Watchdog Timer 1 (hardware watchdog timer)

Preparation of Stand-by Stop Mode:

As the shutdown mode must not be enabled in this mode '`PUMCTRL_SHDE`' has to set to '0'

In case PLL RUN mode is active CPU must go into main RUN state first.

The Stand-by Stop Mode will be activating by a dedicated procedure:

- Set the corresponding STOP bit in Stand-by Control Register STBCR
- Read the written data back from STBCR register
- Perform a dummy process for pipeline adjustment

Example:

```
void LPM_EnterStopMode()
{
    volatile unsigned int ui8Dummy;

    // activation of timer mode
    STBCR_STOP = 1;

    // read back STBCR
    ui8Dummy = STBCR;

    // clean pipeline
    __wait_nop();

    // >>>>> CPU in timer mode here <<<<<
}
```

The function '`LPM_EnterStopMode`' is located in '`lpm.c`'

Wake-up resources for leaving the standby watch mode:

- Reset
- Generation of interrupt requests
- Generation of NMI requests
- Generation of tool break while connected to ICE

2.4 Power-Shutdown Modes

In addition to the regular standby low power modes the timer and stop mode can be configured as “power-shutdown” which means that the power supply of varies MCU modules will be switched of dependent of the low power mode. In Standby Stop Power-Shutdown mode almost all functions are deactivated and the minimum of power consumption is required.

The power-shutdown mode is activated while of low power mode initialization by setting the Shutdown Enable bit “PMUCTRL_SHDE” in PMU Control Register.

Example:

```
// enable shutdown mode
PMUCTRL_SHDE = 1;
```

The low power mode is activated by setting the corresponding low power mode bit in Standby Control Register (STBCR) and is identical to the low power mode transition as done in the corresponding regular Standby Watch/Stop mode.

Wake-up resources for leaving the standby power-shutdown modes:

Reset

External interrupt request

Generation of NMI requests

In addition for the Standby Watch mode following wake-up resources are valid:

- Generation of RTC interrupt request
- Generation of main/sub timer interrupt request

The CPU always starts operation from the reset state.

Important Notes:
After a valid wake-up event has happen the MCU performs a reset. The wake-up event is indicated in the PMU interrupt flag registers “PMUINTF0..2”.
In power shutdown low power modes the regular RAM data will be lost. Therefore please be sure to save all needed application data into BACKUP-RAM.

2.5 I/O port signal behavior in low power mode

The port pins of FR81S behave different in low power modes dependent on the used configuration. Compared to the Sleep modes where the I/O ports are maintained by the hardware the behavior of port signals can be configured in Standby Modes.

I/O ports can be configured for:

- Maintain the value while of low power mode transition
- I/O ports will disable the output function and makes them high impedance

For the standby modes the I/O behavior is configurable via the Standby Level setting in Standby Control Register "STBCR_SLVL".

Figure 1 shows how to configure the I/O port behavior.

Figure 1. I/O port behavior setting in Standby modes

Mode	SLVL[1:0]	Operation control
Stop mode	0x	Does not make pins high impedance.
	1x	Makes pins high impedance.
Watch mode	0x	Does not make pins high impedance.
	1x	Makes pins high impedance.

Example:

```
// Set port pins to high impedance while of Standby low power modes
STBCR_SLVL = 2;
```

In standby power-shutdown modes the MCU performs a reset after a wake-up event. The maintenance of port pin values can be configured in two ways:

- I/O state is maintained until returning from standby
- I/O state is maintained until IOCT register is cleared by software

This behavior is defined in "PMUCTLR_IOCTMD". In case of software cancellation of I/O maintenance the I/O Clear Timing bit "PMUCTLR_IOCT" has to be set to '1'.

Example:

```
// I/O ports are controlled by SW after wake up (PMUCTRL_IOCT = 1 set by
SW)
PMUCTLR_IOCTMD = 1;
```

In the sample program *91520_ppc_91526* there are several ports set as output (e.g. P02_0) which shows the behavior of I/O ports while of low power modes.

2.6 Debugging of low power modes

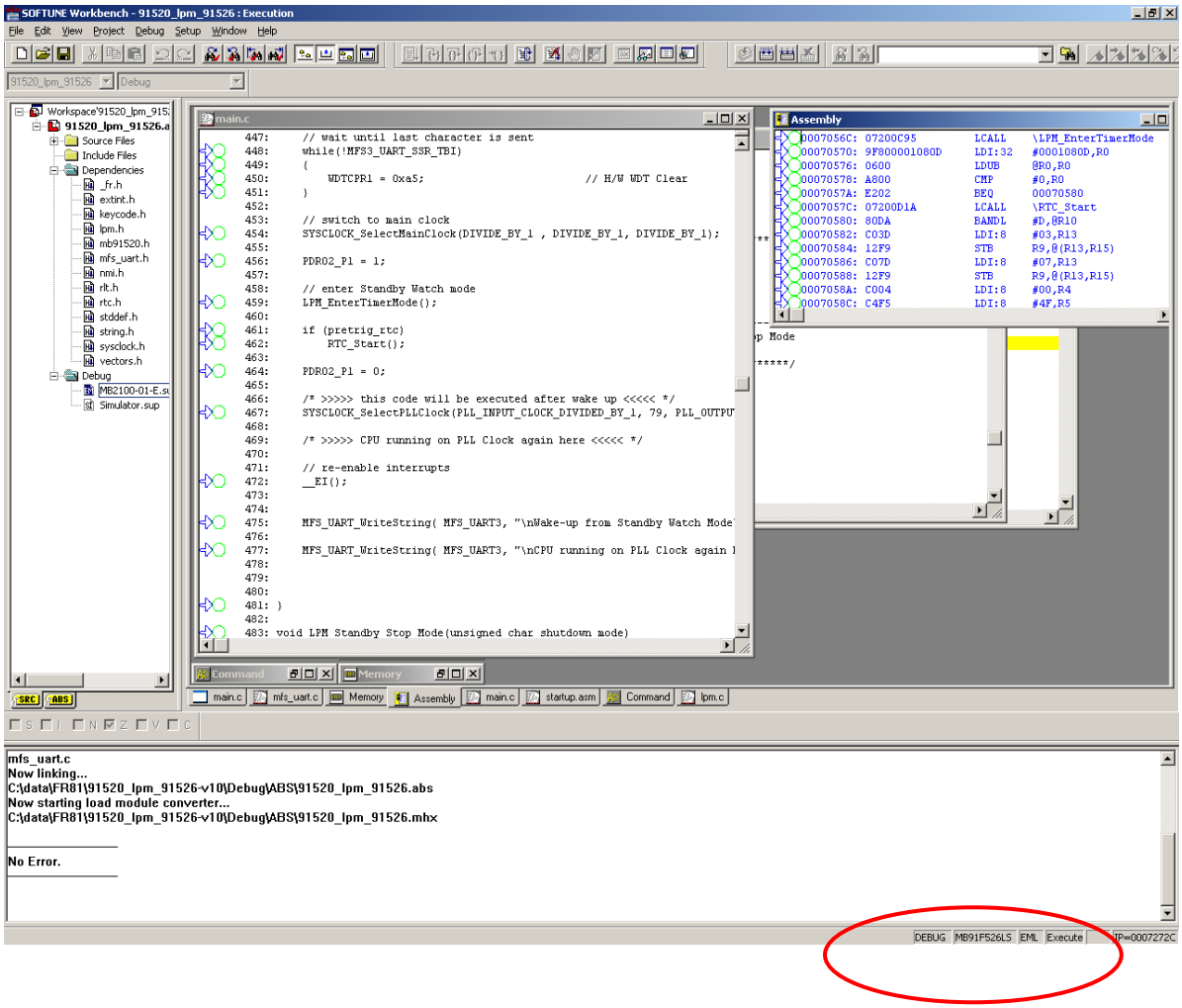
The behavior of low power modes in “debugger mode” is a bit different.

While entering the low power mode the OCD (on-chip debugger) bus is activated which means that the DEBUG I/F clock is still running even in power shutdown modes. This results into a higher power consumption of the MCU. The main clock (MCLK) is supplied for DEBUG I/F main clock (M_MCLK).

Important Notes:
In case of power-shutdown modes no reset will be performed after wake-up event. The program will be continued similar to regular standby modes.
In debugger mode power shutdown low power modes are not supported.

With the given sample program *91520_ppc_91526* it is possible to enter each low power mode.

The status of CPU is displayed in the status bar in the bottom of debugger window.



Dependent of the used low power mode different status information will appear:

Regular program execution:

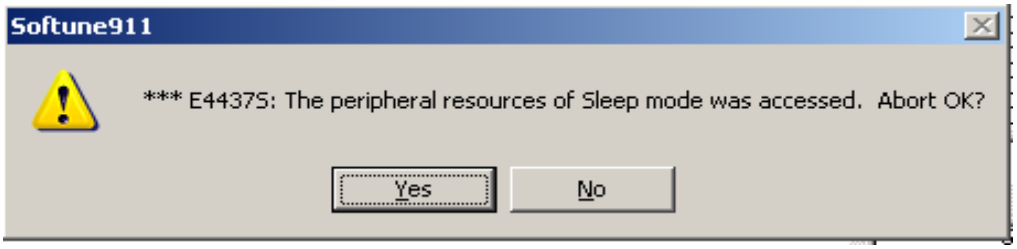
CPU Sleep mode:

Bus Sleep mode:

Standby watch mode:

Standby stop mode:

Important Note:
In case of activated “Memory” window please deactivate the “monitoring” function before entering a low-power mode. Otherwise a failure message will appear.



2.7 Sleep Modes

There are two different sleep modes available:

- CPU sleep mode: Only CPU is stopped
- Bus sleep mode: CPU and on-chip bus are stopped

2.8 Standby Voltage Regulator Mode

The FR81S series includes an autonomous independent internal step-down voltage regulator which supplies the CPU and other modules with different voltages dependent on the current device state. It has to be configured in the Regulator Output Voltage Select Register *REGSEL*. For the low power modes there is a dedicated bit field called *REGSEL_STRSEL* which configures the output voltage in standby modes.

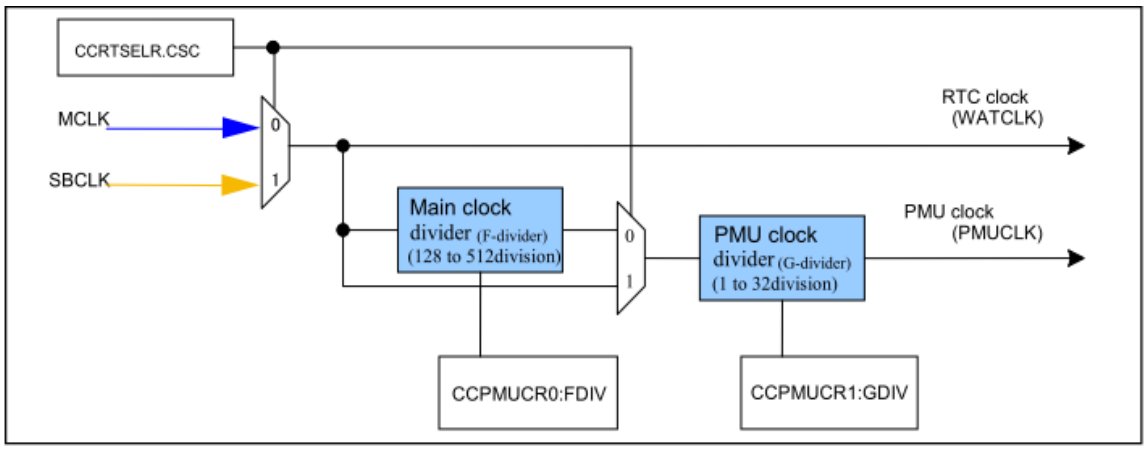
Important Note:
The default value of *REGSEL_STRSEL* is 0,9V **but has to set to 1,2V** before entering any standby low-power mode.

The settings are only necessary in case of standby low-power modes. In Sleep modes the regulator mode is switched to “Main mode” or “Sub mode” settings.

2.9 PMU Clock conditions

The PMU clock (PMUCLK) is the operation clock of Power Management Unit. Before entering any standby mode several conditions of this clock has to be fulfilled otherwise a regular RUN to Standby transition cannot guaranteed. In **Error! Reference source not found.** the generation of PMUCLK is illustrated. Dependent on the actual used clock s ource (main/sub clock) different clock divider settings are activated. In sub clock mode only “CCPMUCR1:GDIV” is active. The clock source itself is selectable with “CCRTSELR:CSC”.

Figure 2. Watch/Power Management Clock Generation Unit



Due to following PMU clock specification limitations the clock divider has to used consequently:

1. F-divider (“CCPMUCR0:FDIV”) must be set for a resulting PMU clock of maximum 32KHz. The default setting of F-divider is a division rate of 128 which is adequate for a 4MHz main oscillation frequency. In case higher frequencies are used the “FDIV” settings has to change accordingly.
2. G-divider (“CCPMUCR1:GDIV”) must be set for a PMU clock frequency which is 4 times lower as the peripheral clock (PCLK1). This setting is only necessary in case the SUB clock is used as the F-divider is bypassed.

3 Current consumption in low power modes

Dependent on the used low power mode the current consumption is different. In this chapter the current consumption of all low power modes are introduced which were measured exemplary on a used starter kit *SK-91520-176PMC* and the sample program *91520_ppc_91526-v10*.

The measurements were done under following conditions:

- All MCU pins disconnected from further components on the starter kit (JP20 – JP36) removed.
- All port pins configured as output driving 'low'-level. (except UART input SIN3_0)
- Supply voltage of MCU (MCUVCC) directly connected to a power supply unit. (Remove JP15 and connect the power supply on pin2)
- For sleep modes CLKB/CLKP/CLKT clock pre-scaler are set to maximum values

Low Power mode	Target Values (VCC=5V)		Measured Values	
	Typ	Max	VCC = 5V	VCC = 3,3V
CPU Sleep Mode	n/a	n/a	1,544 mA*	1,074 mA*
Bus Sleep Mode	n/a	n/a	1,514 mA*	1,051 mA*
Standby Watch Mode - I/O ports maintained - I/O ports high-z	1,5 mA	2,61 mA	1,441 mA 1,455 mA	0,942 mA 0,950 mA
Standby Stop Mode - I/O ports maintained - I/O ports high-z	450 µA	1400 µA	477,7 µA 481,1 µA	477,4 µA 480,0 µA
Power Shutdown Standby Watch Mode - I/O ports maintained - I/O ports high-z	1,1 mA	1,3 mA	1,026 mA 1,035 mA	0,519 mA 0,524 mA
Power Shutdown Standby Stop Mode - I/O ports maintained - I/O ports high-z	30 µA	110 µA	66,5 µA 66,5 µA	64,2 µA 64,2 µA

*The measured current consumption values in Sleep Modes are dependent on the used peripheral modules.

- Further exemplary measurement results for MB9157x and MB9159x series:

- MB9157x series:

Low Power mode	Target Values (VCC=5V)		Measured Values
	Typ	Max	VCC = 5V
Bus Sleep Mode	n/a	n/a	2,37mA
Standby Watch Mode - I/O ports high-z	900 µA	1550 µA	900 µA
Standby Stop Mode - I/O ports high-z	400 µA	1200 µA	637 µA
Power Shutdown Standby Watch Mode - I/O ports high-z	320 µA	480 µA	309 µA
Power Shutdown Standby Stop Mode - I/O ports high-z	120 µA	240 µA	58 µA

- MB9159x series:

Low Power mode	Target Values (VCC=5V)		Measured Values
	Typ	Max	VCC = 5V
Standby Watch Mode - I/O ports high-z	800 µA	1950 µA	860µA
Standby Stop Mode - I/O ports high-z	250 µA	1400 µA	660 µA
Power Shutdown Standby Watch Mode - I/O ports high-z	280 µA	380 µA	230 µA
Power Shutdown Standby Stop Mode - I/O ports high-z	100 µA	200 µA	60 µA

4 Additional Information

- Information about FUJITSU Microcontrollers can be found on the following Internet page:
  http://www.cypress.com/cypress-microcontrollers
- The software examples related to this application note are: *'91520_pcc_91526-v10'*
  It can be found on the following Internet page:
  http://www.cypress.com/documentation/software-and-drivers/91520-pcc-91526-v10

5 Document History

Document Title: AN204888 - FR81S, MB91520 Series, Power Consumption Control

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	MKEA	05/08/2012	V1.0, First draft, PBe
			06/19/2012	V1.1, Adding of current consumptions in low power modes
			07/06/2012	V1.2, Adding of current consumptions for MB9157x and MB9159x series
			08/06/2012	V1.3, Adding Standby Voltage Regulator Mode settings in low-power mode and PMU clock limitation.
*A	5059060	MKEA	12/28/2015	Converted Spansion Application Note “MCU-AN-381007-E-V13” to Cypress format
*B	5836336	AESATMP9	07/28/2017	Updated logo and copyright.
*C	6038716	NOFL	01/20/2018	Updated logo and links. Updated Sales page and Copyright year.

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