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Replaced by: NONE

AN204879

FM3 MB9XFXXX Family with Multifunction Timer

This Application-Note describes the usage of the Multifunction Timer (MFT) of the new Cypress FM3 ARM® Cortex™-M3 MCU (e.g. MB9BF506R). Depending on the device, there are up to three MFT units integrated in the device

Contents

1 Introduction

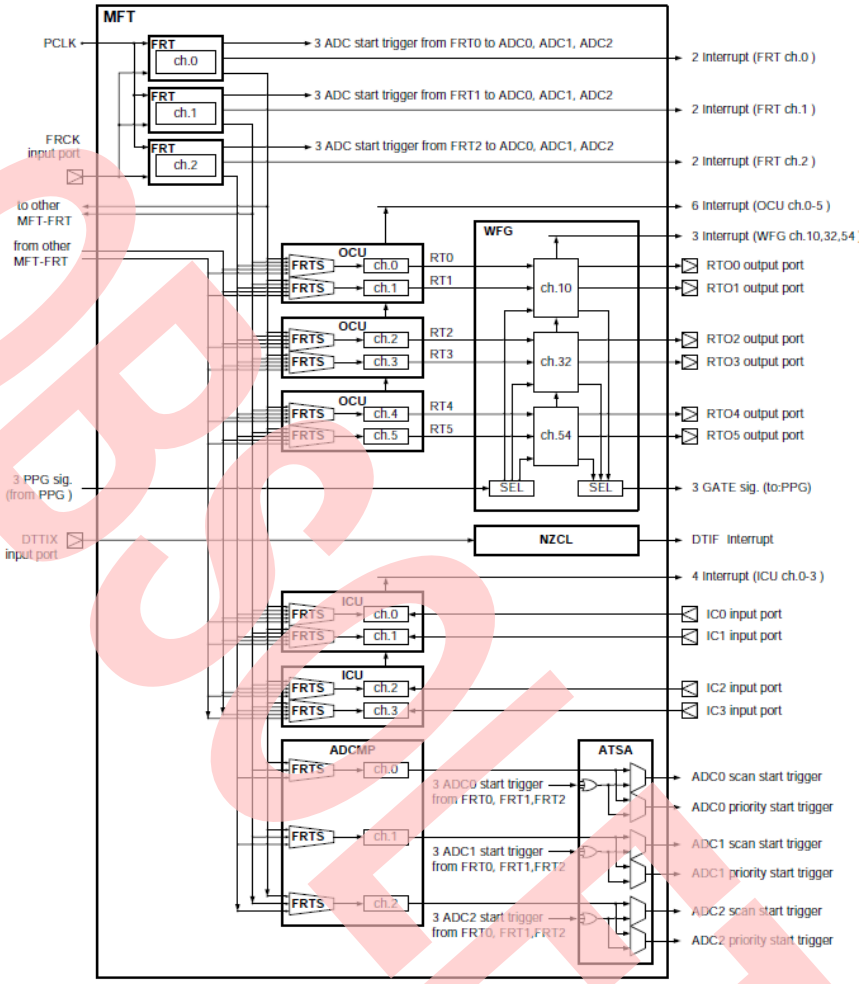
This Application-Note describes the usage of the Multifunction Timer (MFT) of the new Cypress FM3 ARM® Cortex™-M3 MCU (e.g. MB9BF506R). Depending on the device, there are up to three MFT units integrated in the device. This document gives a short overview of the features of this unit.

Each MFT consists of the following function blocks:

Free-run Timer unit (FRT):	3ch.
Output Compare unit (OCU):	6ch.
Waveform Generator unit (WFG)	3ch.
Noise Canceller unit (NZCL)	1ch.
Input Capture unit (ICU)	4ch.
ADC Start Compare unit (ADCMP)	3ch.
ADC Start Trigger Selector unit (ACCP)	3ch.

Because of the close alliance of the blocks, the MFT is not only suited for complex motion-control functionalities. It is also possible to use the functionality separately for time synchronized operation sequences.

Figure 1. Multifunction Timer



2 Parts of the Multifunction Timer

2.1 Free-run Timer (FRT)

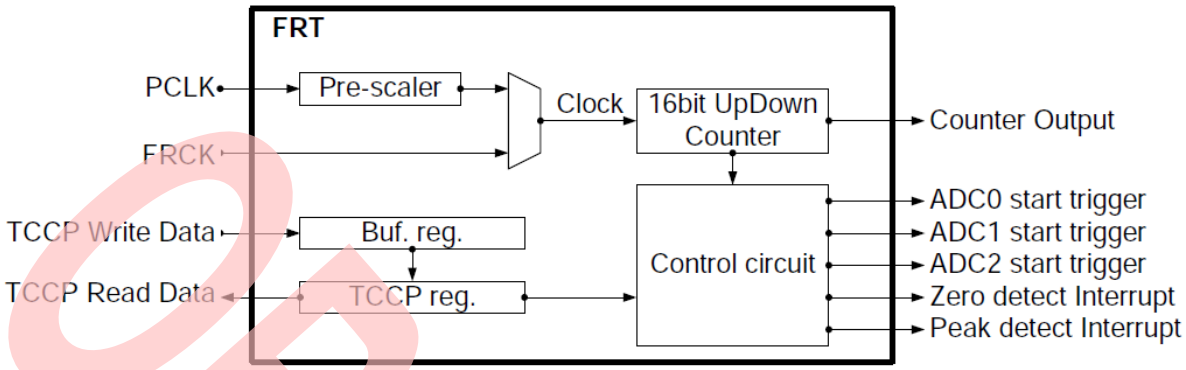
The Free-run timer is the clock-center of the MFT. All operations of the MFT are synchronized with this unit. The clock for the FRT is generated from the PCLK (Peripheral bus clock) or an external clock. The frequency of the PCLK depends on the bus-frequency of the peripheral (e.g.40 MHz at the MB9BFxxx series). The external clock must not exceed 20MHz.

This clock is used to trigger the internal 16bit counter. Depending on the mode of the timer, the counter performs up-count or up/down-count operation to a customized value (TCCP-value). Especially the up/down-counting functionality is used as time-base for center-aligned PWM generation. It is possible to update the TCCP-value by writing to a buffer-register. The written value will be updated after a complete cycle.

There is a control-circuit included which manages the start of the ADC-conversion at the zero-crossing of the TCCP-value. The control-circuit can also generate interrupts when reaching the top or the bottom of this value.

Each MFT consists of three separate units. It is possible to synchronize two MFT by selecting the FRT – signal from the other MFT.

Figure 2. Free-run Timer



Initialization Example FRT

```
// INIT FRT from MFT
FM3_MFT0_FRT->TCSA0 = 0x00b6;  // clock divider 64 (1.6us clock)
                               // up-down count mode
FM3_MFT0_FRT->TCSB0 = 0x0;     // no AD-Trigger from FRT
FM3_MFT0_FRT->TCCP0 = 0x1000;  // cycle time/2
```

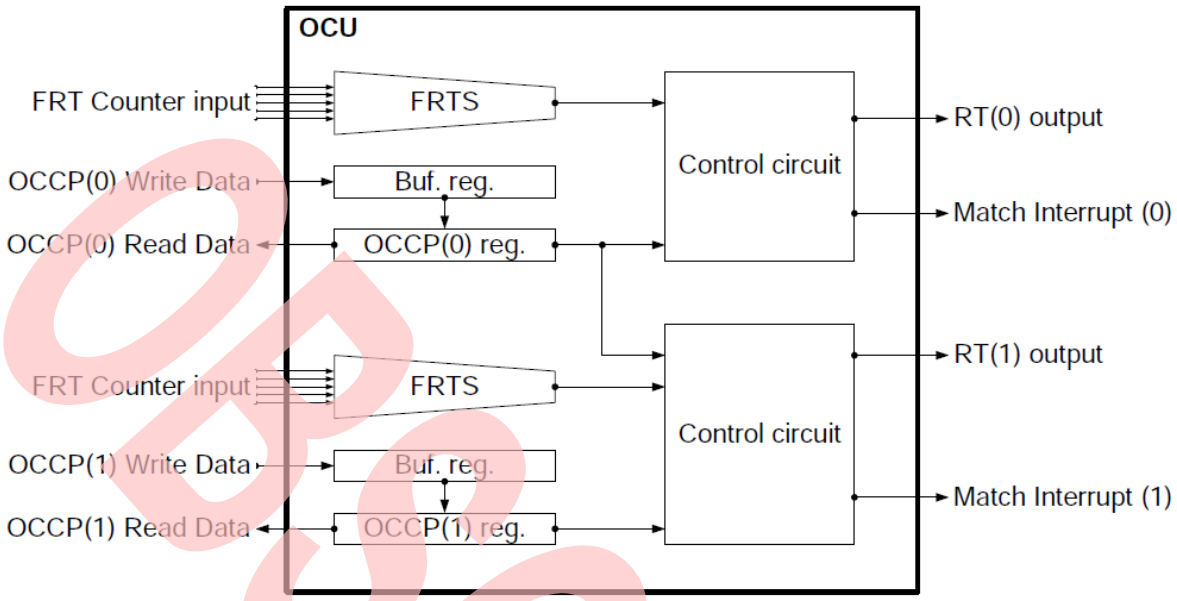
2.2 Compare unit (OCU)

The OCU generates and outputs PWM signals based on the counter value of the FRT. The OCU has five FRT inputs. Three inputs are from the FRT of the corresponding MFT module, two FRT inputs are routed from the other MFT. This enables the MFT to be synchronized using a single clock source.

The output of the OCU channel changes conditioned to the value of the FRT counter input. This action is triggered from the value of the OCCP-Register which can be updated every cycle. Depending on the count-mode of the FRT, there are also some different reactions possible. One example is the up/down-mode which triggers the output of the OCU on compare matches at up-direction, down-direction or up/down-direction of the count. The integrated control circuit is able to generate interrupts on compare-match of the count.

The OCU consists of three independent units with two channels per unit. The output of this unit is directly routed to the Waveform Generator.

Figure 3. Output Capture Unit

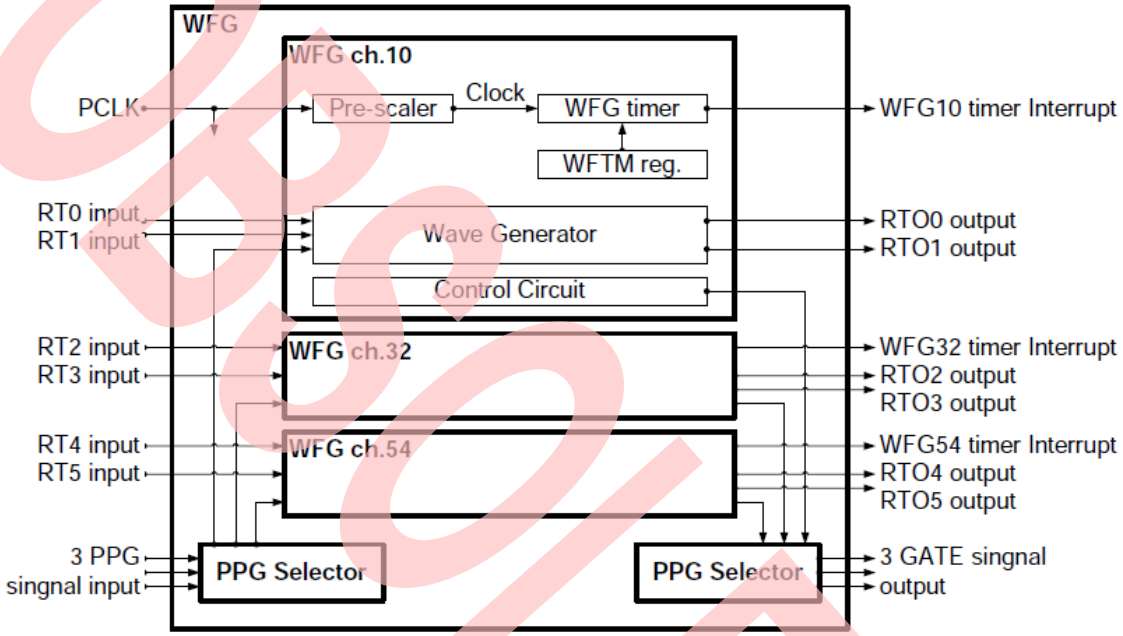



```
FM3_MFT0_OCU->OCFS10 = 0x0;     // Connects FRT0 to OCU
FM3_MFT0_OCU->OCSB10 = 0x0;     // Sets RT(0)to Low level @
OCSA.CST0=0
FM3_MFT0_OCU->OCSC = 0x3f;      // Up/Down-count mode, (Active High)
FM3_MFT0_OCU->OCCP0 = 0x100;    // Set to high/2 time, 1ms
FM3_MFT0_OCU->OCSA10 = 0x01;    // Enable OCU 0
```

2.3 Waveform Generator (WFG)

The WFG generates the RTO output. Depending on the WFG-mode, the WFG is able to bypass the signal from the OCU, superimpose a signal from the PPG with the signals from the OCU or generate signals using only the PPG. For this superimposition of the signal with a PPG signal the generation of a gate-signal is needed.

Figure 4. Waveform Generator



The WFG can react in different modes which affect the output signal:

1. Through mode
2. RT-PPG mode
3. Timer mode
4. RT dead timer mode
5. PPG dead timer mode

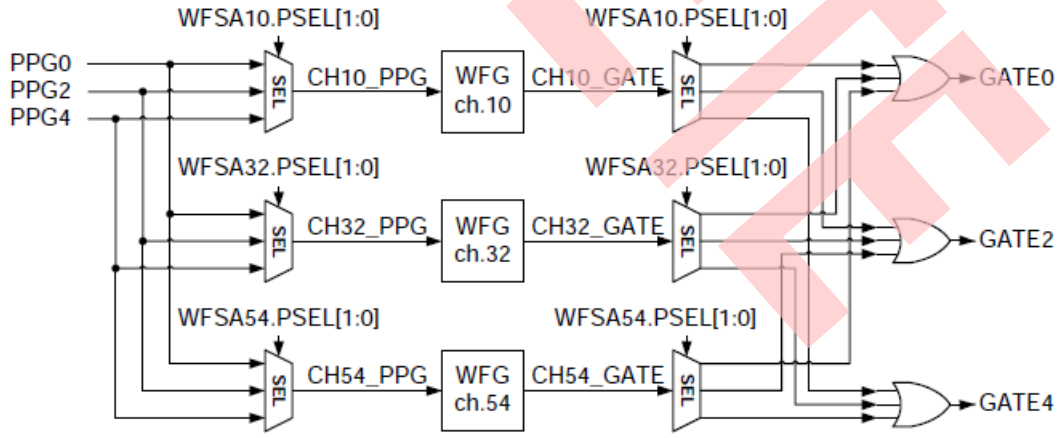
The explanation for the different modes is shown for WFG channel RT0. The other channels react in the same manner but are not mentioned in the software-examples!

2.3.1 Generation of the GATE-signal (e.g. CH10_Gate)

For the superimposition of the PPG-signal, a gate-signal is generated.

Operation Mode	WFSA. TMD[2:0]	WFSA. GTEN[1:0]	CH_GATE Signal Output
Through mode	000	don't care	Always outputs Low-level signals
RT-PPG mode	001	00	Always outputs Low-level signals
		01	Outputs RT(0) without change
		10	Outputs RT(1) without change
		11	Outputs High-level signals when either RT(1) or RT(0) signal is High-level Outputs Low-level signals when both RT(1) and RT(0) signals are Low-level
Timer-PPG mode	010	00	Always outputs Low-level signals
		01	Outputs WFG timer active flag0
		10	Outputs WFG timer active flag1
		11	Outputs High-level signals when either of WFG timer active flags is "1" Outputs Low-level signals when both of WFG timer active flags are "0"
RT dead timer mode	100	don't care	Always outputs Low-level signals
PPG dead timer mode	111	00	Always outputs Low-level signals
		01	Outputs RT(0) without change
		10	Outputs RT(1) without change
		11	Outputs High-level signals when either RT(1) or RT(0) signal is High-level Outputs Low-level signals when both RT(1) and RT(0) signals are Low-level

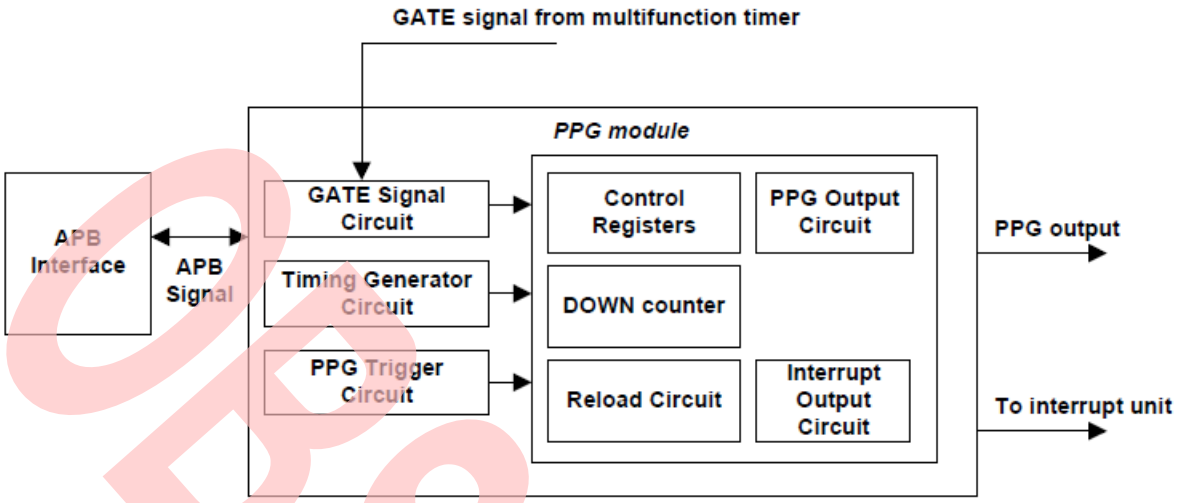
Figure 5. Generation of the Gate Signal



2.3.2 Generation of the PPG-Signal

The PPG is not included in the MFT - it is a separated peripheral of the MCU. The GATE-signal from the MFT gates the PPG-Signal.

Figure 6. Block diagram of the PPG



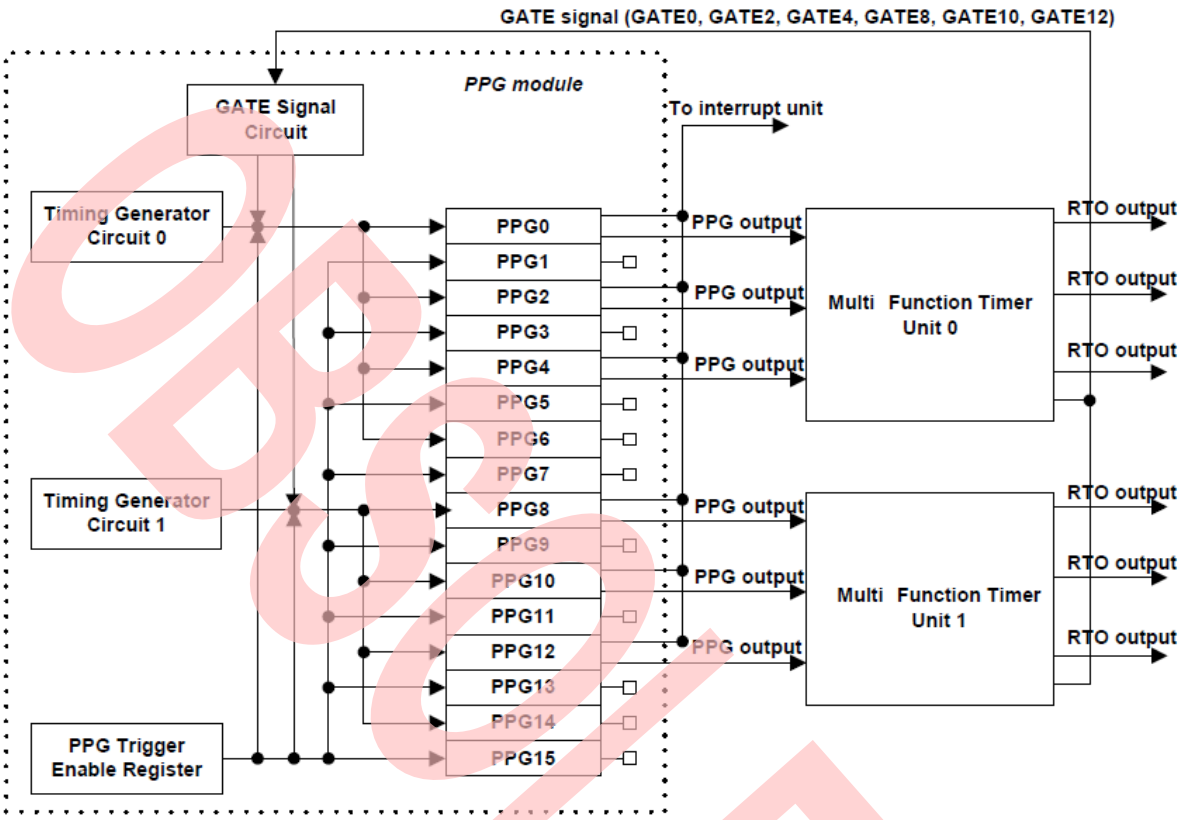

```
bFM3_GPIO_PFR3_PA = 0x1;          // USE Function output
FM3_GPIO->EPFR01 = 0x01;          // Use Pin 19 on SK - FR3 - 100PMC

FM3_MFT0_WFG->WFSA10 = 0x0c00; // Bypass of the WFG, output PPG-
signal
// Init of the PPG
FM3_MFT_PPG->COMP0 = 0xf;         // Set compare-value to 0xf
FM3_MFT_PPG->REVC = 0x0;          // Don't reverse the output
FM3_MFT_PPG->PPGC0 = 0x0;         // No interrupt generation, 8 bit
FM3_MFT_PPG->PRLL0 = 0xe;         // Set the Low width of PPG
FM3_MFT_PPG->PRLH0 = 0xe;         // Set the High width of PPG
FM3_MFT_PPG->GATEC0 = 0x0;        // Start by TRG-Bit, Start low level

FM3_MFT_PPG->TTCR0 = 0x0001;      // Uses PCLK/2, Start Counting
FM3_MFT_PPG->TRG = 0x1;           // Starts PPG 0
```

The complete example is available on the webpage: mb9bfxxx_ppg_mft-v10.zip

PPG connection to the WFG

For example the MB9BF506R includes 16 PPGs and two separate MFT. This figure shows the connection of the PPG to the MFT.

Figure 7. Connection of the PPG to the MFT



2.3.3 Modes of the WFG

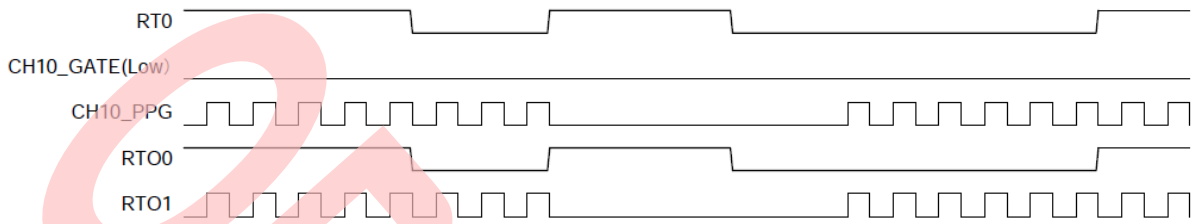
The following table shows the different operation-modes of the WFG.

Operation Mode	WFSA. TMD [2:0]	WFSA. PGEN [1:0]	WFSA. DMOD	Output of RTO(1) Signal	Output of RTO(0) Signal
Through mode	000	00	don't care	Outputs RT(1) signal through	Outputs RT(0) signal through
		01		Outputs RT(1) signal through	Outputs CH_PPG signal through
		10		Outputs CH_PPG signal through	Outputs RT(0) signal through
		11		Outputs CH_PPG signal through	Outputs CH_PPG signal through
RT-PPG mode	001	00	don't care	Outputs RT(1) signal through	Outputs RT(0) signal through
		01		Outputs RT(1) signal through	(*A) Outputs Low-level signals when RT(0) is Low-level Outputs CH_PPG signal when RT(0) signal is High-level
		10		(*B) Outputs Low-level signals when RT(1) signal is Low-level Outputs CH_PPG signal when RT(1) signal is High-level	Outputs RT(0) signal through
		11		Same as *B	Same as *A
Timer-PPG mode	010	00	don't care	(*D) Outputs Low-level signals when WFG timer active flag1 is "0" Outputs High-level signals when WFG timer active flag1 is "1"	(*C) Outputs Low-level signals when WFG timer active flag0 is "0" Outputs High-level signals when WFG timer active flag0 is "1"
		01		Same as *D	(*E) Outputs Low-level signals when WFG timer active flag0 is "0" Outputs CH_PPG signal when WFG timer active flag0 is "1"
		10		(*F) Outputs Low-level signals when WFG timer active flag1 is "0" Outputs CH_PPG signal when WFG timer active flag1 is "1"	Same as *C
		11		Same as *F	Same as *E
RT RT dead timer mode	100	don't care	0	Starts WFG timer at the rising and falling edges of the RT(1) signal and generates the non-overlap signal. Outputs the generated non-overlap signal with normal polarity (Active High)	
			1	Starts WFG timer at the rising and falling edges of the RT(1) signal and generates the non-overlap signal. Outputs the generated non-overlap signal with reversed polarity (Active Low)	
PPG dead timer mode	111	don't care	0	Starts WFG timer at the rising and falling edges of the CH_PPG signal and generates the non-overlap signal. Outputs the generated non-overlap signal with normal polarity (Active High)	
			1	Starts WFG timer at the rising and falling edges of the CH_PPG signal and generates the non-overlap signal. Outputs the generated non-overlap signal with reversed polarity (Active Low)	

WFG - Through mode

The signals were not modified in the through-mode. It is possible to choose between the CH10_PPG-signal and the RTO-signal for the RTO 0/1 output. In Figure 8 you see an example of the through-mode. The RT0 input is routed to the output RTO0, the CH10_PPG is routed to the RTO1 output of the MCU.

Figure 8. WFG - Trough mode

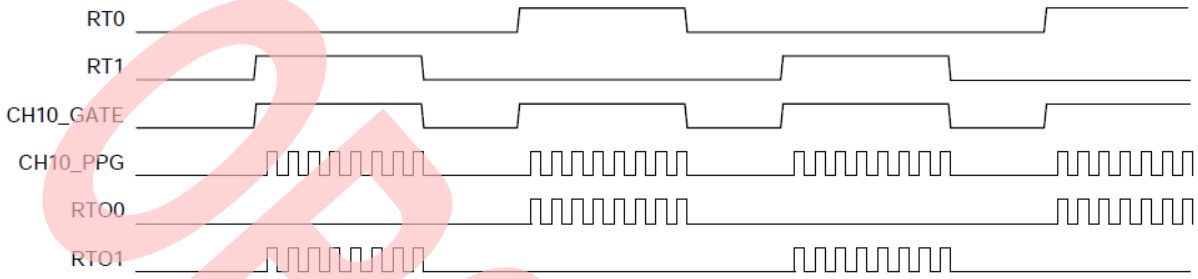



```
bFM3_GPIO_PFR3_PA = 0x1;        // USE Function output
FM3_GPIO->EPFR01 = 0x01;        // Use Pin 19 on SK-FR3-100PMC, Port
P3A
// INIT FRT from MFT
FM3_MFT0_FRT->TCSA0 = 0x00b6;   // up - down count mode
FM3_MFT0_FRT->TCSB0 = 0x0;      // no generation of AD - Trigger from
FRT
FM3_MFT0_FRT->TCCP0 = 0x80;     // cycle time/2
// INIT OCU
FM3_MFT0_OCU->OCFS10 = 0x0;     // Connects FRT0 to OCU
FM3_MFT0_OCU->OCSB10 = 0x0;     // Buffer transfer at zero value
FM3_MFT0_OCU->OCSC = 0x3f;      // Up/Down-count mode, (Active High)
FM3_MFT0_OCU->OCCP0 = 0x40;     // Set to high/2 time
FM3_MFT0_OCU->OCSA10 = 0x01;    // Enable OCU 0
// INIT WFG in Through mode
FM3_MFT0_WFG->WFSA10 = 0x0002; // Bypass of the WFG,
                                // RT00=RT0, RTO1=CH10_PPG
```

WFG - RT-PPG mode

The output of the OCU (RT0, RT1) is superimposed with the PPG-Signal. The PPG-signal is generated externally from the PPG-unit with the influence of the Gate-signal.

Figure 9. WFG - RT-PPG mode



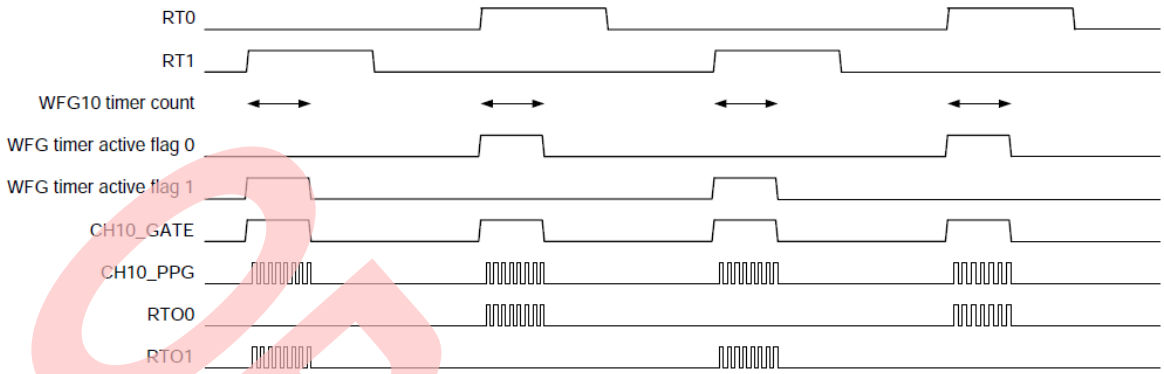

```
bFM3_GPIO_PFR3_PA = 0x1;        // USE Function output
FM3_GPIO->EPFR01 = 0x01;        // Use Pin 19 on SK-FR3-100PMC, Port P3A
// INIT FRT from MFT
FM3_MFT0_FRT->TCSA0 = 0x00b6; // up - down count mode
FM3_MFT0_FRT->TCSB0 = 0x0;      // no generation of AD - Trigger from FRT
FM3_MFT0_FRT->TCCP0 = 0x80;     // cycle time/2
// INIT OCU
FM3_MFT0_OCU->OCFS10 = 0x0;     // Connects FRT0 to OCU
FM3_MFT0_OCU->OCSB10 = 0x0;     // Buffer transfer at zero value
FM3_MFT0_OCU->OCSC = 0x3f;      // Up/Down-count mode, (Active High)
FM3_MFT0_OCU->OCCP0 = 0x40;     // Set to high/2 time
FM3_MFT0_OCU->OCSA10 = 0x01;    // Enable OCU 0
// Init of the PPG
FM3_MFT_PPG->COMP0 = 0xff;      // Set compare-value to 0xff
FM3_MFT_PPG->REVC = 0x0;        // Don't reverse the output
FM3_MFT_PPG->PPGC0 = 0x0;       // No interrupt generation, 8 bit
operation
FM3_MFT_PPG->PRLL0 = 0xfe;      // Set the Low width of PPG
FM3_MFT_PPG->PRLH0 = 0xfe;      // Set the High width of PPG
FM3_MFT_PPG->GATEC0 = 0x22;     // Start by Gate-signal, Start low level
FM3_MFT_PPG->TTCR0 = 0xfd;      // Uses PCLK/64, Start Counting
FM3_MFT_PPG->TRG = 0x1;         // Starts PPG 0
// INIT WFG
FM3_MFT0_WFG->WFSA10 = 0x0cc8;// Count clock=PCLK, RT-PPG-Mode
                                // generation of GATE-signal PPG0
```

The complete example is available on the webpage: mb9bfxxx_mft_wfg_rt_ppg-v10

WFG - Timer mode

The WFG-Timer mode uses the RT0 and RT1 signals to start a timer inside of the WFG. This timer is used to generate the WFG active flags which act as Gate-signals. The output of the WFG is a superimposition of the WFG timer active flag and the PPG.

Figure 10. WFG - Timer mode



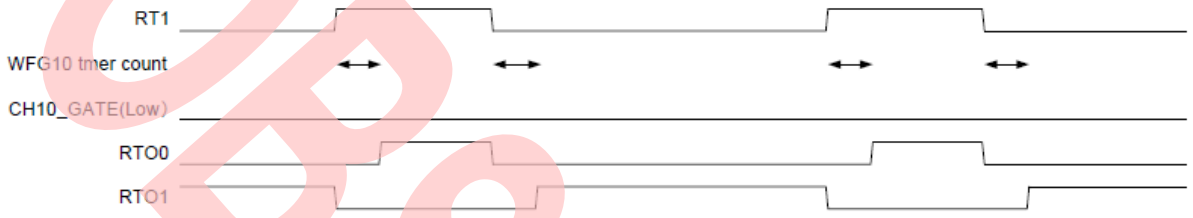

```
bFM3_GPIO_PFR3_PA = 0x1;        // USE Function output
FM3_GPIO->EPFR01 = 0x01;        // Use Pin 19 on SK - FR3 - 100PMC
// INIT FRT from MFT
FM3_MFT0_FRT->TCSA0 = 0x00b6; // up - down count mode
FM3_MFT0_FRT->TCSB0 = 0x0;    // no generation of AD - Trigger from FRT
FM3_MFT0_FRT->TCCP0 = 0x80;   // cycle time/2
// INIT OCU
FM3_MFT0_OCU->OCFS10 = 0x0;   // Connects FRT0 to OCU
FM3_MFT0_OCU->OCSB10 = 0x0;   // Buffer transfer at zero value
FM3_MFT0_OCU->OCSC = 0x3f;    // Up/Down-count mode, (Active High)
FM3_MFT0_OCU->OCCP0 = 0x40;   // Set to high/2 time
FM3_MFT0_OCU->OCSA10 = 0x01;  // Enable OCU 0
// Init of the PPG
FM3_MFT_PPG->COMP0 = 0xff;    // Set compare-value to 0xff
FM3_MFT_PPG->REVC = 0x0;      // Don't reverse the output
FM3_MFT_PPG->PPGC0 = 0x1;     // 8 bit operation, Uses timing generator
FM3_MFT_PPG->PRLL0 = 0xf;     // Set the Low width of PPG
FM3_MFT_PPG->PRLH0 = 0xf;     // Set the High width of PPG
FM3_MFT_PPG->GATEC0 = 0x22;   // Start by Gate-signal, Start low level
FM3_MFT_PPG->TTCR0 = 0xfd;    // Uses PCLK/64, Start Counting
// INIT WFG
FM3_MFT0_WFG->WFSA10 = 0x0cd0;// Count clock=PCLK, Timer-Mode,
                              // generation of GATE-signal, PPG0
FM3_MFT0_WFG->WFTM10 = 0x500; // Set the WFG-Timer (PCKL is is used)
```

The complete example is available on the webpage: mb9bfxxx_mft_wfg_timer-v10

WFG - RT dead timer mode

The RT-dead timer mode uses only the RT1 signal from the OCU. When the rising edge of the RT1 is detected, the output of the RTO1 signal is set to the low level and the WFG timer starts. After the WFG timer elapses, the RTO0 signal is set to the high level. When the falling edge of the RT1 is detected, the output of the RTO0 signal is set to the low level and WFG timer starts. After the WFG timer elapses, the RTO1 signal is set to the high level.

Figure 11. WFG - RT dead timer mode




```
bFM3_GPIO_PFR3_PA = 0x1;       // USE Function output
bFM3_GPIO_PFR3_PB = 0x1;       // Use Function Output
FM3_GPIO->EPFR01 = 0x05;       // Use Pin 19 and 20 on SK - FR3 - 100PMC
// INIT FRT from MFT
FM3_MFT0_FRT->TCSA0 = 0x00b6; // up - down count mode
FM3_MFT0_FRT->TCSB0 = 0x0;     // no generation of AD - Trigger from FRT
FM3_MFT0_FRT->TCCP0 = 0x80;    // cycle time/2
// INIT OCU
FM3_MFT0_OCU->OCFS10 = 0x0;    // Connects FRT0/1 to OCU
FM3_MFT0_OCU->OCSB10 = 0x0;    // Buffer transfer at zero value
FM3_MFT0_OCU->OCSC = 0x3f;     // Up/Down-count mode, (Active High)
FM3_MFT0_OCU->OCCP1 = 0x40;    // Set to high/2 time
FM3_MFT0_OCU->OCSA10 = 0x02;   // Enable OCU 1
// INIT WFG
FM3_MFT0_WFG->WFSA10 = 0x0020;// Count clock=PCLK, Dead-Timer-Mode
                               // no generation of GATE-signal
FM3_MFT0_WFG->WFTM10 = 0x500; // Set the WFG-Timer (PCKL is is used)
```

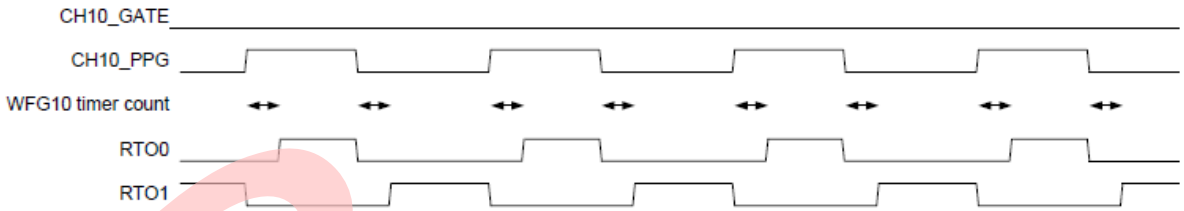
The complete example is available on the webpage: mb9bfxxx_mft_wfg_dead_timer-v10

WFG - PPG dead timer mode

The PPG dead timer mode uses only the PPG – Signal for the generation of the RTO0 and

RTO1 signals. When the rising edge of the CH10_PPG is detected, the output of the RTO1 signal is set to the low level and the WFG timer starts. After the WFG timer elapses, the RTO0 signal is set to the high level. When the falling edge of the CH10_PPG is detected, the output of the RTO0 signal is set to the low level and WFG timer starts. After the WFG elapses, the RTO1 signal is set to the high level.

Figure 12. WFG - PPG dead time mode



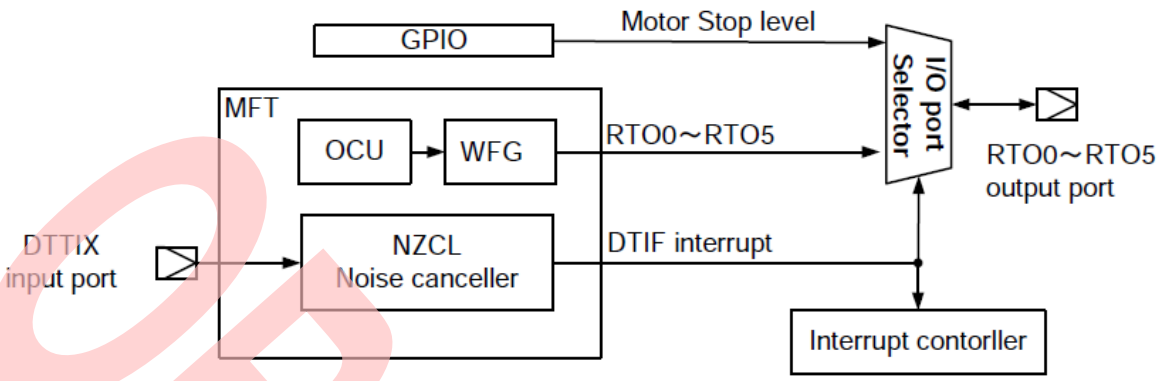

```
bFM3_GPIO_PFR3_PA = 0x1;        // USE Function output
bFM3_GPIO_PFR3_PB = 0x1;        // Use Function Output
FM3_GPIO->EPFR01 = 0x05;        // Use Pin 19 and 20 on SK - FR3 - 100PMC
// Init of the PPG
FM3_MFT_PPG->COMP0 = 0xf;       // Set compare-value to 0xf
FM3_MFT_PPG->REVC = 0x0;        // Don't reverse the output
FM3_MFT_PPG->PPGC0 = 0x1;       // No interrupt generation, 8bit operation
                                // start by timing generator
FM3_MFT_PPG->PRLL0 = 0xe;       // Set the Low width of PPG
FM3_MFT_PPG->PRLH0 = 0xe;       // Set the High width of PPG
FM3_MFT_PPG->GATEC0 = 0x22;     // Start by Gate-signal, Start low level
FM3_MFT_PPG->TTCR0 = 0x00f3;    // Uses PCLK/2, Start Counting
// INIT WFG
FM3_MFT0_WFG->WFSA10 = 0x0038;// WFG in PPG dead timer mode
FM3_MFT0_WFG->WFTM10 = 0x5;    // Set the WFG-Timer (PCKL is is used)
```

The complete example is available on the webpage: mb9bfxxx_mft_wfg_ppg_dead_time-v10

2.4 Noise Canceller unit (NZCL)

With the DTTIX – Input it is possible to realize emergency – stop of the RTO-Outputs. The external input-signal is filtered to prevent wrong trigger. After trigger the output is set to the predefined level of the GPIO Port. Depending on the configuration the level is high, low or tri-state. This enables the MCU to react very fast to external events. Additionally to this function an interrupt is generated.

Figure 13. Noise Canceller unit (NZCL)



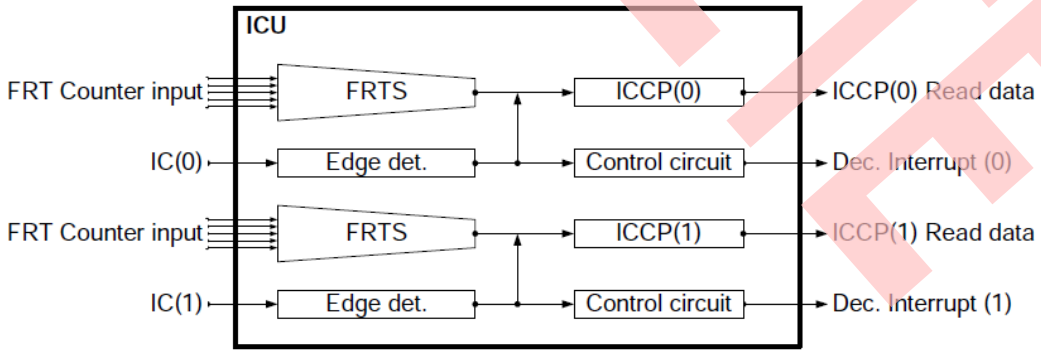

```
  bFM3_GPIO->PFR3_P9 = 0x1;          // Use function input
  FM3_GPIO->EPFR01 |= 0x1000;        // Use DTTI0X_0
  FM3_MFT0->NZCL = 0x0009;           // External Fault detect, 32clk
noise
```

2.5 Input Capture unit (ICU)

The ICU is used to capture external events for the generation of an interrupt or to count the time between two events. For the time base it is possible to select the three FRT from this MFT module or two external from another MFT module. The level of this event is adjustable from rising or falling edge. The value of the counted data can be read trough the ICCP – register. It is also possible to use this unit for encoder-switches to up-down counting a value.

Each MFT has two modules with each two units included.

Figure 14. Input Capture unit (ICU)



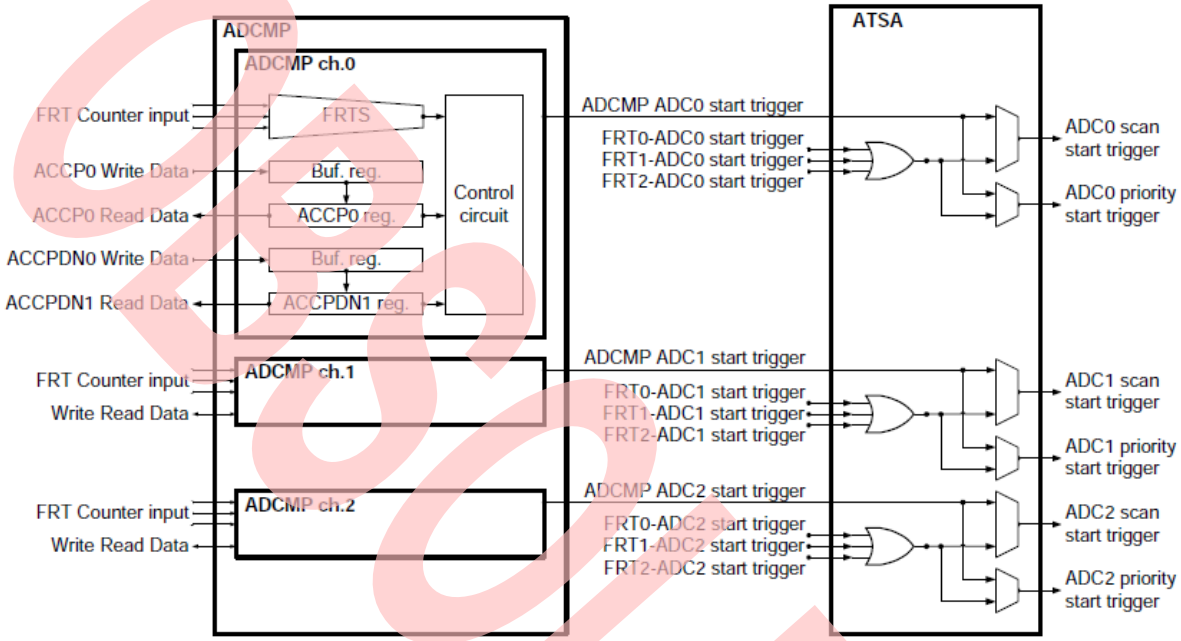
An example for the usage of the ICU is available on the webpage:

mb9bfxxx_mft_icu_irq_freqcnt-v10

2.6 ADC Start Compare unit (ADCMP), ADC Start Trigger Selector unit (ACCP)

The ADC Start Compare unit is used to trigger the ADC in a defined time schedule. The unit uses one of the three integrated FRT counters for the correct time synchronization. The value for the trigger can be set in the ACCP register. The ATSA-unit selects the trigger-source from the ADCMP-unit or directly from the FRT. The unit is able to perform normal scan triggers and also priority triggers.

Figure 15. ADC Start Compare unit (ADCMP), ADC Start Trigger Selector unit (ACCP)




```
FM3_MFT0_ADCMP->ACCP0 = VAL; // trigger ADC0+1
       FM3_MFT0_ADCMP->ACCP1 = VAL;
       FM3_MFT0_ADCMP->ATSA=0x0005; // Trigger ADC0+1 by ADTRG unit
FM3_MFT0_ADCMP->ACSA=0x0005; // Enables ADCMP ch.0.
                                //Connects FRT ch.0 to ADCMP ch.0.
```

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	CHRH	04/29/2011	Initial release.
			06/17/2011	Review of the document.
*A	5053167	CHRH	12/17/2015	Updated to Cypress template.
*B	5835056	AESATP12	07/27/2017	Updated logo and copyright.
*C	6415017	CHRH	12/20/2018	Obsolete document. Completing Sunset Review.

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