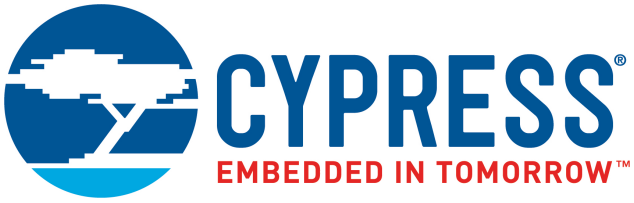
Please note that Cypress is an Infineon Technologies Company.
The document following this cover page is marked as “Cypress” document as this is the company that originally developed the product. Please note that Infineon will continue to offer the product to new and existing customers as part of the Infineon product portfolio.

Continuity of document content
The fact that Infineon offers the following product as part of the Infineon product portfolio does not lead to any changes to this document. Future revisions will occur when appropriate, and any changes will be set out on the document history page.

Continuity of ordering part numbers
Infineon continues to support existing part numbers. Please continue to use the ordering part numbers listed in the datasheet for ordering.



THIS SPEC IS OBSOLETE

Spec No: 002-04877

Spec Title: AN204877 - FM3 MB9BFXXX SERIES, HARDWARE SET UP

Replaced by: None

AN204877

FM3 MB9BFXXX Series, Hardware Set Up

This application note describes how to set up a hardware environment for Cypress ARM® Cortex®-M3 (FM3) MCUs. As an example the MB9BF50xN MCU is used.

Contents

1 Introduction 1
2 Minimum System 1
2.1 Schematic (RS232 Programming) 1
2.2 Schematic (USB Programming) 2
2.3 Power supply 3
2.4 Analog Digital Converter Supply Pins 3
2.5 Analog Input Pins 3
2.6 Reset/Init Pin (INITX) 4
2.7 C Pin 4
2.8 Clock Source 4
2.9 Mode Pins 4
2.10 NC Pins 4
3 Layout and Electromagnetic Compatibility 4
3.1 General 4
3.2 Power Line Routing 5
3.3 C Pin Decoupling 5
3.4 Power Supply Decoupling 6
3.5 Quartz Crystal Placement and Signal Routing 8
3.6 Other documents 8
3.7 Resonator/Crystal IC matcher 8
3.8 MCU Pin Summary 9
4 Port Input / Unused Pins / Latch-up 9
4.1 Port Input / Unused Digital I/O Pins 9
4.2 Latch-up consideration (switch) 10
5 JTAG Connection 14
5.1 JTAG/SWD 14
5.2 ETM Trace Port 15
Document History 16
Worldwide Sales and Design Support 17
Products 17
PSoC® Solutions 17
Cypress Developer Community 17
Technical Support 17

OBSOLETE

1 Introduction

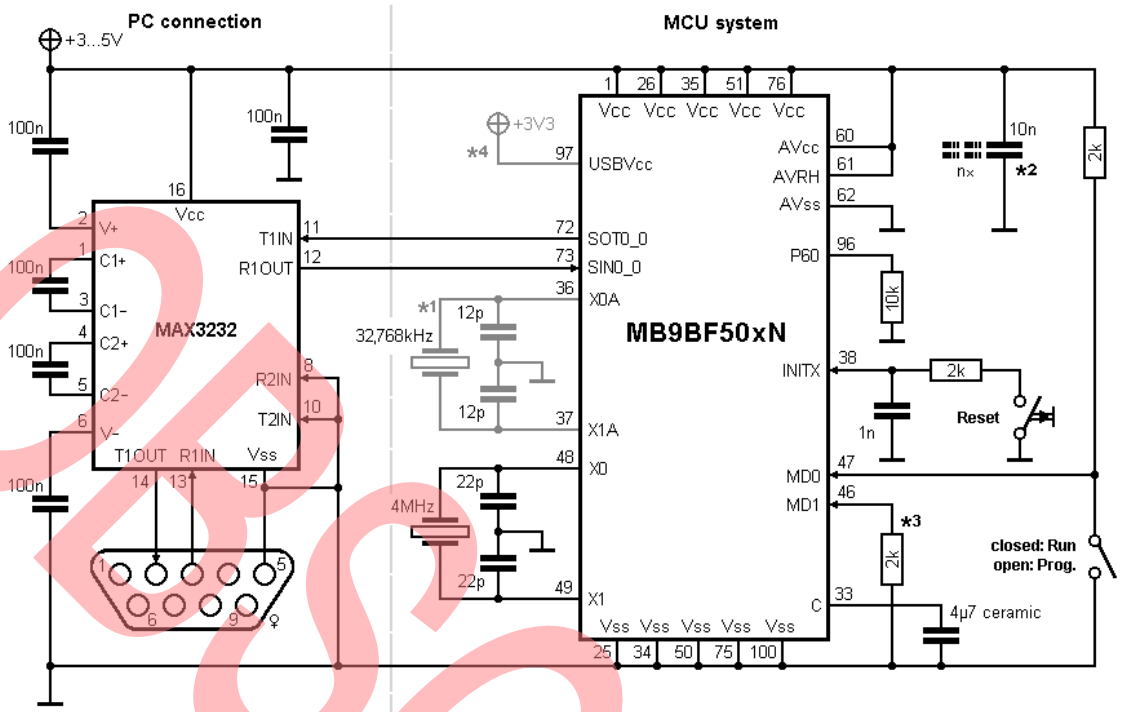
This application note describes how to set up a hardware environment for Cypress ARM® Cortex®-M3 (FM3) MCUs. As an example the MB9BF50xN MCU is used.

2 Minimum System

This chapter gives an example of a minimum hardware system.

2.1 Schematic (RS232 Programming)

The following graphic shows a schematic of a minimum hardware system, which uses the UART asynchronous channel for Flash programming. Note that for other MCU families a different pinning is needed.



*1 only needed if sub clock necessary

*2 please refer to Chapter 3

*3 If PCB has good EMI routing, resistors can be 0Ω for mode pins

*4 If USB UDPn and UDMn ports are used for USB, connect USBVcc to 3.3 V, if UDPn and UDMn are used as GPIO, connect USBVcc to Vcc

2.1.1 Serial Interface

The “PC connection” section is only needed, if no 3...5V external serial data lines for Programming are existing. The MAX3232 is a standard level shifter, which converts the 3...5V levels of the MCU to ±12V RS232V24 levels and vice versa.

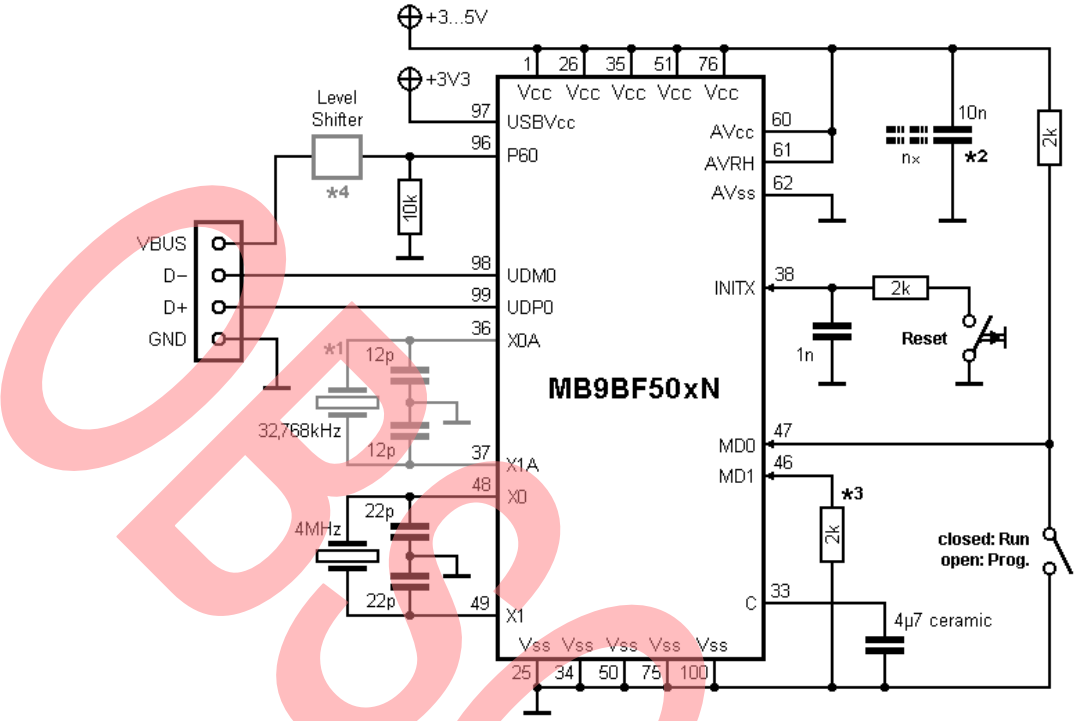
Please consider, that the internal charge pumps of the level shifter can produce noise on the +3…5 Volts line, which can influence the ADC, if AVcc and AVRH are directly (unfiltered) Connected to it.

Consider that the logic level at Port P60 determines UART or USB programming. If the port Is not used in the user’s application and USB programming is not needed, it can also directly Connected to GND (considering good EMI routing). Do not switch this port to output mode in this case!

2.2 Schematic (USB Programming)

The following graphic shows a schematic of a minimum hardware system, which uses the USB function for Flash programming. Note that for other MCU families a different pinning is needed.

OBSOLETE



*1 only needed if sub clock necessary

*2 please refer to chapter 3

*3 If PCB has good EMI routing, resistors can be 0Ω for mode pins

*4 Provide Level shifter from VBUS (+5 Volts) to MCU-Vcc, if MCU- Vcc is different from +5 Volts

2.2.1 USB Interface

The MCU can be supplied either by external power or by VBUS connection to the USB host. In any case, for USBVcc +3.3 Volts are needed. Use an 3.3V-regulator for USBVcc, if VBUS is used for powering the MCU.

Please consider, that the internal charge pumps of the level shifter can produce noise on the +3...5 Volts line, which can influence the ADC, if AVcc and AVRH are directly (unfiltered) connected to it.

2.3 Power supply

The power supply should be from 2.7 Volts to 5.5 Volts for normal usage depending on the used FM3 series. Refer to the datasheet for maximum and minimum power supply voltages. In any case provide 3.3 Volts to USBVcc, if USB functionality is needed. USBVcc can be connected to Vcc, if the USB data ports (USDMn, USDPn) only used as digital I/O ports.

2.4 Analog Digital Converter Supply Pins

The analog converter supply pins (AVcc, AVss, and AVRH) should be connected even if the ADC of the MCU is not used to avoid latch-up conditions on the analog pins even if they are switch to digital input.

2.5 Analog Input Pins

Because the ADC works with an internal sample capacitor the input impedance and external capacity must be low. Refer to the corresponding datasheet, ADC electrical characteristics chapter for recommended impedance and capacity.

OBSOLETE

2.6 Reset/Init Pin (INITX)

To reset the MCU a switch connects this pin to Vss (GND). Additionally a capacitor has to be connected between Vss and the INITX pin for debouncing the switch and for EMI protection. From experience Cypress recommend a capacity of not more than 1 nF. This capacity covers the most common frequency protection in a wide range. Higher capacities and high impedance may cause latch-up effects together with an RSTX-Switch and low EMI protection.

2.7 C Pin

A 1...10µF ceramic capacitor (dielectric X7R, e. g. 4, 7µF) *must* be connected close to the C pin of the MCU. Otherwise the MCU may not operate correct or will be damaged in worst case. Also see chapter 3.

2.8 Clock Source

A clock source should be provided to the MCU. Therefore crystals or external clock signals can be used. For external source pin X0 (X0A) is used whereby pin X1 (X1A) is not connected.

Also refer to the chapter *Handling Devices* in the corresponding datasheet for details.

2.9 Mode Pins

The mode pins signalize the MCU the current operation mode. They should be pulled-up with 2k resistors. If the PCB routing protects ESD and EMI influence, the mode pins can be connected directly to Vcc and Vss (GND) depending on needed logic level. See chapter 4 for details.

The following settings are used for the both modes mentioned above:

2.9.1 Flash-(A) synchronous-Serial-Programming-Mode

MD0	MD1	P60
1	0	0

2.9.2 Flash-(A) synchronous-USB-Programming-Mode

MD0	MD1	P60
1	0	1

2.9.3 Run Mode

MD0	MD1	P60
0	0	Don't care

2.10 NC Pins

Do not leave input pins open. If not possible, switch pin to output.

Read Chapter4 for how to proceed with unused (not connected) pins.

3 Layout and Electromagnetic Compatibility

This chapter gives some tips for layout design

3.1 General

To avoid ESD problems and noise emission of the system some rules for the layout design has to be observed.

The most critical point is the C pin because this is the connection to the internal 1.2 V supply for the MCU core. Thus the two decoupling capacitors have to be placed very near to this pin.

Also the ground and Vcc routing has to be done carefully. Vcc lines should be routed in star shape. We recommend a Vss ground plane *on the mounting side* just under the MCU. For both Vcc and Vss only *one* connection to the rest of the circuit should be done, otherwise noise is carried-over from and to the MCU. Decoupling capacitors (DeCaps) have to be placed as nearest as possible to the related pins. If they are placed too far away their function becomes useless.

OBSOLETE

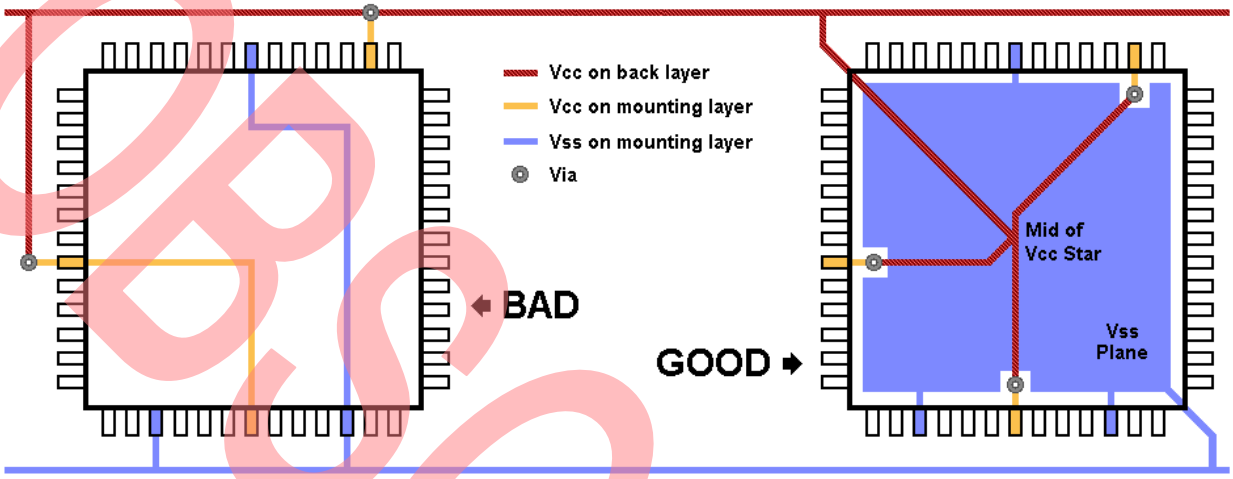
If crystals are used, they have to be placed as nearest as possible to the Xn(A) pins.

If possible all decoupling capacitors should be placed on the same mounting side as the MCU.

3.2 Power Line Routing

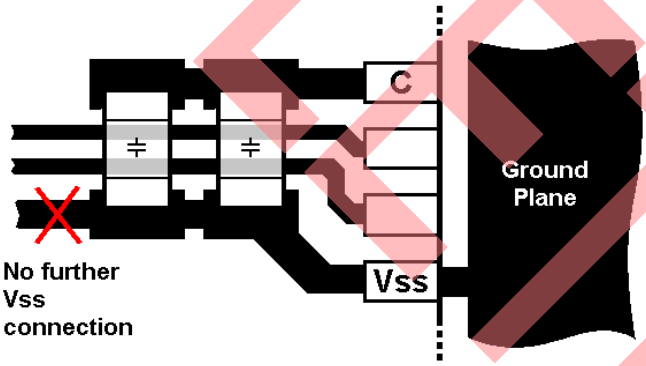
In general the Vcc and Vss lines should not be routed in “chains”, but in “star shape”. For Vss a ground plane is recommended which covers the chip package, and is connected in *one* point to Vss of the whole circuit.

Below is a example of a bad and a good power line routing:



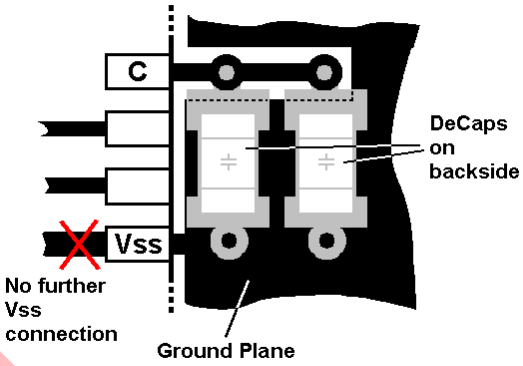
3.3 C Pin Decoupling

The following routing and placement for single sided metal layer is recommended (Note, that in all following illustrations the mounting metal layer is drawn in black and the back side metal layer in gray):



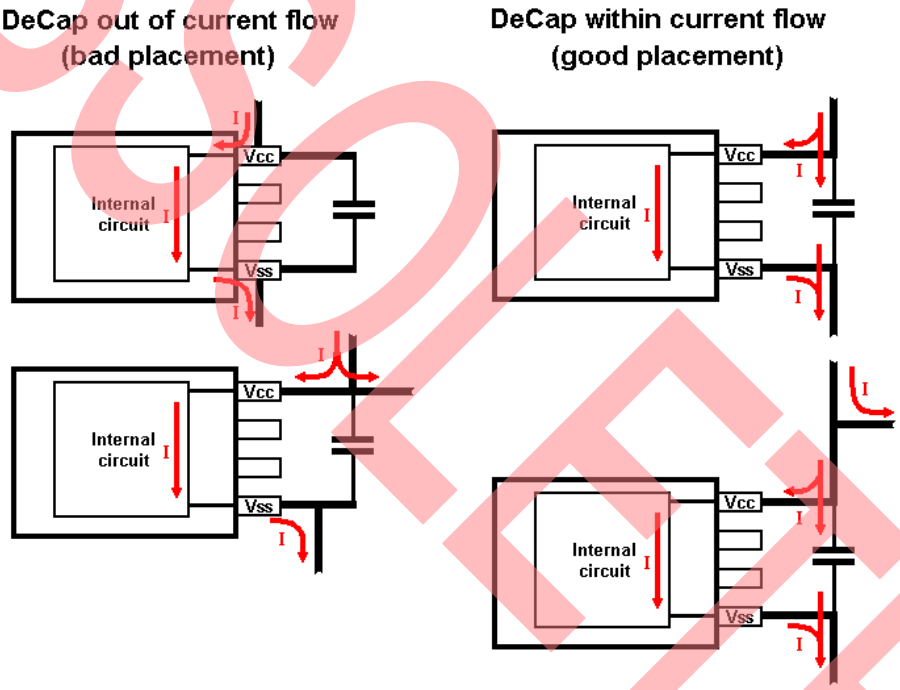
The following routing and placement for double sided metal layer is recommended. Note that despite the capacitors are placed on the opposite side as the MCU, this solution is the best.

OBSOLETE



3.4 Power Supply Decoupling

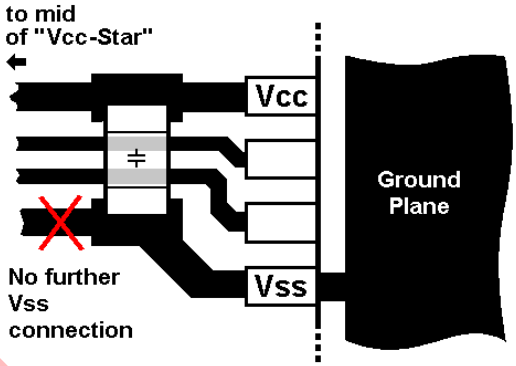
DeCaps for power supply have to be placed within the “current flow”. Otherwise they are senseless, because then their function become inoperable. The following graphic illustrates this:



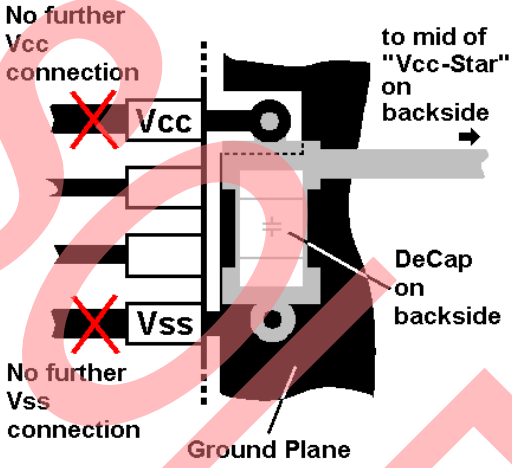
For EMI reasons all decoupling capacitors should have the same capacitance, so that all have a common resonance frequency. Cypress recommends 10nF (~100 MHz resonance) to 100nF (~10 MHz resonance) depending on application. For further detailed information please refer to the application note *16bit-EMC-Guideline* which is also valid for 32 bit MCUs.

The following routing and placement for single sided metal layer is recommended:

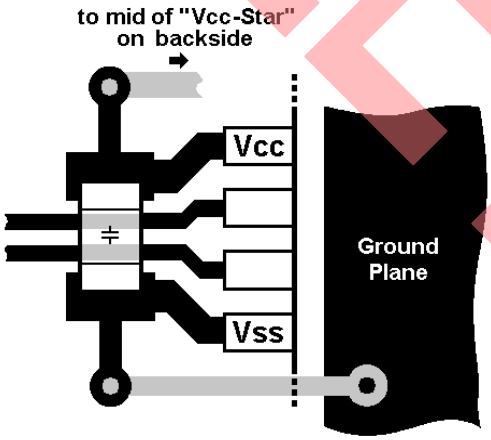
OBSOLETE



The following routing and placement for double sided metal layer is recommended. Note that despite the capacitor is placed on the opposite side as the MCU, this solution is the best like for the C pin.



If mounting on both sides is not possible the following placement and routing is recommended:

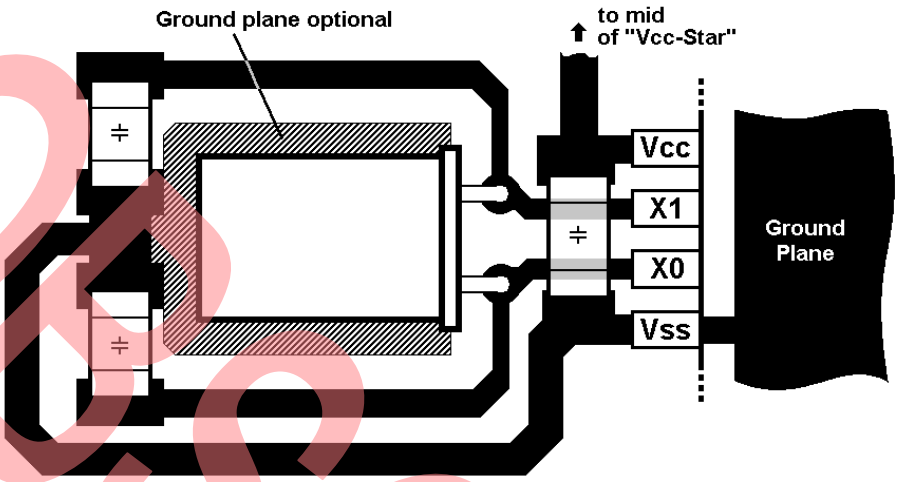


OBSOLETE

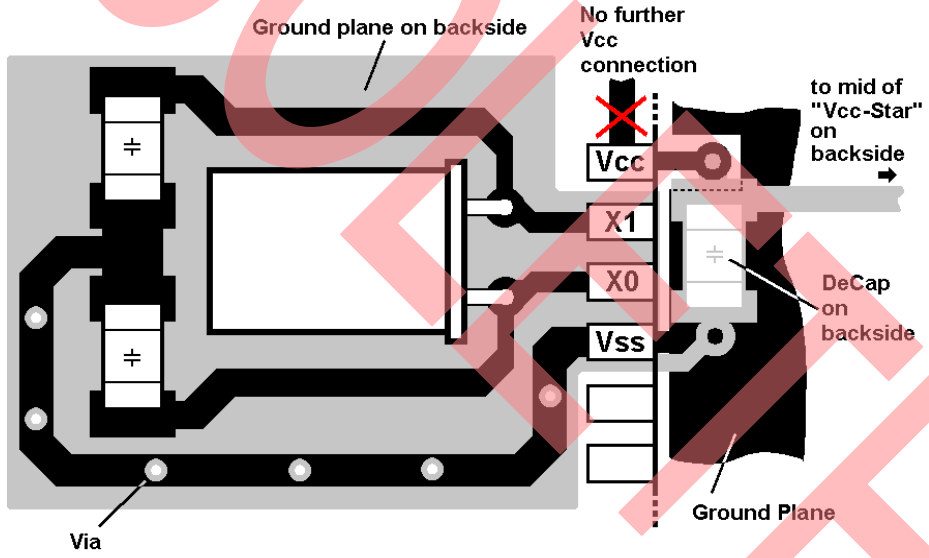
3.5 Quartz Crystal Placement and Signal Routing

The crystal has to be placed as nearest as possible to the MCU. Therefore the oscillator capacitors has to be placed “behind” the crystal.

For single metal layer circuit board the following placement and signal routing is recommended:



For double sided metal layer layout the following is recommended:



3.6 Other documents

For further detailed information please refer to the application note *16bit-EMC-Guideline* which are also valid for 32 bit MCUs.

3.7 Resonator/Crystal IC matcher

Proposals for resonators/crystals can be found on following websites:

muRata: http://search.murata.co.jp/Ceramy/ICsearchAction.do?sLang=en

Kyocera/AVX: http://www3.kyocera.co.jp/electro/app/en/searchTopShow.do

Please consider the recommendations of the application note MCU-AN-300007.

OBSOLETE

3.8 MCU Pin Summary

The following table shows the EMC critical pins and gives short information about how to connect them.

Pin name	Function
VCC	Main supply for IO buffer MCU core, close to input the internal 1.2V regulator, close to crystal oscillator
VSS	Main supply for IO buffer and MCU core, close to the internal 1.2V regulator, close to crystal oscillator
C	External 1..10µF ceramic capacitor (dielectric X7R) as smooth capacitors for internal 1.2V regulator output, it is used for supply of the MCU core. Note, that this pin leads the most of noise. Refer to the datasheet of used MCU series for selection of capacitance value.
AVCC	Power supply for the A/D converter
AVSS	Power supply for the A/D converter
AVRH	Reference voltage input for the A/D converter
USBVCC	Power supply for internal USB host/function. Use voltage according datasheet and purpose of supplied pins (USB or GPIO)
X0, X0A	Oscillator input, if not used so shall be connected with pull-up or pull-down resistor (see datasheet)
X1, X1A	Oscillator output, the crystal and bypass capacitor must be connected via shortest distance with X1/X1A pin, if not used so shall be open

4 Port Input / Unused Pins / Latch-up

How to connect Input Port Pins and how to proceed with unused Pins

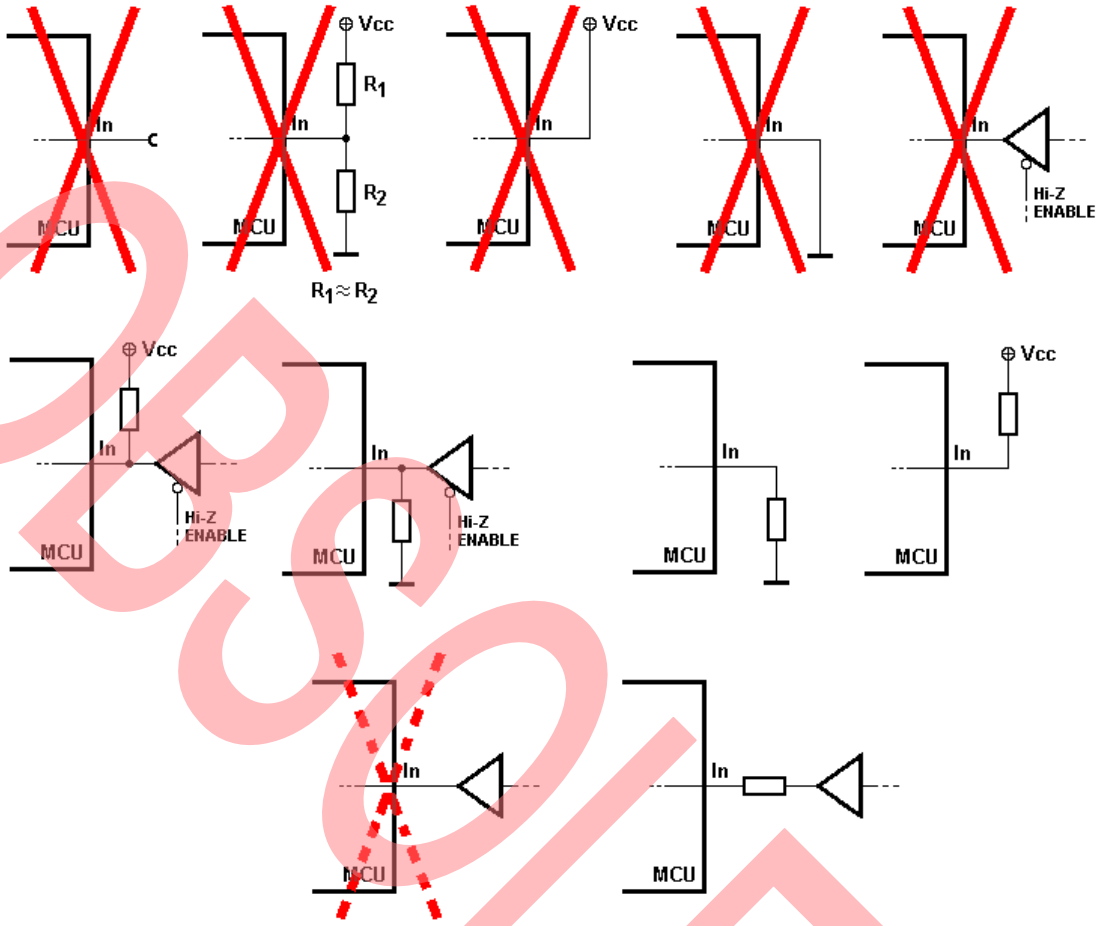
4.1 Port Input / Unused Digital I/O Pins

It is strongly recommended to do not leave digital I/O pins unconnected, while they are switched to input. In this case those pins can enter a so-called *floating state*. This can cause a high I_{CC} current, which is adverse to low power modes. Also damage of the MCU can happen.

Use the internal pull-up resistors in this case. If not, use external pull-up or pull-down resistors to define the input-level.

Never connect a potential divider with almost same resistor values.

OBSOLETE



OBSOLETE

Be careful with connection of input pins to other devices, which can go into High-Z states. Always use internal pull-up or external pull-up or pull-down resistors in this case.

Outputs from external digital circuits should always be connected via a serial resistor to a MCU input pin to prevent latch-up effects caused by under- or overshoots (4.2).

Debouncing and decoupling capacitors should always be chosen as smallest as possible. Please refer to Chapter 4.2.

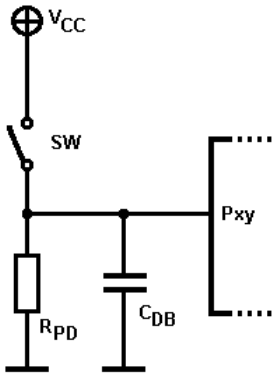
All pins are set to input after their power-on default, if they do not share an analog port. Analog ports have the digital I/O functionality disabled after reset. They may be left open, but for ESD protection they should be terminated with a pull-up/-down resistor, if not used.

Do not connect any input ports directly to V_{CC} or V_{SS} (GND) if PCB routing and power supply can carry noise! Use pull up or down resistors (2k … 4k Ohms).

4.2 Latch-up consideration (switch)

Be careful with external switches to V_{CC} or ground together with debouncing capacitors connected to port pins.

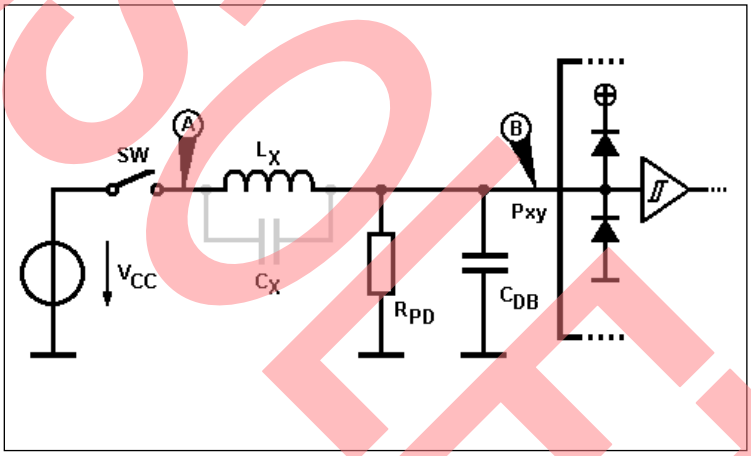
A usual configuration is shown in the following schematic:



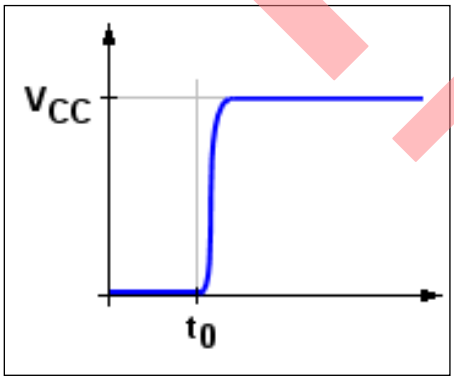
R_{PD} is a pull-down resistor and C_{BD} a debouncing capacitor. If the switch SW is open, a “0” is read from the port pin Pxy. If the switch is closed the input changes to “1”.

From the physical aspect, it has to be considered, that the switch is often placed in distance to the MCU by cable, wire, or circuit path. The longer the circuit path is the higher will be its inductivity L_X (and capacity C_X).

An equivalent circuit diagram looks like the following illustration:

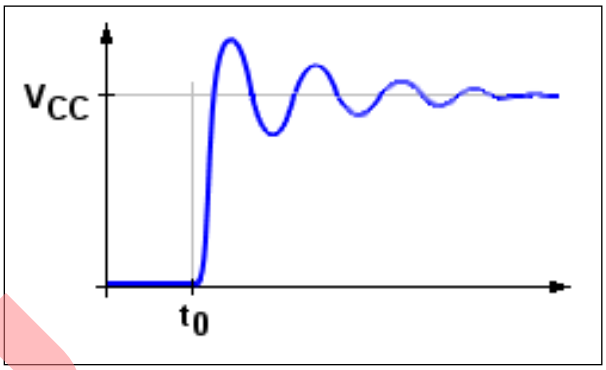


By closing the switch SW at time t_0 the following voltage can be measured at point (A):

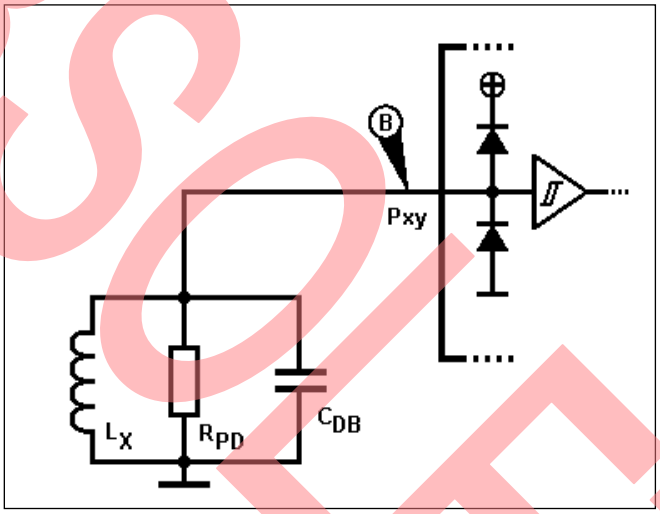


OBSOLETE

But at the port pin Pxy on point (B) the following voltage can be measured:

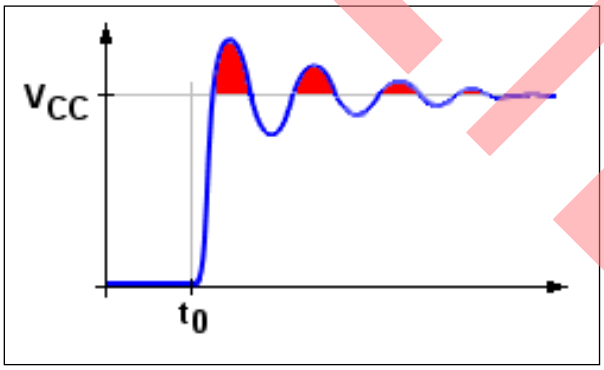


By closing the switch SW the circuit becomes a parallel oscillator with the wire-inductivity LX, the debouncing capacity CX and the damping RPD of the pull-down resistor (Assume the power supply to be ideal, i. e. it has no internal resistance):



Because R_{PD} is often chosen high (> 50 K Ohms), its damping effect is weak.

This (weakly) attenuated oscillator causes voltage overshoots on the port pin, drawn in red in the illustration below:



These overshoots may cause an internal latch-up on the port pin, because the internal clamping diode connected to V_{CC} becomes conductive. Similar is the effect, if the switch SW is opened. In this case there are under shoots on the port pin.

OBSOLETE

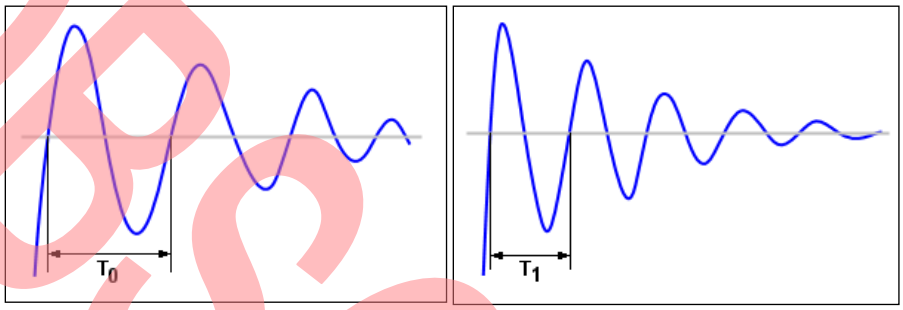
The frequency of the oscillation can be calculated by

$$f_{OSC} = \frac{1}{2\pi\sqrt{L_X C_{DB}}}$$

The inductivity L_X is the unknown value and depends on the PCB, its routing, and the wire lengths.

There are two counter measurements to prevent from latch-up.

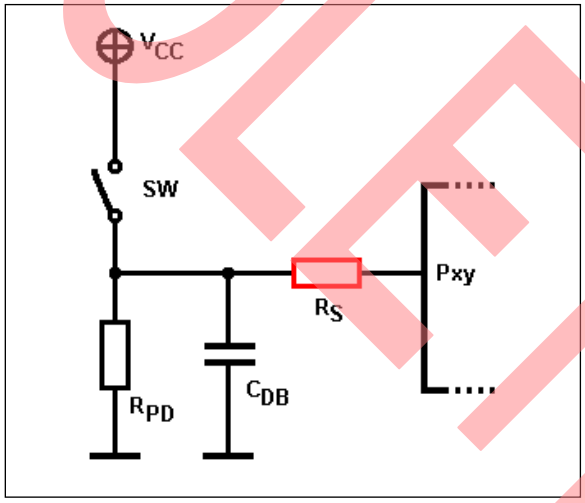
One solution is to decrease the capacity of the debouncing capacitor. This increases the oscillation frequency, and the over-all energy of the overshoots is smaller.



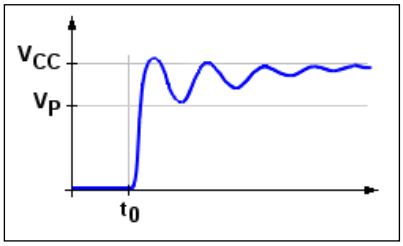
"big" capacity "small" capacity

This solution has two disadvantages: First the debouncing effect decreases and second, there is no guarantee, that the latch-up condition is eliminated.

A better solution is to use a series resistor at the port pin like in the following schematic:



The series resistor R_S reduces the amplitude of the oscillation and decreases the voltage offset at first. The resistor must not be chosen too high, so that the port pin input voltage V_P is within the positive CMOS/TTL/Automotive level.



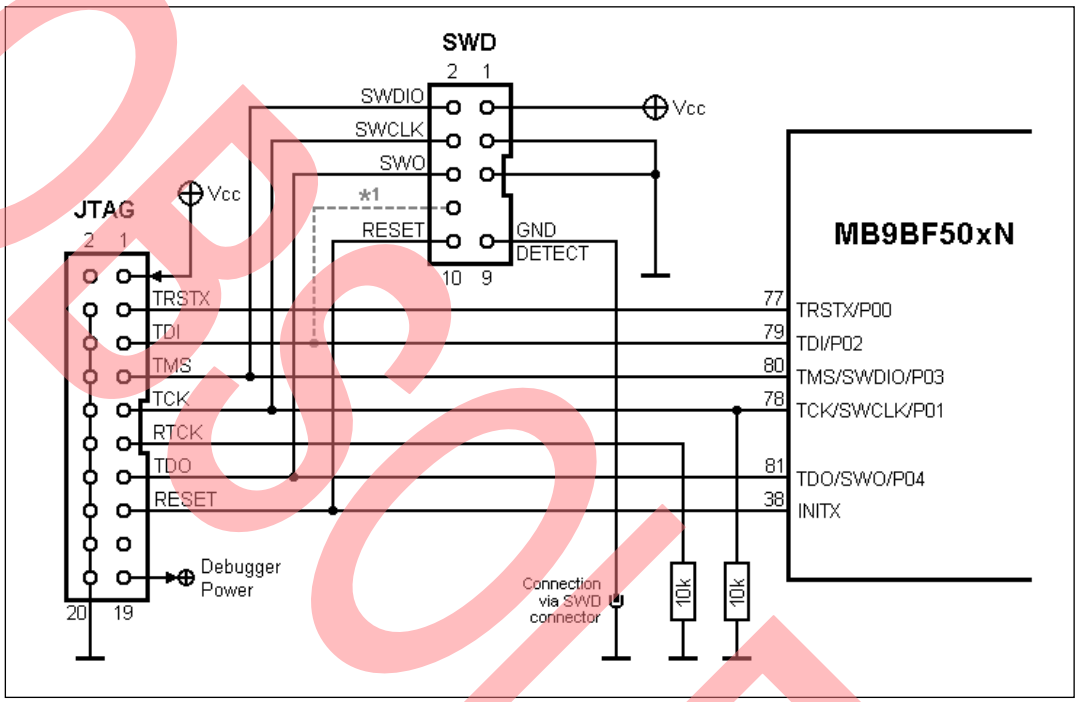
OBSOLETE

5 JTAG Connection

This chapter discusses the port connection for JTAG Debugging

5.1 JTAG/SWD

The FM3 MCU family supports JTAG debugging for full JTAG and SWD. The following schematic shows the connection for the MB9BF50xN as an example. Refer to the corresponding datasheet for different FM3 derivatives and their JTAG/SWD pin locations.

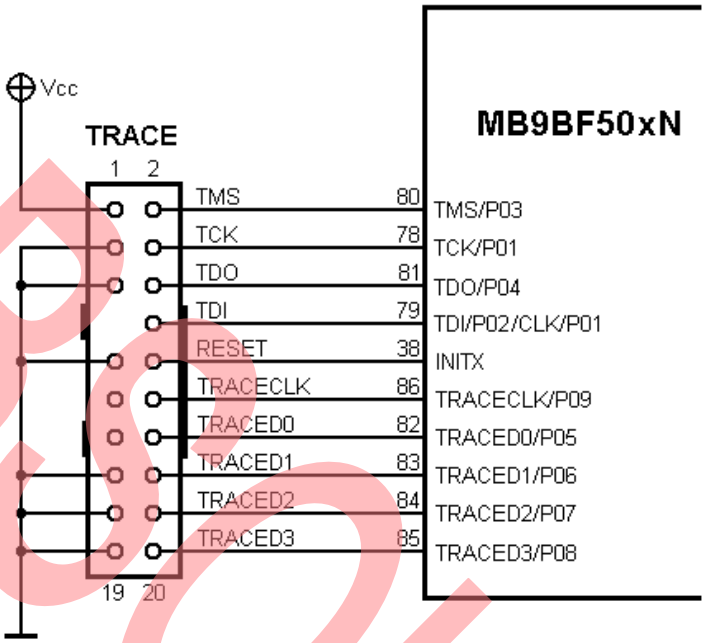


*1 only needed, if SWD connector should also provide JTAG lines

OBSOLETE

5.2 ETM Trace Port

Besides the JTAG/SWD ports the FM3 MCU family supports also debug trace ports. The following schematic shows the connection for the MB9BF50xN as an example. Refer to the corresponding datasheet for different FM3 derivatives and their ETM port pin locations.



OBSOLETE

Document History

Document Title: AN204877 - FM3 MB9BFXXX Series, Hardware Set Up

Document Number: 002-04877

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	MAWI	02/03/2011	Initial Release
			03/24/2011	Update crystal supplier links
*A	5062249	MAWI	01/05/2016	Migrated Spansion Application Note MCU-AN-300400-E-V11 to Cypress format
*B	5874608	AESATMP8	09/06/2017	Updated logo and Copyright.
*C	6501436	WOFR	03/05/2019	Obsolete the document, as this product is longer needed.

OBSOLETE

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6 MCU

Cypress Developer Community

Community | Projects | Videos | Blogs | Training | Components

Technical Support

cypress.com/support

OBSOLETE

All other trademarks or registered trademarks referenced herein are the property of their respective owners.

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709

© Cypress Semiconductor Corporation, 2011-2019. This document is the property of Cypress Semiconductor Corporation and its subsidiaries, including Spansion LLC ("Cypress"). This document, including any software or firmware included or referenced in this document ("Software"), is owned by Cypress under the intellectual property laws and treaties of the United States and other countries worldwide. Cypress reserves all rights under such laws and treaties and does not, except as specifically stated in this paragraph, grant any license under its patents, copyrights, trademarks, or other intellectual property rights. If the Software is not accompanied by a license agreement and you do not otherwise have a written agreement with Cypress governing the use of the Software, then Cypress hereby grants you a personal, non-exclusive, nontransferable license (without the right to sublicense) (1) under its copyright rights in the Software (a) for Software provided in source code form, to modify and reproduce the Software solely for use with Cypress hardware products, only internally within your organization, and (b) to distribute the Software in binary code form externally to end users (either directly or indirectly through resellers and distributors), solely for use on Cypress hardware product units, and (2) under those claims of Cypress's patents that are infringed by the Software (as provided by Cypress, unmodified) to make, use, distribute, and import the Software solely for use with Cypress hardware products. Any other use, reproduction, modification, translation, or compilation of the Software is prohibited.

TO THE EXTENT PERMITTED BY APPLICABLE LAW, CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS DOCUMENT OR ANY SOFTWARE OR ACCOMPANYING HARDWARE, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. No computing device can be absolutely secure. Therefore, despite security measures implemented in Cypress hardware or software products, Cypress shall have no liability arising out of any security breach, such as unauthorized access to or use of a Cypress product. CYPRESS DOES NOT REPRESENT, WARRANT, OR GUARANTEE THAT CYPRESS PRODUCTS, OR SYSTEMS CREATED USING CYPRESS PRODUCTS, WILL BE FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (collectively, "Security Breach"). Cypress disclaims any liability relating to any Security Breach, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any Security Breach. In addition, the products described in these materials may contain design defects or errors known as errata which may cause the product to deviate from published specifications. To the extent permitted by applicable law, Cypress reserves the right to make changes to this document without further notice. Cypress does not assume any liability arising out of the application or use of any product or circuit described in this document. Any information provided in this document, including any sample design information or programming code, is provided only for reference purposes. It is the responsibility of the user of this document to properly design, program, and test the functionality and safety of any application made of this information and any resulting product. "High-Risk Device" means any device or system whose failure could cause personal injury, death, or property damage. Examples of High-Risk Devices are weapons, nuclear installations, surgical implants, and other medical devices. "Critical Component" means any component of a High-Risk Device whose failure to perform can be reasonably expected to cause, directly or indirectly, the failure of the High-Risk Device, or to affect its safety or effectiveness. Cypress is not liable, in whole or in part, and you shall and hereby do release Cypress from any claim, damage, or other liability arising from any use of a Cypress product as a Critical Component in a High-Risk Device. You shall indemnify and hold Cypress, its directors, officers, employees, agents, affiliates, distributors, and assigns harmless from and against all claims, costs, damages, and expenses, arising out of any claim, including claims for product liability, personal injury or death, or property damage arising from any use of a Cypress product as a Critical Component in a High-Risk Device. Cypress products are not intended or authorized for use as a Critical Component in any High-Risk Device except to the limited extent that (i) Cypress's published data sheet for the product explicitly states Cypress has qualified the product for use in a specific High-Risk Device, or (ii) Cypress has given you advance written authorization to use the product as a Critical Component in the specific High-Risk Device and you have signed a separate indemnification agreement.

Cypress, the Cypress logo, Spansion, the Spansion logo, and combinations thereof, WICED, PSoC, CapSense, EZ-USB, F-RAM, and Traveo are trademarks or registered trademarks of Cypress in the United States and other countries. For a more complete list of Cypress trademarks, visit cypress.com. Other names and brands may be claimed as property of their respective owners.