THIS SPEC IS OBSOLETE

Spec No: 002-04329

Spec Title: AN204329 - ICS FOR MONITORING POWER VOLTAGE POWER SUPPLY ASSP APPLICATION NOTES

Replaced by: None

AN204329

ICs for Monitoring Power Voltage Power Supply ASSP Application Notes

Associated Part Number: MB3761, MB3771, MB3773, MB3790, MB3793

This application note is composed of a collection of frequently asked questions and data items which provide supplementary information to data sheets.

Contents

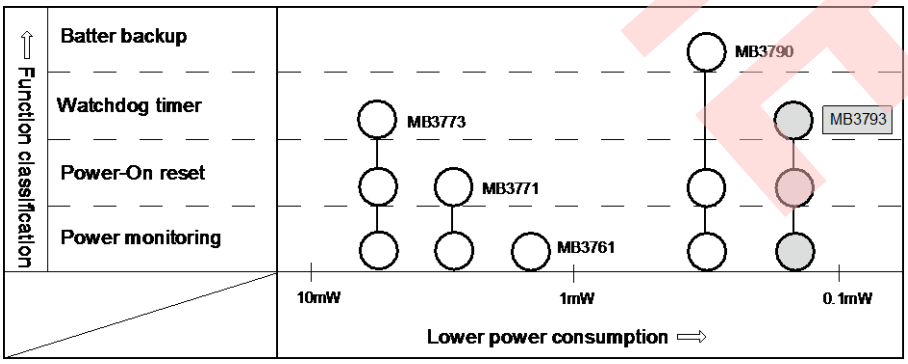
Objectives and Intended Reader

The purpose of this manual is to promote the idea among our users that Cypress' ICs are easy to use. It is composed of a collection of frequently asked questions and data items which provide supplementary information to data sheets. Through numerous examples, it provides easy-to-understand explanations aimed at helping users make effective use of our products. We hope that this manual will be helpful for the users of Cypress ICs engaged in power voltage monitoring.

It should be remembered that the circuit diagrams and data values mentioned in this manual are for reference use only and that these numerical values are not guaranteed ones.

This manual should be read by engineers responsible for developing products which will use Cypress ICs for monitoring power voltage.

Function Classification of ICs for Monitoring Power Voltage



1 MB3761 Applications

1.1 How to Produce Hysteresis Characteristics

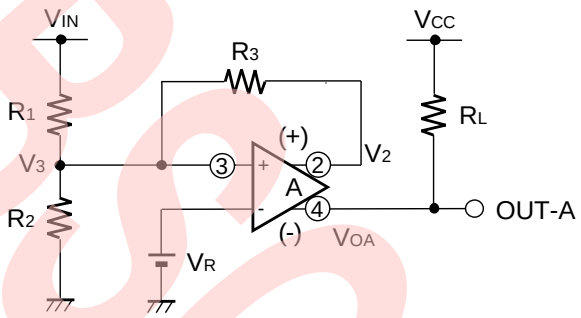
Using an external circuit, it is possible to add hysteresis characteristics to Comparators A and B (Comp. A and Comp. B) that are housed in the MB3761.

Related data sheet(s): Operational Definitions

1.1.1 Hysteresis Characteristics for Comp. A

Comp. A shows different values of detection, depending on whether there is a current flow through R_3 (refer to Figure 1).

Figure 1. Comp. A Equivalent Circuit



At the Time of a V_{IN} Rise

As shown in Figure 1, set an equivalent circuit. If the pin 3 terminal voltage (V_3) is lower than V_R, the internal circuit operates as shown in Figure 3; the transistors at pins (2 and 4) are off. Because of an R_L pull-up, pin 4 provides an H output, which corresponds to the [1] range in Figure 2.

There is no current flow at point P, so that no current will flow out from pin (2). Therefore, there is no current flow at R_3. This means that the Figure 1 and Figure 4 circuits are equivalent.

Figure 2. Output Operation of Comp. A (during a V_{IN} rise)

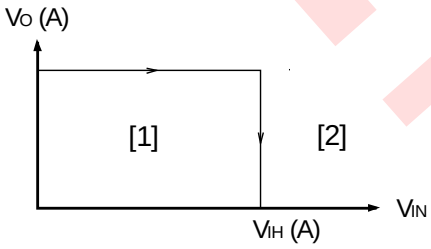


Figure 3. Circuit Operation of Comp. A with Pin 3 Terminal Voltage Lower than V_R

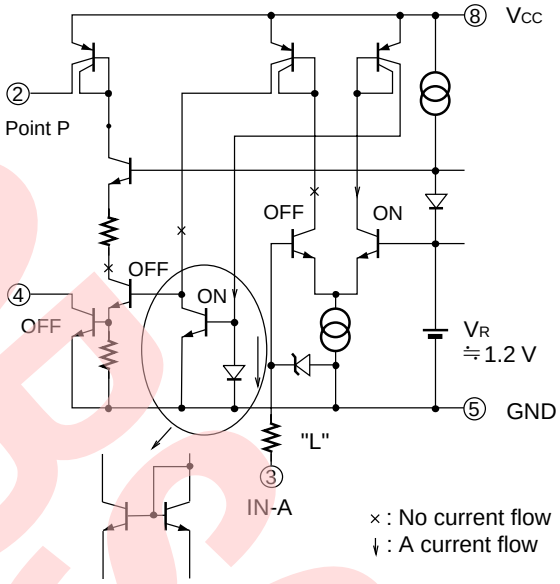
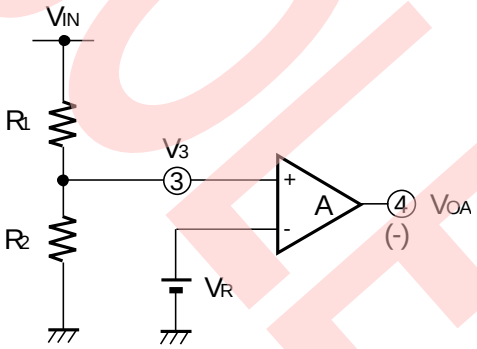


Figure 4. Equivalent Circuit of Comp. A Under $V_3 < V_R$ Condition



The pin 3 terminal voltage (V_3) may be calculated from the following equation.

$$V_3 = \frac{R_2}{R_1 + R_2} V_{IN}$$

the detection voltage, V_{IN} (A), will reach the value of V_{IN} available when $V_3 = V_R$. Therefore, the following equation applies.

$$V_{IH}\ (A) = \frac{R_1 + R_2}{R_2} VR$$

$$= (1 + \frac{R_1}{R_2})\ VR$$

This reverses the output, resulting in the [2] range in Figure 2.

At the Time of a V_{IN} Fall

As the value of V_{IN} is decreased gradually, the internal circuit operates as shown in Figure 6, when the pin 3 terminal voltage is higher than V_R (this corresponds to the [3] range in Figure 5. The internal transistors at pins 2 and 4 are turned on. This changes the output at pin 4 to the L level, so that a current begins to flow at the pin 2 terminal (refer to Figure 7).

Figure 5. Output Operation of Comp. A (during a V_{IN} fall)

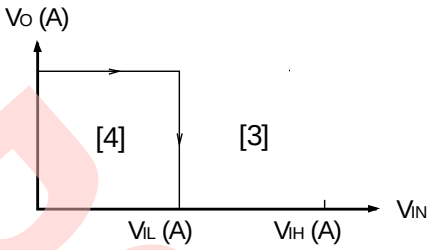


Figure 6. Circuit Operation of Comp. A with Pin 3 Terminal Voltage Higher than V_R

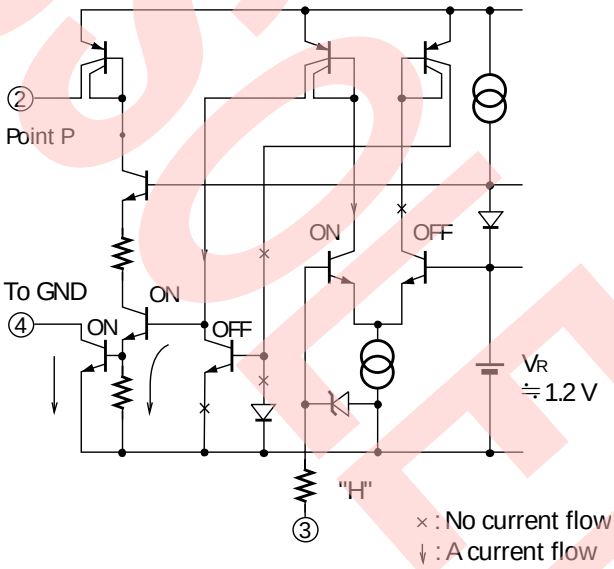
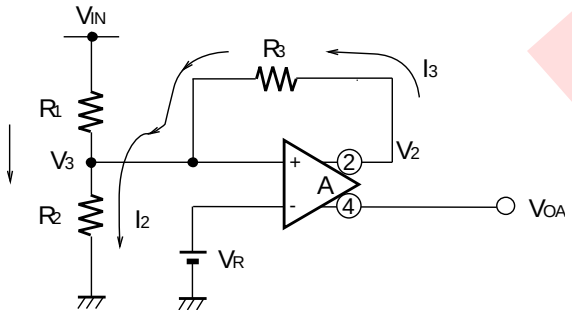


Figure 7. Equivalent Circuit of Comp. A Under $V_3 > V_R$ Condition



As shown in Figure 7, there is a current flow (I_3) through R_3, thus increasing the value of current I_2 flowing through R_2. This, in turn, increases the voltage drop through R_2 and increases the V_3 voltage level. To meet the $V_3 = V_R$ relationship, the increase in the V_3 voltage level requires a lower V_{IN} value, which is lower than the value of V_{IN} available during the change from [1] to [2] in Figure 2 (refer to the description of hysteresis characteristics).

Under these conditions, the following equations apply.

$$\frac{V_2 - V_3}{R_3} + \frac{V_{IN} - V_3}{R_1} = \frac{V_3}{R_2} \quad \text{---(a)}$$

$$V_2 \fallingdotseq V_{CC} \quad \text{---(b)}$$

Substituting equation (b) into equation (a) provides the V_{IN} equation as follows.

$$V_{IN} = V_3\left(1 + \frac{R_1}{R_2 // R_3}\right) - \frac{R_1}{R_3} V_{CC}$$

The detection voltage, V_{IL} (A), will reach the value of V_{IN} available when $V_3 = V_R$.

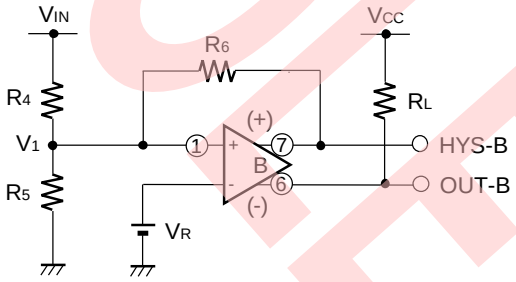
Therefore, the following equation applies.

$$V_{IL}(A) = V_R\left(1 + \frac{R_1}{R_2 // R_3}\right) - \frac{R_1}{R_3} V_{CC}$$

1.1.2 Hysteresis Characteristics for Comp. B

Comp. B shows different values of detection, depending on whether there is a current flow through R6 (refer to Figure 8).

Figure 8. Comp. B Equivalent Circuit



At the Time of a V_{IN} Fall

As shown in Figure 8, set an equivalent circuit. If the pin 1 terminal voltage (V_1) is higher than V_R, the internal circuit operates as shown in Figure 10; the transistor at pin 6 is turned on. V_O (B) provides an L output, which corresponds to the [1] range in Figure 9.

The transistor at pin 7 is turned off, so that no current will flow at point P of R_6. In this case, the Figure 8 and Figure 11 circuits are equivalent.

Figure 9. Output Operation of Comp. B (during a V_{IN} fall)

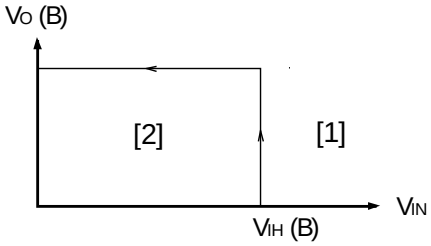


Figure 10. Circuit Operation of Comp. B with Pin 1 Terminal Voltage Higher than V_R

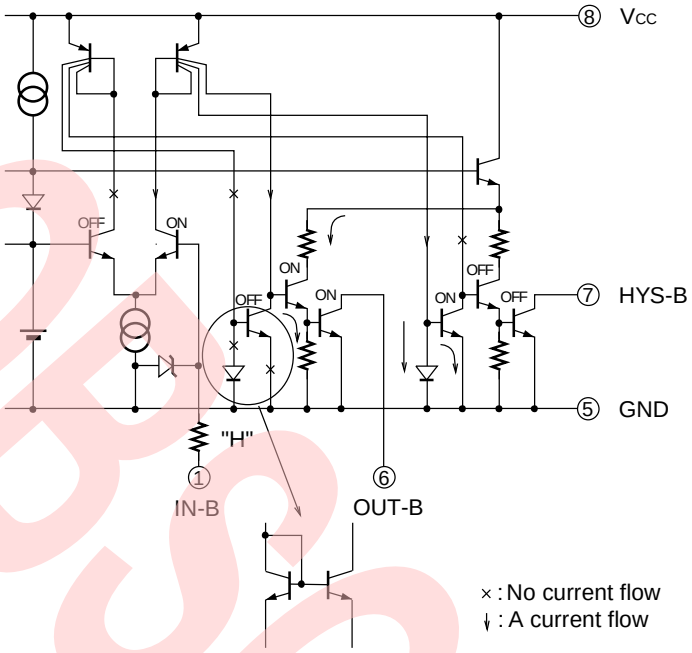
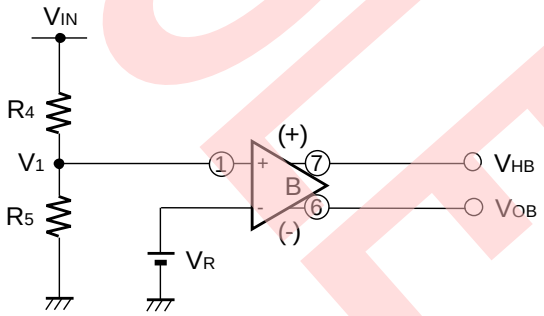


Figure 11. Equivalent Circuit of Comp. B Under $V_1 > V_R$ Condition



From Figure 11 the threshold voltage, V_{IL} (B), may be expressed as follows.

$$V_{IL}(B) = (1 + \frac{R_4}{R_5})V_R$$

At the Time of a V_{IN} Rise

As the value of V_{IN} is increased gradually, the internal circuit operates as shown in Figure 13, when the pin 1 terminal voltage is lower than V_R (this corresponds to the [3] range in Figure 12). This turns off the internal transistor at pin 6 and turns on the internal transistor at pin 7. In this case, the Figure 8 and Figure 14 circuits are equivalent.

Figure 12. Output Operation of Comp. B (during a V_{IN} rise)

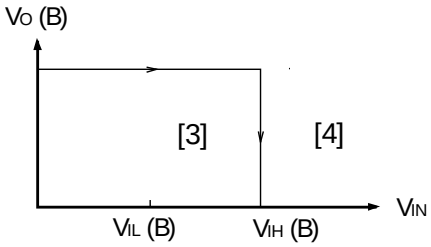


Figure 13. Circuit Operation of Comp. B with Pin 1 Terminal Voltage Lower than V_R

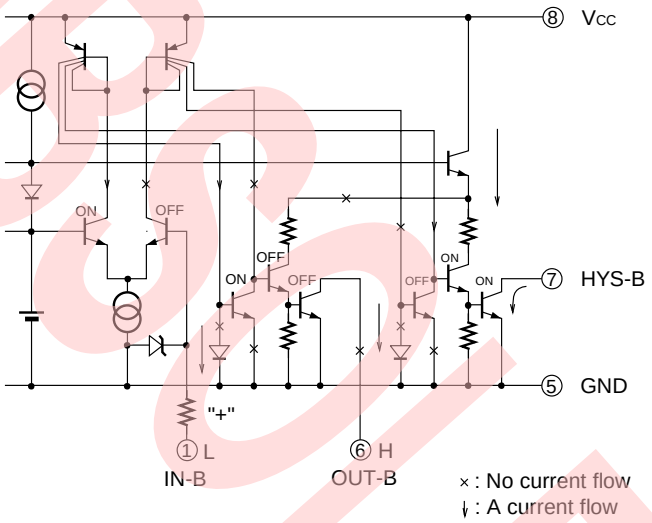
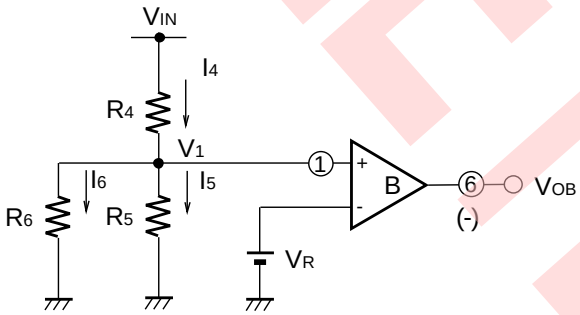


Figure 14. Equivalent Circuit of Comp. B Under $V_1 < V_R$ Condition



As shown in Figure 14, when pin 7 changes to the L level, current I_4 flowing through R_4 branches into current I_6 flowing through R_6 and current I_5 flowing through R_5. This reduces the R5-based voltage drop by the I6 equivalent, thus lowering the V_1 voltage level.

Causing another output reverse under the $V_1 > V_R$ condition requires a much higher value of V_{IN}, which is higher the value of V_{IN} available during the change from [1] to [2] in Figure 9, resulting in the $V_1 = V_R$ relationship (refer to the description of hysteresis characteristics).

Under these conditions, the following equation applies.

$$\frac{V_{IN} - V_1}{R_4} = \frac{V_1}{R_6} + \frac{V_1}{R_5}$$

When $V_1 = V_R$, V_{IN} satisfies the $V_{IN} = V_{IH}$ (B) relationship. As the value of V_{IN} undergoes a gradual increase, therefore, the value of detection value, V_{IH} (B), may be expressed by the following equation.

$$V_{IH}\,(B) = \left(1 + \frac{R_4}{R_5 // R_6}\right) * V_R$$

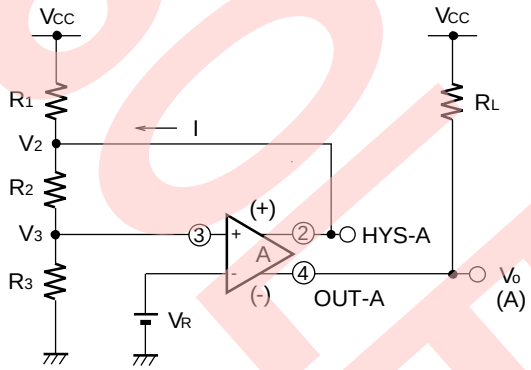
1.2 How to Add Hysteresis Characteristics

It is possible to add hysteresis characteristics to Comparators A and B (Comp. A and Comp. B) that are housed in the MB3761.

Related data sheet(s): Application Examples - Addition of Hysteresis

1.2.1 How to Add Hysteresis Characteristics to Comp. A

Figure 15. Hysteresis Characteristics Added to Comp. A

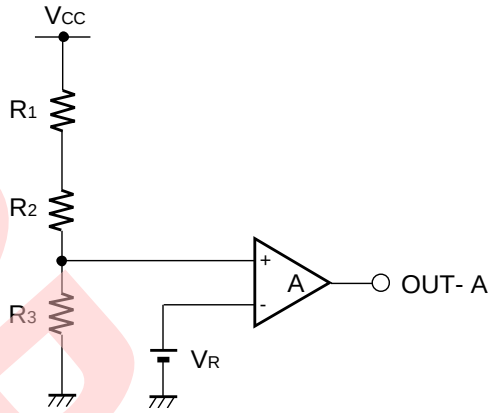


When $V_3 < V_R$

There is no current flowing out at pin (2) because the internal transistor at pin (2) shown in Figure 15 is off. This is equivalent to the Figure 16 circuit; therefore, the detection voltage may be expressed by the following equation.

$$V_{IH}(A) = \left(1 + \frac{R_1 + R_2}{R_3}\right) V_R$$

Figure 16. Equivalent Circuit of Comp. A Under $V_3 < V_R$ Condition

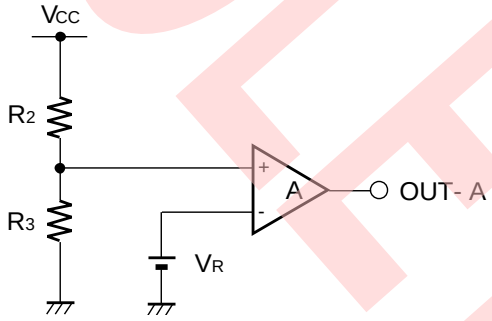


When $V_3 > V_R$

The internal transistor at pin (2) shown in Figure 15 is turned on, so that V_2 is nearly equal to V_{CC}. This is equivalent to the Figure 17 circuit; therefore, the detection voltage may be expressed by the following equation.

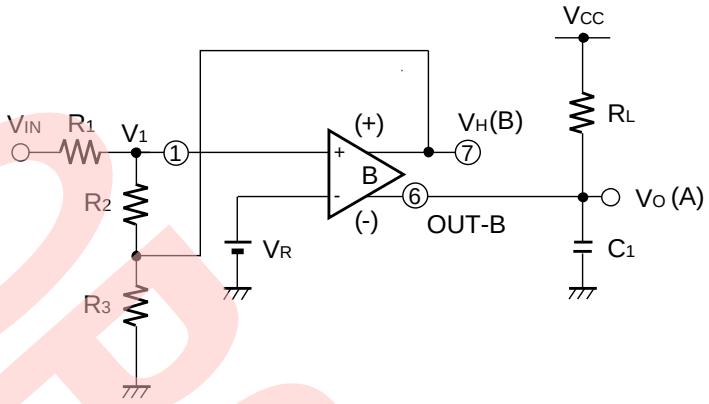
$$V_{IL}(A) = \left(1 + \frac{R_2}{R_3}\right) V_R$$

Figure 17. Equivalent Circuit of Comp. A Under $V_3 > V_R$ Condition



1.2.2 How to Add Hysteresis Characteristics to Comp. B

Figure 18. Hysteresis Characteristics Added to Comp. B



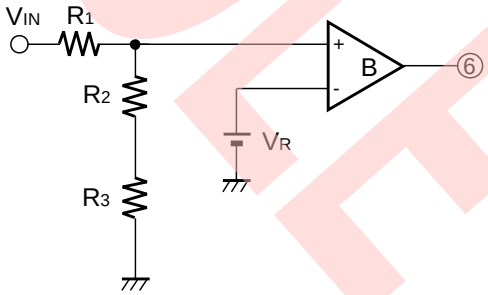
When $V_1 > V_R$

The internal transistor at pin (7) shown in Figure 18 is off and an equivalent circuit is given in Figure 19. When the internal output transistor at pin (6) is turned on, the output level changes to L.

The detection voltage may be expressed by the following equation.

$$V_{IL}(B) = (1 + \frac{R_1}{R_2 + R_3})V_R$$

Figure 19. Equivalent Circuit of Comp. B Under $V_1 > V_R$ Condition



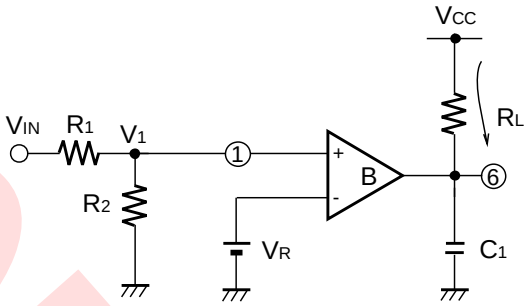
When $V_1 < V_R$

Because the internal transistor at pin (7) shown in Figure 18 is on, the output level changes to L; an equivalent circuit is given in Figure 20. When the internal output transistor at pin (6) is turned off, the output level changes to H.

The detection voltage may be expressed by the following equation.

$$V_{IH}(B) = (1 + \frac{R_1}{R_2})V_R$$

Figure 20. Equivalent Circuit of Comp. B Under $V_1 < V_R$ Condition

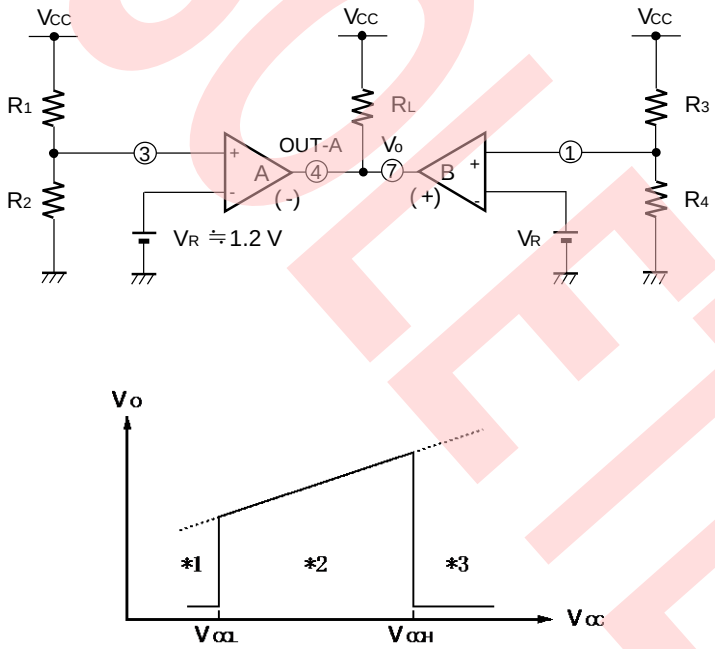


1.3 How to Search for Power Voltage Malfunctions [1]

This section explains how to search for malfunctions in power voltage using the MB3761.

Related data sheet(s): Application Examples - Voltage Detection for Alarm

How to Search for Power Voltage Malfunctions [1]



*1: When $V_{CC} < V_{CCL}$

When the output at pin (4) in Comp. A changes to H, V_O changes to L.

When the output at pin (7) in Comp. B changes to L, V_O changes to L.

As the detection voltage in Comp. B, V_{CCL} may be expressed by the following equation.

$$V_{CCL} = (1 + \frac{R_3}{R_4})V_R$$

*2: When $V_{CC} < V_{CCL} < V_{CCH}$

When the output at pin (4) in Comp. A changes to H, V_O changes to H.

When the output at pin (7) in Comp. B changes to H, V_O changes to H.

*3: When $V_{CC} > V_{CCH}$

When the output at pin (4) in Comp. A changes to L, V_O changes to L.

When the output at pin (7) in Comp. B changes to H, V_O changes to L.

As the detection voltage in Comp. A, V_{CCH} may be expressed by the following equation.

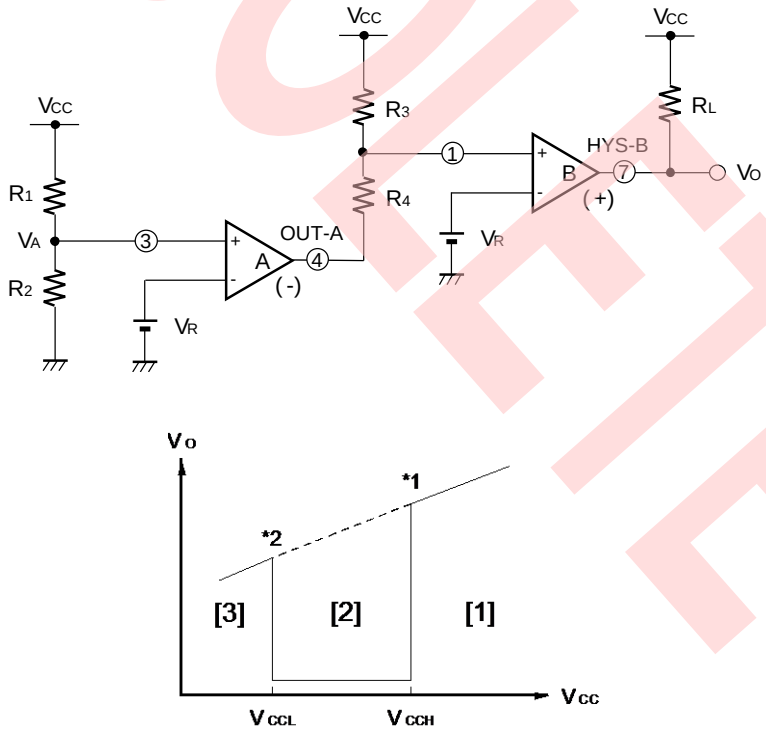
$$V_{CCH} = (1 + \frac{R_1}{R_2})V_R$$

1.4 How to Search for Power Voltage Malfunctions [2]

This section explains how to search for malfunctions in power voltage using the MB3761.

Related data sheet(s): Application Examples - Voltage Detection for Alarm

How to Search for Power Voltage Malfunctions [2]



[1]: At a high value of V_{CC}, if the $V_R < V_A$ relationship is met, the output of Comp. A changes to the L level and the value of V_B depends on the R_3 and R_4 combination.

[2]: When $V_B < V_R$, the output of Comp. B changes to the L level.

[3]: If the value of V_{CC} decreases and the $V_R > V_A$ relationship is met, the OUT-A output changes to H and the output of Comp. B also changes to H.

[How Comp. B works]

When Pin (4) of OUT-A is at the L Level

*1: $V_{CC} > \frac{R_3+R_4}{R_4} \cdot V_R$ - - - The output V_O changes to the H level.

*1: $V_{CC} < \frac{R_3+R_4}{R_4} \cdot V_R$ - - - The output V_O changes to the L level.

When Pin (4) of OUT-A is at the H Level

The output Vo changes to the H level.

[How Comp. A works]

*2: $V_{CC} > \frac{R_1+R_2}{R_2} \cdot V_R$ - - - The OUT - A output changes to the L level.

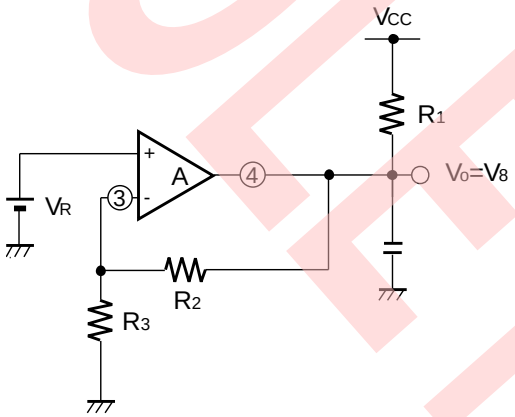
*2: $V_{CC} < \frac{R_1+R_2}{R_2} \cdot V_R$ - - - The OUT - A output changes to the H level.

1.5 Programmable Zener

This section explains programmable Zener that use the MB3761.

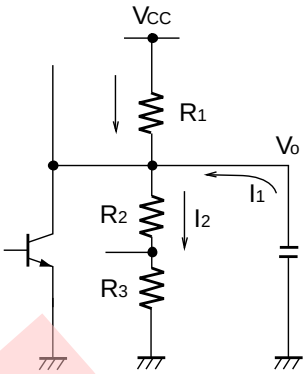
Related data sheet(s): Application Examples - Programmable Zener

- **Programmable Zener**



$$VO = \frac{R2 + R3}{R3} \cdot VR$$

$$= (1 + \frac{R2}{R3}) \cdot VR$$



6mA* > I_1 > I_2

*: Because of transistor capability

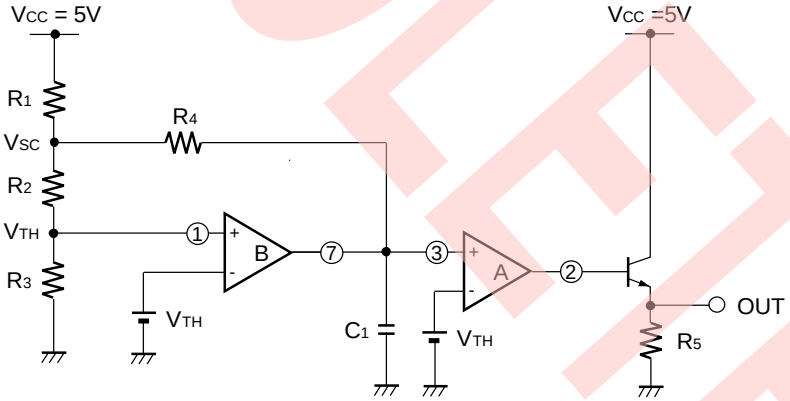
1.6 Calculation in Sample Circuit for Resetting Reduced Voltage

This section explains equations regarding a sample circuit used for resetting reduced voltage using the MB3761.

Related data sheet(s): Application Examples - Recovery Reset Circuit

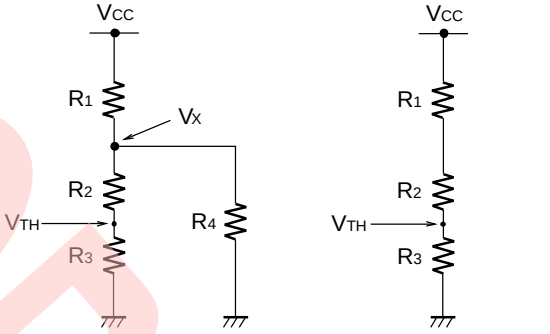
Calculation in Sample Circuit Used for Resetting Reduced Voltage

Figure 21. Equivalent Circuit for Resetting Reduced Voltage



[How to Calculate V_{CC} (H) and V_{CC} (L)]

Figure 22. Equivalent Circuits for V_{CC} (H) and V_{CC} (L)



Equivalent to VCC (H) Equivalent to VCC (L)

How to Calculate V_{CC} (H):

$$\frac{(R_2+R_3)//R_4}{R_1+(R_2+R_3)//R_4}V_{CC}=V_X \quad ---(a)$$

$$\frac{R_3}{R_2+R_3}V_X=V_{TH} \quad ---(b)$$

From (a) and (b), you get the following equation

$$\frac{\frac{(R_2+R_3)R_4}{R_2+R_3+R_4}}{R_1+\frac{(R_2+R_3)R_4}{R_2+R_3+R_4}}V_{CC}=\frac{R_2+R_3}{R_3}V_{TH}$$

$$\frac{(R_2+R_3)R_4}{R_1(R_2+R_3+R_4)+(R_2+R_3)R_4}V_{CC}=\frac{R_2+R_3}{R_3}V_{TH}$$

$$\begin{aligned}V_{CC}(H)&=\frac{R_1(R_2+R_3+R_4)+(R_2+R_3)R_4}{R_3R_4}V_{TH}\\&=\frac{R_1(R_2+R_3)}{R_3R_4}V_{TH}+\frac{(R_1+R_2+R_3)R_4}{R_3R_4}V_{TH}\\&=\frac{R_1(R_2+R_3)}{R_3R_4}V_{TH}+V_{CC}(L)\end{aligned}$$

How to Calculate V_{CC} (L):

$$\frac{R_3}{R_1+R_2+R_3}V_{CC} = V_{TH} \quad ---(c)$$

From (c), you get the following equation

$$V_{CC}(L) = \frac{R_1+R_2+R_3}{R_3}V_{TH}$$

1.7 How to Search for Malfunctions in Power Voltage with Hysteresis Characteristics [1]

This section explains how to search for malfunctions in power voltage with hysteresis characteristics using the MB3761.

Related data sheets: Operational Definitions

Application Examples - Voltage Detection for Alarm

How to Search for Malfunctions in Power Voltage with Hysteresis Characteristics [1]

See Figure 22, which is a combination of the circuits in the Operational Definitions and Application Examples - Voltage Detection for Alarm data sheets. The detection voltage may be expressed by the following equation.

$$V_{IL}(B) = (1+\frac{R_4}{R_5}) \times V_R$$

$$V_{IL}(B) = (1+\frac{R_4}{R_5 // R_6}) \times V_R$$

$$V_{IL}(A) = (1+\frac{R_4}{R_2 // R_3}) \times V_R - \frac{R_4}{R_3} \times V_{CC}$$

$$V_{IL}(A) = (1+\frac{R_1}{R_2}) \times V_R$$

Note: Check for proper operation by considering factors such as current consumption, each terminals' maximum rating, and recommended operating conditions. Then, set the resistance values.

Figure 23. Sample Circuit Detecting for Malfunctions in Power Voltage with Hysteresis Characteristics [1]

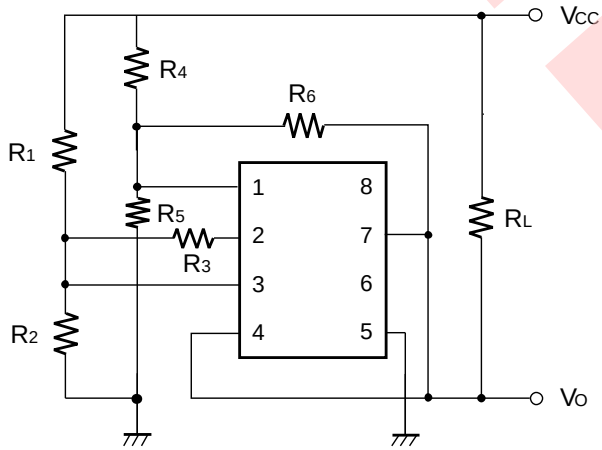


Figure 24. Output Operation of Sample Circuit Detecting for Malfunctions in Power Voltage with Hysteresis Characteristics [1]

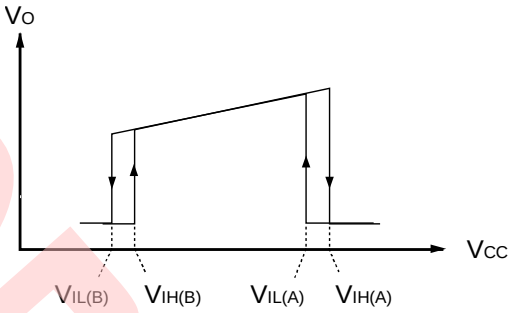
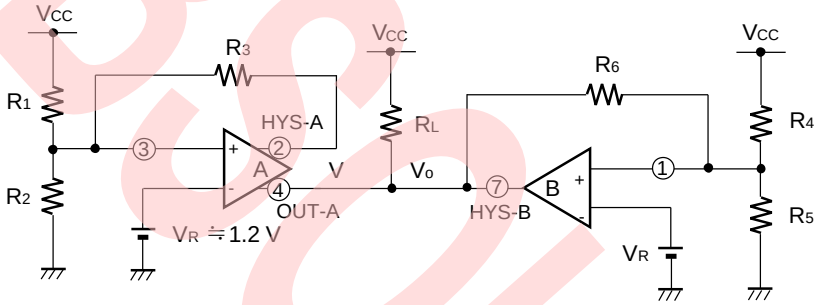


Figure 25. Equivalent Circuit Detecting Malfunctions in Power Voltage with Hysteresis Characteristics [1]



1.8 How to Search for Malfunctions in Power Voltage with Hysteresis Characteristics [2]

This section explains how to search for malfunctions in power voltage with hysteresis characteristics using the MB3761.

Related data sheets: Application Examples-Addition of Hysteresis

Application Examples-Voltage Detection for Alarm

How to Search for Malfunctions in Power Voltage with Hysteresis Characteristics [2]

See Figure 26 which is a modification of the circuits in the Addition of Hysteresis and Application Examples - Voltage Detection for Alarm data sheets. Comp. A detects for malfunctions in V_{CCL1} and V_{CCL2}; and Comp. B for V_{CCH3} and V_{CCH4}.

The detection voltage may be expressed by the following equations.

$$V_{CCL1} = (1 + \frac{R_2}{R_3}) \times V_R$$

$$V_{CCL2} = (1 + \frac{R_1 + R_2}{R_3}) \times V_R$$

$$V_{CCH3} = (1 + \frac{R_4}{R_5 + R_6}) \times V_R$$

$$V_{CCH4} = (1 + \frac{R_4}{R_5}) \times V_R$$

Note: If the desired detection voltage is relatively high, the voltage at pin (7) is small, depending on the resistance ratio. Therefore, the above method is not applicable when it is not possible to detect the system side as H level at the specified smoll voltage.

For more details, refer to the section 1.2 “How to Add Hysteresis Characteristics” and section 1.4 “How to Search for Power Voltage Malfunctions [2]”.

Figure 26. Sample Circuit Detecting for Malfunctions in Power Voltage with Hysteresis Characteristics [2]

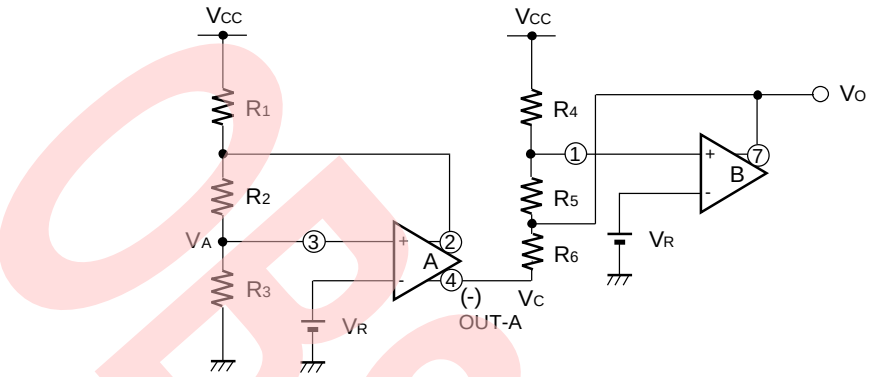
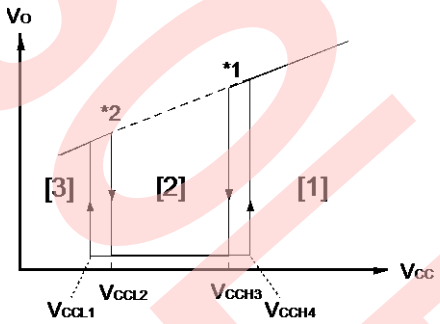


Figure 27. Output Operation of Sample Circuit Detecting for Malfunctions in Power Voltage with Hysteresis Characteristics [2]



1.9 How to Troubleshoot the MB3761

This section explains how to troubleshoot the MB3761.

How to Troubleshoot the MB3761

1. If there are output fluctuations
   - You may encounter output fluctuations when the input change speed is low. For details, refer to the sub section 1.9.1 “If There are Output Fluctuations”.
2. If hysteresis characteristics are not appropriate
   - Depending on the setting of resistance values, the measurement of the lower detection voltage may be higher than the setting. For details, refer to the sub section 1.9.2 “If Hysteresis Characteristics are not Appropriate”.

1.9.1 If There are Output Fluctuations

You may encounter output fluctuations when the input change speed is low.

If There are Output Fluctuations

[Probable Causes]

1. Because of the offset between the output OUT-B and HYS-B in comparator B (Comp. B), OUT-B may change to the H level before HYS-B changes to the L level at the falling edge of the input IN-B.If this occurs, the OUT-B output will become unstable because of noise to INB or the "2." reason below.By contrast, the circuit configuration of comparator A (Comp. A) will cause little output offset.
2. A switch between the outputs of Comp. B or Comp. A will cause a slight fluctuation in the internal reference voltage or comparator offset. The fluctuation in an extremely narrow voltage range in IN-B or IN-A is attributable to the common impedance inside the ICs.

[Corrective Action]

1. Such an unstable output will usually take place in a slight input voltage range.Therefore,this phenomenon is not seen if the input change speed is high (refer to Figure 28). At a low input change speed, it is recommended that you use Comp. A; refer to "1." in [Probable causes]. Even when you use Comp.A, however, you may encounter a similar phenomenon if the speed is extremely high.Careful experimentation and validation is necessary.
2. In case you use Comp.B with signals whose input change speed is low, it is recommended that you reverse OUT-B through an external transistor for hysteresis characteristics (refer to the Figure 29).

Figure 28. How to Remove Unstable Output [1]

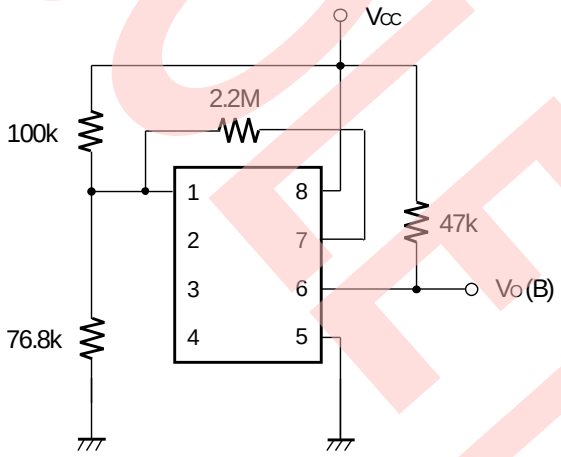
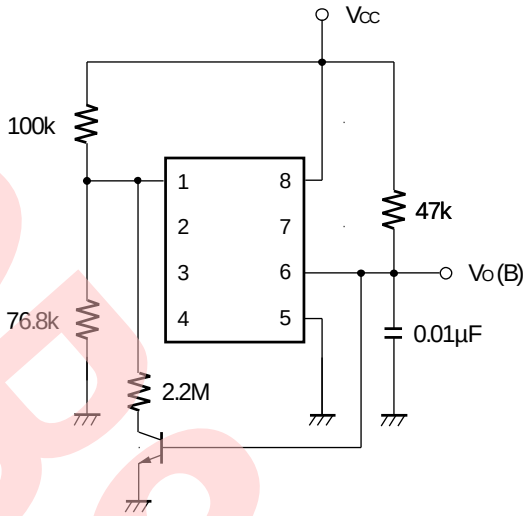


Figure 29. How to remove unstable output [2]



3. When you remove any unstable output resulting from "2." in [Probable causes] above, it is recommended that you insert a capacitor into the output in order to acquire sufficient time for hysteresis to work, and to eliminate the unstable output.

1.9.2 If Hysteresis Characteristics are not Appropriate

When you set the resistance values according to the Application Examples data sheets, the measurement of the lower detection voltage may be higher than the setting, depending on the setting of resistance values.

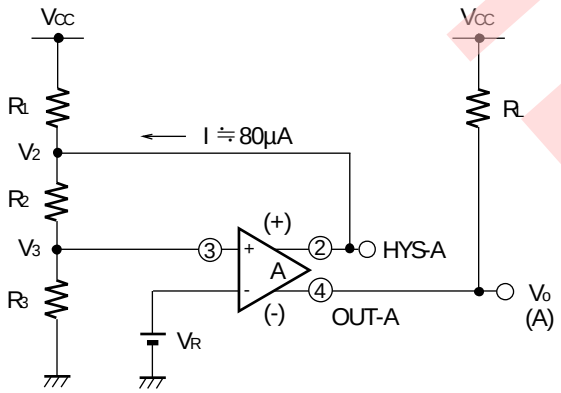
Related data sheet(s): Application Examples - Addition of Hysteresis

If Hysteresis Characteristics are not Appropriate

[Probable Cause and Corrective Action]

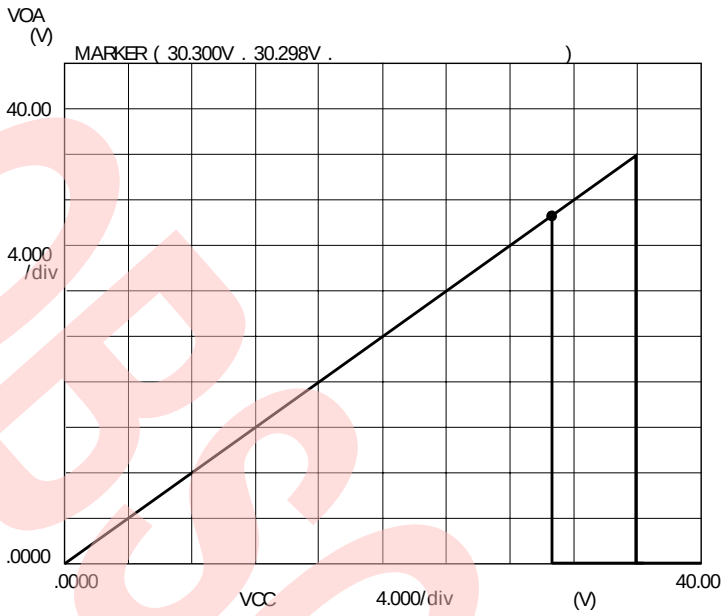
See Figure 30, which shows the operating principle of comparator A (Comp. A) in the Addition of Hysteresis data sheet. Depending on whether or not there is current I from pin 2, the value of V_2 voltage switches to produce hysteresis characteristics. The equation regarding V_{IL} (A) shown in the particular data sheet neglects any voltage drop through R_1. In reality, however, there is a small current of approximately 80 µA and the R_1-based voltage drop cannot be neglected depending on the resistance value. There may be difference between the calculated and measured values. (When V_3 is greater than V_R, the internal transistor at pin (2) is turned on. The value of V_{IL} (A) is calculated assuming that V_2 is nearly equal to V_{CC}. This assumption will cause an error because the two values are not exactly equal.)

Figure 30. Adding Hysteresis Characteristics to Comp. A



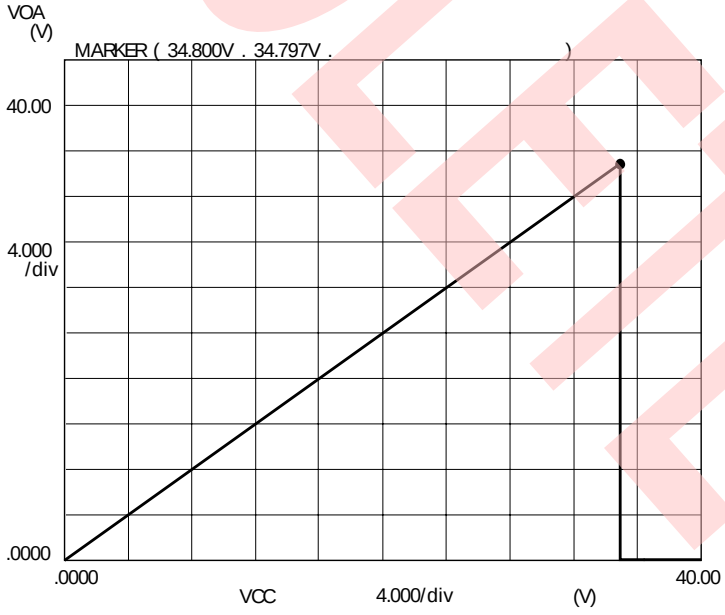
Tip: When the values of detection are set as V_{IH} (A) = 36 V and V_{IL} (A) = 30 V, resistance selection reveals differences in detection measurement, as shown in Figure 31 and Figure 32. The width of hysteresis is seen to become smaller as the resistance changes.

Figure 31. Result Close to the Setting



(R1=100k, R2=480k, R3=20k, RL=11k)

Figure 32. Result not Close to the Setting

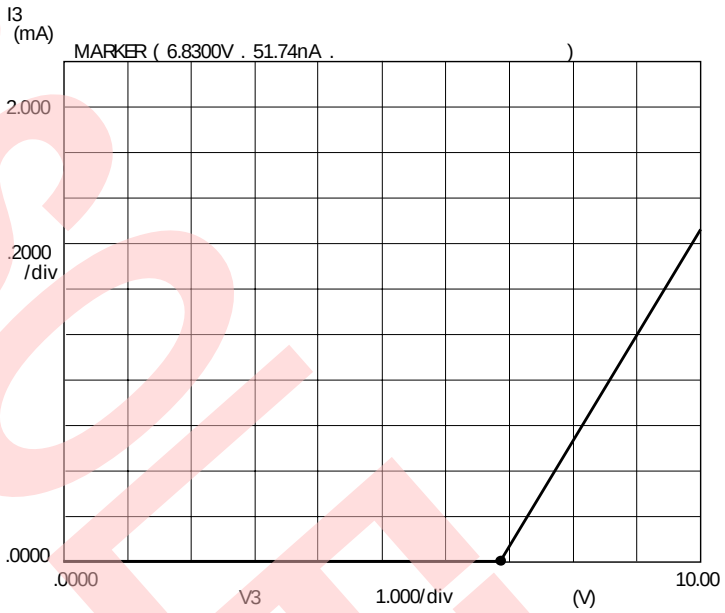
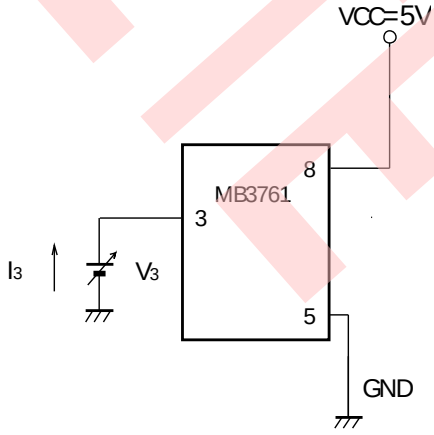


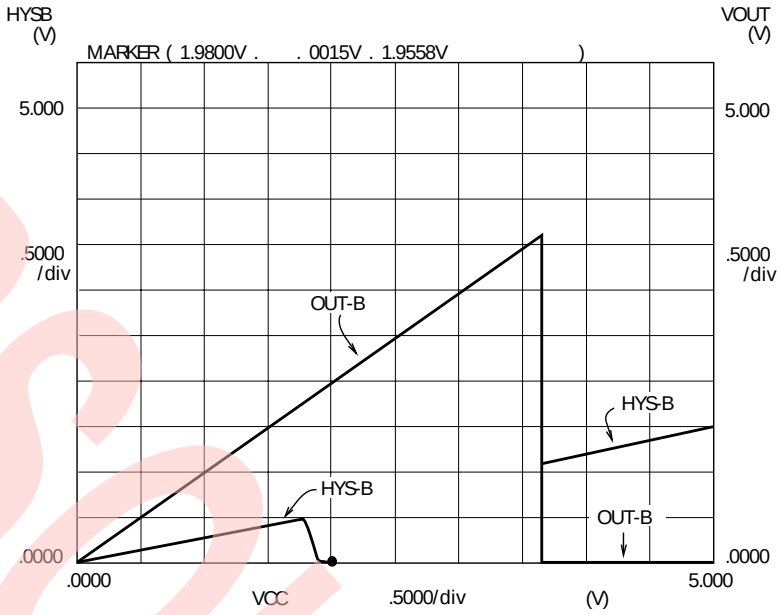
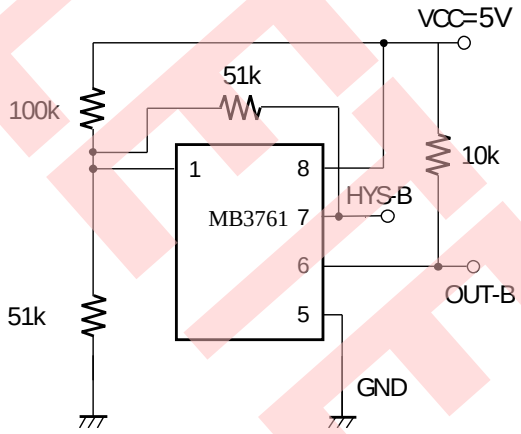
(R1=11k, R2=4.7k, R3=200W, RL=11k)

1.10 Q&A Set Regarding the MB3761

This section provides a set of questions and answers regarding the MB3761.

Q&A Set Regarding the MB3761

Q&A Set Regarding the MB3761			
Q1	Even at a V_{CC} value of 40 V, is the input voltage up to 6.5 V? What is the clamp voltage for the protective diode at pin 3?	A1	Yes, the input voltage is up to 6.5 V. The clamp voltage at pin 3 is approximately 6.5 V, as shown below. Remember that the input pins are not designed to withstand a large current.  **[Measuring circuit]** 

Q&A Set Regarding the MB3761			
Q2	With the MB3771, if the power voltage is 0.8 V, the reset provides an L output. Is this same with the MB3761?	A2	The MB3761 provides 2.5 V as the power voltage that guarantees the L level. Capability data is illustrated below.  **[Measuring circuit]** 

2 MB3771 Applications

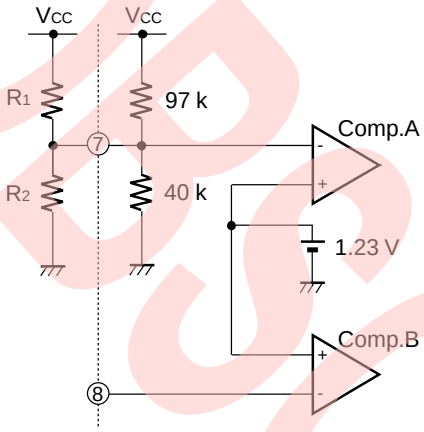
2.1 Equations for Calculating External Fine-tuning Types

It is possible to externally adjust the VSA detection voltage.

Related data sheet(s): Application Examples-Power Supply Monitor with External Adjust

2.1.1 Equations for Calculating External Fine-tuning Types

Figure 33. Equivalent Circuit for Calculating External Fine-tuning Types



Note: The internal IC resistance is plus or minus 30 % in absolutea accuracy and plus or minus 2 % in relative accuracy (potential capability: 1 %).

In Figure 33 R_A is a combined resistance between the 97 kΩ and external R_1 resistance; R_B is a combined resistance between the 40 kΩ and external R_2 resistance.

$$R_A = R_1 \times 97\ k\Omega / (R_1 + 97\ k\Omega)\ [\Omega]$$

$$R_B = R_2 \times 40\ k\Omega / (R_2 + 40\ k\Omega)\ [\Omega]$$

The detection voltage may be calculated as follows.

$$\text{Detection voltage } V_{SAL} = \frac{R_A + R_B}{R_B} \times V_{SB} \quad [V]$$ (At a falling value of V_{CC})

$$\text{Detection voltage } V_{SAH} = \frac{R_A + R_B}{R_B} \times (V_{SB} + V_{HYSB}) \quad [V]$$ (At a rising value of V_{CC})

The above calculation assumes that the threshold level of comparator B is V_{SB} equal to 1.230 V (typ.) and that the width of hysteresis is Y_{HSYB} equal to 28 mV (typ.).

If you choose appropriate values of R_1 and R_2 so that they meet the R_1 << 97 k and R_2 << 40 k relations, you get simpler equations for determining the detection voltage.

$$\text{Detection voltage } V_{SAL} \fallingdotseq \frac{R_A + R_B}{R_B} \times V_{SB} \quad [V]$$ (At a falling value of V_{CC})

$$\text{Detection voltage } V_{SAH} \fallingdotseq \frac{R_A + R_B}{R_B} \times (V_{SB} + V_{HYSB}) \quad [V]$$ (At a rising value of V_{CC})

Note: The minimum of power voltage for the MB3771 is 3.5 V. Therefore, you must set a detection value higher than 3.5 V. The method of external adjustment using either R_1 or R_2 is not recommended because of poor accuracy in detection voltage.

2.1.2 Details of Calculating External Fine-tuning Types (calculating maximum value)

Table 1. Details of Calculating External Fine-tuning Types (calculating maximum value)

Parameter		Typ.	Numerical Values for Maximum Calculation
Resistance	R_1	9.1 k	9.191 k (+1 %)
	R_2	3.3 k	3.267 k (-1 %)
	R’	97 k	126.1 k (30 %)
	R’’	40 k	51.2 k (28 %): Relative accuracy of at least 2 %
Combined resistance	$R_A = \frac{R_1 \cdot R'}{R_2 + R'}$ *1	8.3195	$\frac{9.191 \cdot 126.1}{9.191 + 126.1} = 8.5666$
	$R_B = \frac{R_2 \cdot R''}{R_2 + R''}$ *2	3.0485	$\frac{3.267 \cdot 51.2}{3.267 + 51.2} = 3.0710$
	$\frac{R_A + R_B}{R_B}$ *3	3.7290	$\frac{8.5666 \cdot 3.0710}{3.0710} = 3.7895$
Reference voltage	V_{SB} (Reference)	1.230 V	1.248 V (Standard value)
	V_{HYSB} (Hysteresis)	0.028 V	0.042 V (Standard value)
Detection voltage *4	V_{SAL}	4.59 V	3.7895 × 1.248 = 4.729 V
	V_{SAH}	4.69 V	3.7895 × (1.248?0.042) = 4.888 V

*1: R_A becomes the maximum when R_1 and R' are the maximum.

*2: R_B becomes the minimum when R_2 and R" are minimum.

*3: (R_A + R_B) / R_B becomes the maximum when R_A is the maximum, and R_B is minimum.

*4: If fluctuations in reference and hysteresis are not considered, the values of V_{SAL} and V_{SAH} may be calculated as follows.

V_{SAL} = 3.7895 × 1.23=4.66 V

V_{SAH} = 3.7895 × (1.23 + 0.028) = 4.77 V

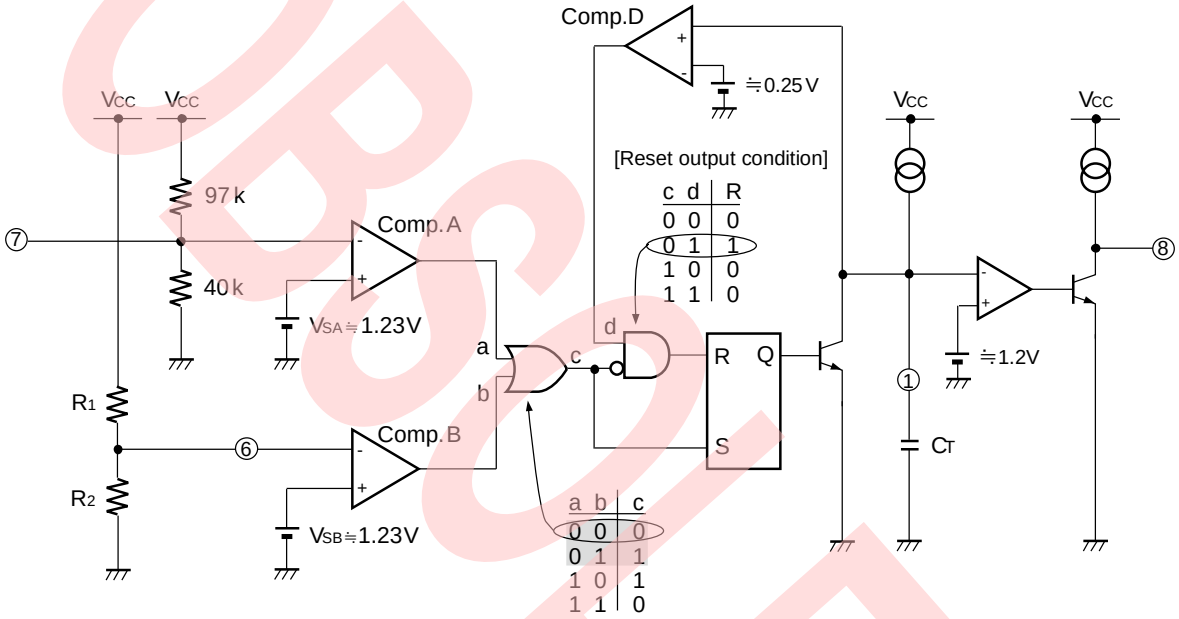
2.2 Monitoring Arbitrary Power Voltage (for V_{CC} smaller than or equal to 18 V Relationship)

This section describes how to monitor the power voltage in the V_{CC} smaller than or equal to 18 V range by means of the MB3771. As the boundary is V_{CC} = 4.45 V, pin 7 is handled differently in the following method.

Related data sheet (s): Application Examples-Arbitrary Voltage Supply Monitor Case (V_{CC} smaller than or equal to 18 V)

Monitoring Arbitrary Power Voltage (for V_{CC} smaller than or equal to 18 V relationship)

Figure 34. Result not Close to the Setting



Only when outputs from comparators A and B (Comp. A and Comp. B) are both at the L level, the reset will provide an H output. When monitoring arbitrary power voltage under the V_{CC} smaller than or equal to 18 V relationship, you should set the output of Comp. A so that it will always remain at the L level; Comp. B is responsible for monitoring the voltage.

The value of V_{SAH} is required to be 4.45 V (maximum) under the temperature conditions: Ta = - 40°C to + 85°C. At a V_{CC} value of at least 4.45 V, Comp. A will always provide an output at the L level, even if temperature fluctuations are taken into account (this means that at V_{CC} smaller than or equal to 4.45 V, Comp. A will be ineffective). Therefore, pin 7 can be made open if the detection voltage is set at 4.45 V or a higher value.

In case the detection voltage is lower than 4.45 V, it is necessary to connect pin 7 to V_{CC} so that only the output of Comp. B will be effective (The output of Comp. A may be nullified by setting pin 7 at a value higher than the V_{SA} voltage).

The detection voltage may be calculated as follows.

$$\text{Detection voltage} = \frac{R_1 + R_2}{R_2} \times V_{SB} \quad [V]$$

V_{SB} : At a falling value of V_{CC} 1.23 V (Typ.)
At a rising value of V_{CC} 1.23 V (Typ.) + 28 mV (Hysteresis equivalent)

Note: The minimum of power voltage for the MB3771 is 3.5 V. Therefore, you must set a detection value higher than 3.5 V.

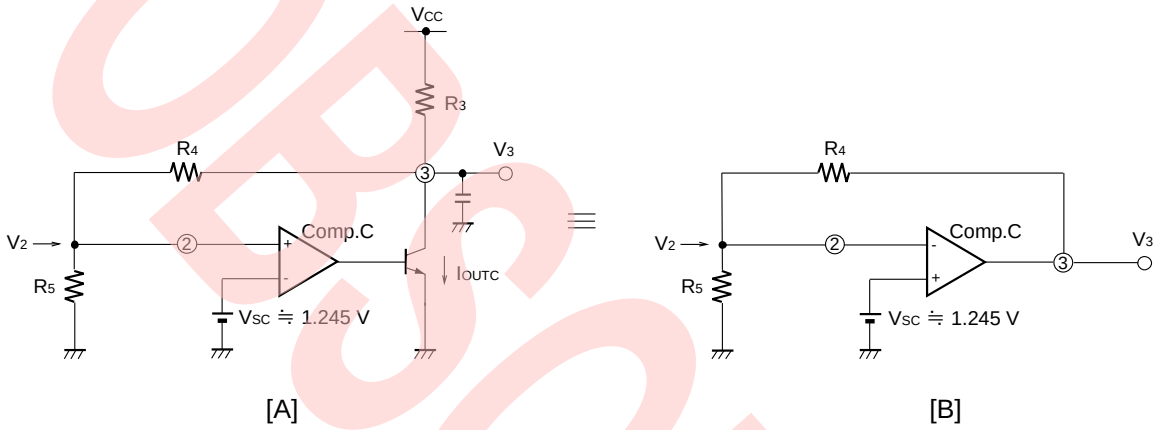
2.3 Monitoring Arbitrary Power Voltage (for 5 V constant voltage output)

This section describes how to provide an output of 5 V constant voltage by means of the MB3771.

Related data sheet (s): Application Examples - Arbitrary Voltage Supply Monitor Case (V_{CC} > 18 V)

Monitoring Arbitrary Power Voltage (for 5V constant voltage output)

Figure 35. Equivalent Circuit for Providing Constant Voltage Output



In Figure 35 [A], comparator C (Comp. C) is used as an operational amplifier to produce a constant voltage output. Because of an open collector output, the transistor is given an R_3 pullup. The output capacitor is used to reduce ripples.

See Figure 35 [B], which shows an equivalent circuit of [A]; it is a constant voltage power circuit (By equivalent, it means that pin 3 provides an output at the L level when the voltage at pin 2 is higher than V_{SC}). The relationship between V_2, the voltage at pin 2 and V_3, the voltage at pin 3, is as follows.

$$V_3 = V_2 \times \left(1 + \frac{R_4}{R_5}\right) \quad [V]$$

For example, when R_4 is 100 kΩ and R_5 is 100 kΩ, V_3 is nearly equal to 5 V. The value of V_3 is usually used as the power voltage for the MB3771.

How to Determine R3 (when VCC = 140 V)

In Figure 35 [A], the transistors output current I_{OUTC} is set at a maximum of 6 mA. It is necessary to determine a resistance value that will prevent the output current from exceeding the maximum value even at a maximum value of V_{CC}

$$(140\ V - 5\ V) / 6\ mA \approx 22.5\ [k\Omega]$$

Therefore, the value of R_3 should be set to at least 22.5 kΩ.

Because the maximum of resistance depends on the output current, you should consider load conditions when attempting to set an optimum value.

When R_3 is 110 kΩ, for example, the value of a current flowing through R_3 is as follows.

$$(140\ V - 5\ V) / 110\ k\Omega \approx 1.2\ [mA]$$

To obtain constant voltage on a stable basis, it is also necessary to set the current flowing out at pin 3 to a value not higher than 0.2 mA by considering the values of I_{OUTC} and I_{CC}.

2.4 Monitoring Power Voltages of 5 V and 12 V

This section describes how to monitor the power voltages of 5 V and 12 V by means of the MB3771.

Related data sheet (s): Block Diagram;

Application Examples – 5 V and 12 V Power Supply Monitor

Monitoring 12 V Power Voltage

Figure 36. Equivalent Circuit for Monitoring 12 V Power Voltage (when voltage at pin 2 is higher than 1.245 V)

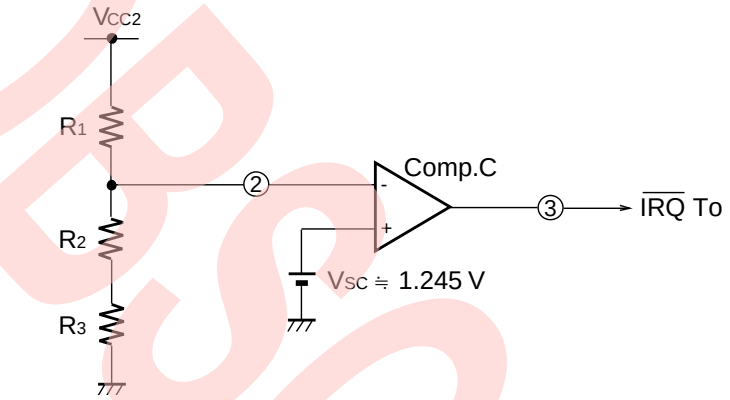
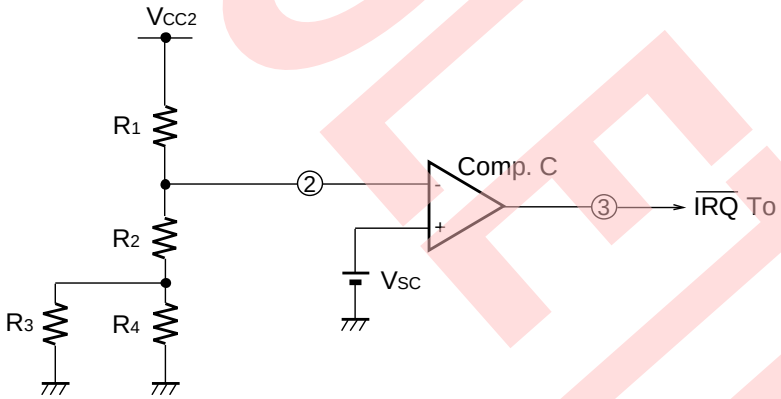


Figure 37. Equivalent Circuit for Monitoring 12 V Power Voltage (when voltage at pin 2 is lower than 1.245 V)



When the voltage at pin 2 is higher than 1.245 V, the output of Comp. C in the Diagram data sheet changes to the H level. Because the internal transistor at pin 3 is turned on, the output at pin 3 changes to the L level. In this case, the external transistor shown in the Application Examples data sheet is turned off and an equivalent circuit shown in Figure 36 is applicable.

The detection voltage may be expressed by the following equation.

$$V_{SCL} = \frac{R1 + R2 + R3}{R2 + R3} \times V_{SC}$$

When the voltage at pin 2 is lower than 1.245 V, the output of Comp. C in the Diagram data sheet changes to the L level. Because the internal transistor at pin 3 is turned off, the output at pin 3 changes to the H level. In this case, the external transistor shown in the Application Examples data sheet is turned on and an equivalent circuit shown in Figure 37 is applicable.

The detection voltage may be expressed by the following equation.

$$V_{SCH} = \frac{R_1 + R_2 + R_3 // R_4}{R_2 + R_3 // R_4} \times V_{SC}$$

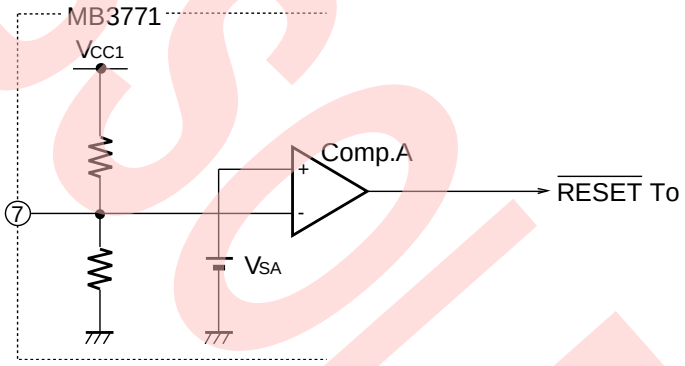
The hysteresis width V_{HYSC} may be expressed by the following equation.

$$V_{HYSC} = V_{SCH} - V_{SCL}$$
$$= \frac{R_4 (R_3 - R_3 // R_4)}{(R_1 + R_2)(R_2 + R_3 // R_4)} \times V_{SC}$$

Monitoring 5 V Power Voltage

Comp. A is responsible for monitoring the 5 V power voltage.

Figure 38. Equivalent Circuit for Monitoring 5 V Power Voltage



2.5 Monitoring Power Voltage with Delayed Trigger

This section describes how to monitor the power voltage with a delayed trigger by means of the MB3771.

Related data sheet(s): Application Examples - Power Supply Monitor with Delayed Trigger

Monitoring Power Voltage with Delayed Trigger

Figure 39. Equivalent Circuit for Monitoring Power Voltage with Delayed Trigger

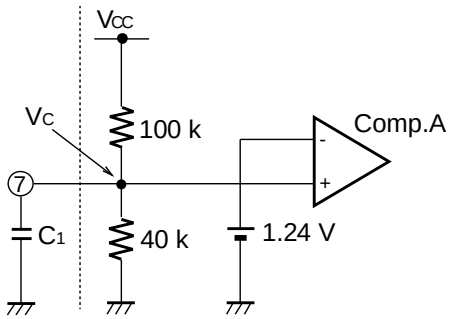
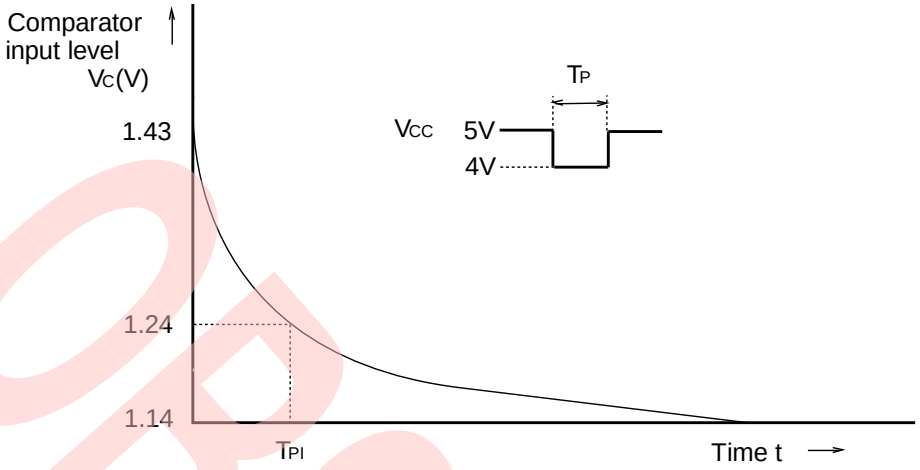


Figure 40. Change in Voltage Level at Pin 7



When the value of V_{CC} changes from 5 V to 4 V, a part of the charge stored in capacitor C is discharged to GND through the 40 kΩ resistor (refer to Figure 39).

The voltage level at pin 7 changes as shown in Figure 40. The detection time TPI may be determined by equation (b).

It is possible to calculate the comparators input voltage VC from equation (a).

$$V_C = \left(\frac{40\ k}{100\ k + 40\ k} \times 5\ V - \frac{40\ k}{100\ k + 40\ k} \times 4\ V \right) \times e^{-tpl\ /\ 40\ k.\ C1} + \frac{40\ k}{100\ k + 40\ k} \times 4\ V \quad \text{--- (a)}$$

Using equation (a), TPI may be expressed as follows.

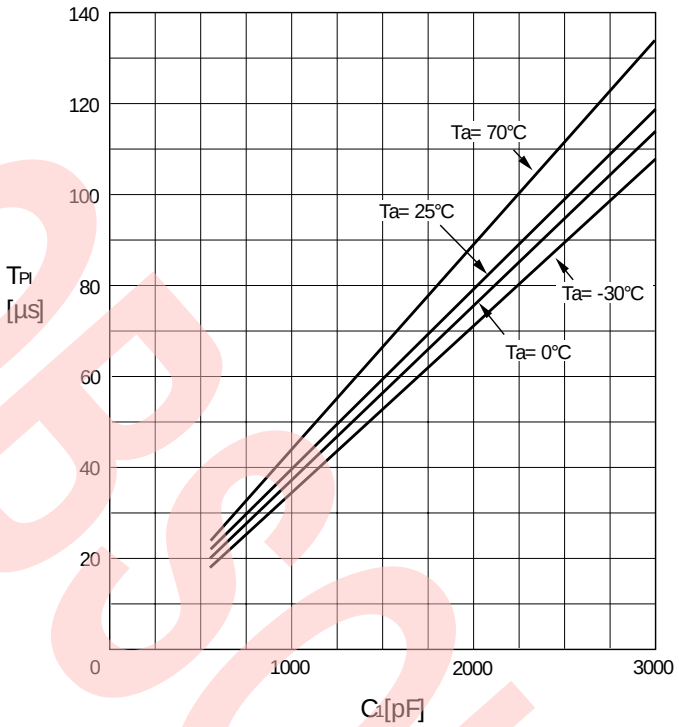
$$T_{PI}\ [\mu s] \approx 4 \times 10^{-2} \times C_1 \quad \text{--- (b)}$$

[Example]

When C1 is 1000 pF, TPI is equal to 40 µs.

Tip: Measurements of detection time TPI are plotted below. It should be noted that these are for reference only; they are not guaranteed values. (Potentially, the diffused resistor has a fluctuation of plus or minus 20 % and the reference voltage has a fluctuation of plus or minus 5 %; therefore, it is necessary to allow TPI a fluctuation of plus or minus 30 % in addition to the C1 fluctuation).

Figure 41. Measurements of Detection Time TPI (reference only)



2.6 Monitoring Negative Power Supply

This section describes how to monitor the negative power supply by means of the MB3771.

Related data sheet(s): Application Examples - 5V and Arbitrary Negative Voltage Monitor

Monitoring Negative Power Supply

Figure 42. Equivalent Circuit for Monitoring Negative Power Supply [1]

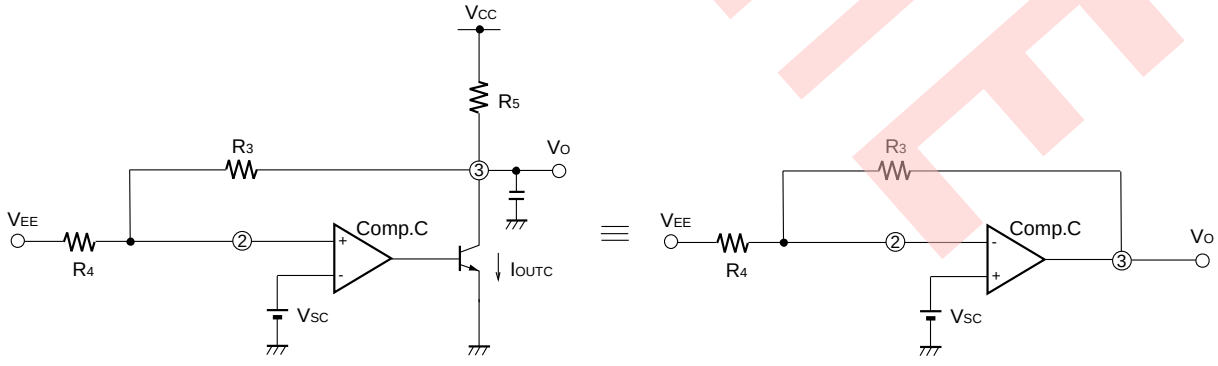
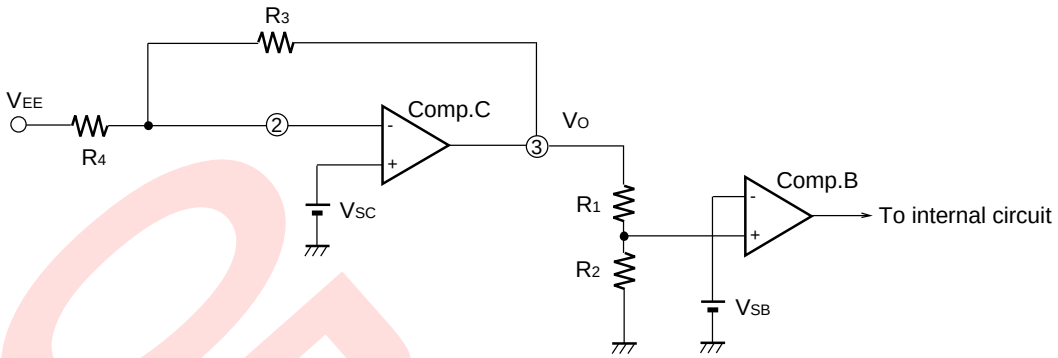


Figure 43. Equivalent Circuit for Monitoring Negative Power Supply [2]



In Figure 42 [A], Comp. C is used as an operational amplifier. Because of an open collector output, the transistor is given an R_5 pull-up. The output capacitor is used to reduce ripples.

See Figure 42 [B], which shows an equivalent circuit of [A]; it is a reverse amplifier circuit. Using V_{SC} as the threshold voltage of Comp. C and V_{SL} as the detection value for the negative power supply V_{EE}, the output V_O (voltage at pin 3) of Comp. C may be expressed by the following equation.

$$V_O = V_{SC} - \frac{(V_{SL} - V_{SC})}{R_4} \times R3\ [V] \quad ---(a)$$

As shown in Figure 43, R_1 and R_2 are used to divide the V_O voltage and the resulting values are detected by Comp. B. Using V_{SB} as the threshold voltage of Comp. B, V_O may be expressed as follows.

$$V_O = \frac{R_1 + R_2}{R_2} \times V_{SB}\ [V] \quad ---(b)$$

Let's assume that $R_1 = R_2 = R_3$ and that V_{SB} is nearly equal to V_{SC}. From equations (a) and (b), V_{SL} may be expressed as follows.

$$\boxed{V_{SL} = V_{SB}(1 - R_4 / R_3)\ [V]}$$

V_{SB} : At a falling value of V_{CC} 1.23 V
At a rising value of V_{CC} 1.23 V + 28 mV

[Example]

Let's use the following conditions: $R_1 = R_2 = R_3 = 20$ kΩ; $R_4 = 183$ kΩ; and $V_{SB} = 1.23$ V. In this case, the detection voltage V_{SL} is equal to -10 V.

2.7 Generating Reference Voltage and Monitoring Voltage Drops [1]

This section describes how to generate reference voltage and monitor voltage drops by means of the MB3771.

Related data sheet (s): Application Examples - Reference Voltage Generation and Voltage Sagging Detection - 9V Reference Voltage Generation and 5V/9V Monitoring.

Application Examples - Reference Voltage Generation and Voltage Sagging Detection - 5V Reference Voltage Generation and 5V Monitoring.

2.7.1 Generating 9 V and Monitoring 5 V/9 V

Figure 44. Equivalent Circuit for Reference Voltage Generation and Voltage Drop Detection [1] (generating 9 V and monitoring 5 V / 9 V)

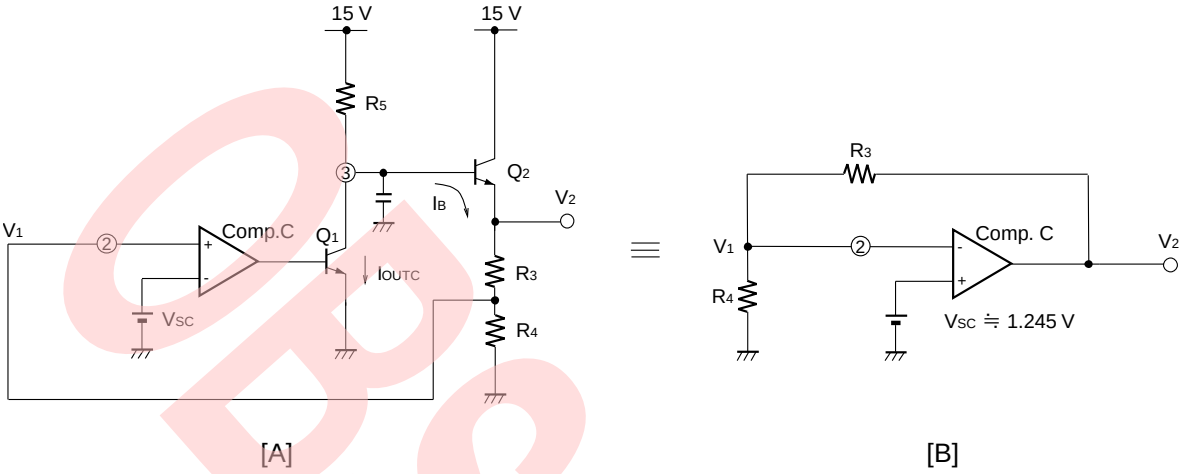
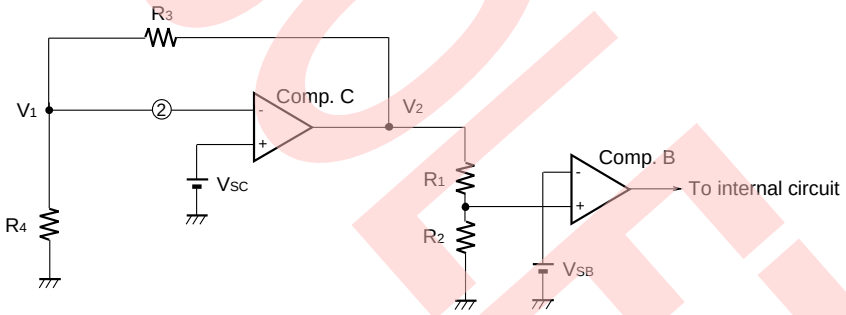


Figure 45. Equivalent Circuit for Reference Voltage Generation and Voltage Drop Detection [2] (generating 9 V and monitoring 5 V / 9 V)



In Figure 44 [A], Comp. C is used as an operational amplifier to produce a constant voltage output. Because of an open collector output, the transistor (Q_1) at pin 3 is given an R_5 pull-up.

The external capacitor at pin 3 is used to reduce ripples.

I_{OUTC} is specified up to 6 mA. Therefore, R_5 should be set to higher than 25 kΩ resistor under 15 V/6 mA condition.

See Figure 44 [B], which shows a simpler equivalent circuit of [A]; it is a low voltage power circuit. Using V_1 as the voltage at pin 2 and V_2 as the output voltage, the following equation applies.

$$V_2 = V_1 \bullet (1 + R_3 / R_4)\ [V]$$

[Example]

Let's use the following conditions: R_3 = 7.5 kΩ; R_4 = 1.2 kΩ; and V_{SC} = 1.245 V. Because V_2 is nearly equal to 9 V, the value of V_2 gives a 9 V output.

See Figure 44, in which Comp. B is used to detect divided voltage of the V_2 output from the constant voltage power circuit shown in Figure 44 [B]. The detection voltage V_{2SL} for V_2 may be expressed as follows.

$$V_{2SL} = (R_1 + R_2) \bullet V_{SB} / R_2\ [V]$$

[Example]

When R_1 = 300 kΩ and R_2 = 60 kΩ, V_{2SL} is nearly equal to 7.2 V.

Regarding the Output Current

The voltage at pin 3 is equal to the sum of the V_2 voltage and the V_{BE} voltage at Q_2: that is, 9 V + 0.7 V (assumed value). Therefore, it is nearly equal to 9.7 V. As a result, the voltage drop by R_5 is as follows.

15 V - 9.7 V = 5.3 [V]

The current flowing through R_5 (= 3 kΩ) is equal to 1.7 mA by calculating 5.3 V / 3 kΩ. Therefore, the current available from V_2 may be calculated as follows.

Output current from V_2 ≈ Base current IB at Q_2 Q_{2hFE} V_2 / (R_3 + R_4) - V_2 / (R_1 + R_2)

Assuming that the value of h_{FE} at Q_2 is nearly equal to 100, the output current from V_2 may be calculated as follows.

Output current from V_2 ≈ 1.76 mA · 100 – 9 V / (8.7 kΩ) – 9 V / (62.3 kΩ) ≈ 175 [mA]

Note: For the sake of stable supply, the output current from V_2 should be up to 50 mA by considering fluctuations of the external transistor Q_2.

2.7.2 Generating 5 V and Monitoring 5 V (No. 1)

If you give the R_3 = 3.6 kΩ and R_4 = 3.6 kΩ relationships to the explanation under the item, "2.7.1 Generating 9 V and monitoring 5 V / 9 V", you find that V_2 is a 5 V output.

Note: For the sake of stable supply, the output cur6rent from V_2 should be up to 50 mA by considering fluctuations of the external transistor Q_2

2.8 Generating Reference Voltage and Monitoring Voltage Drops [2]

This section describes how to generate reference voltage and monitor voltage drops by means of the MB3771.

Related data sheet (s): Application Examples - Reference Voltage Generation and Voltage Sagging Detection 5 V Reference Voltage Generation and 5 V Monitoring (No. 2)

Application Examples - Reference Voltage Generation and Voltage Sagging Detection - 1.245 V Reference Voltage Generation and 5 V Monitoring

2.8.1 Generating 5 V and Monitoring 5 V (No. 2)

Figure 46. Equivalent Circuit for Reference Voltage Generation and Voltage Drop Detection [1] (generating 5 V and monitoring 5 V)

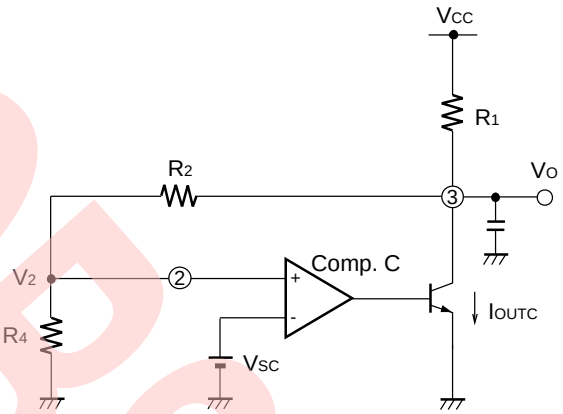
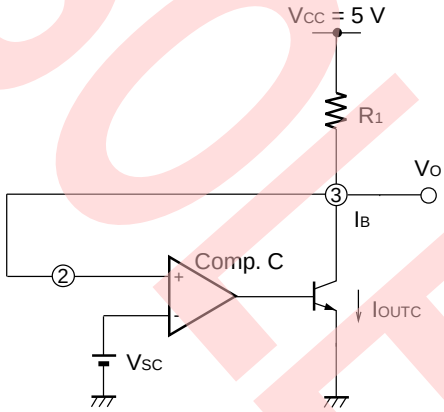


Figure 47. Equivalent Circuit for Reference Voltage Generation and Voltage Drop Detection [2] (generating 1.245 V and monitoring 5 V)



In Figure 46, Comp. C is used as an operational amplifier to produce the constant voltage output. Because of the open collector output, the transistor (Q_1) at pin 3 is given an R_1 pull-up. The output capacitor is used to reduce ripples. Using V_2 as the voltage at pin 2 and Vo as the output voltage, the following equation applies.

$$V_O = V_2 \bullet (1 + R_2 / R_3)\ [V]$$

Let's use the following conditions: R_2 = 100 kΩ; R_3 = 33 kΩ; and V_{SC} = 1.245 V. Because V_{SC} is nearly equal to V_2, the value of V_2 is nearly equal to 5 V.

[Example]

The value of I_{OUTC} is up to 6 mA according to the standard. When V_{CC} = 40 V, the value of R_1 is as follows.

$$R_1 \geq (40\ V - 5\ V) / 6\ mA \approx 5.8\ [k\Omega]$$

Taking the margin into consideration, use R_1 = 11 kΩ, the output current I is as follows.

$$I = (40\ V - 5\ V) / 6\ k\Omega \approx 3.2\ [mA]$$

For the sake of stable supply, the output current should meet the I < 1.6 mA relationship.

2.8.2 Generating 1.245 V and Monitoring 5 V

See Figure 47, which shows a voltage follower circuit. In this case, output V_O is equal to V_{SC}.

[Example]

The value of I_{OUTC} is up to 6 mA according to the standard. When V_{CC} = 5 V, the value of R_1 is as follows.

Note: See the data sheet: Application Examples - Reference Voltage Generation and Voltage Sagging Detection - 1.245 V Reference Voltage Generation and 5 V Monitoring. The 0.47 µF capacitor at pin 3 in the data sheet is intended to reduce ripples. Depending on the system, you should modify the capacitance.

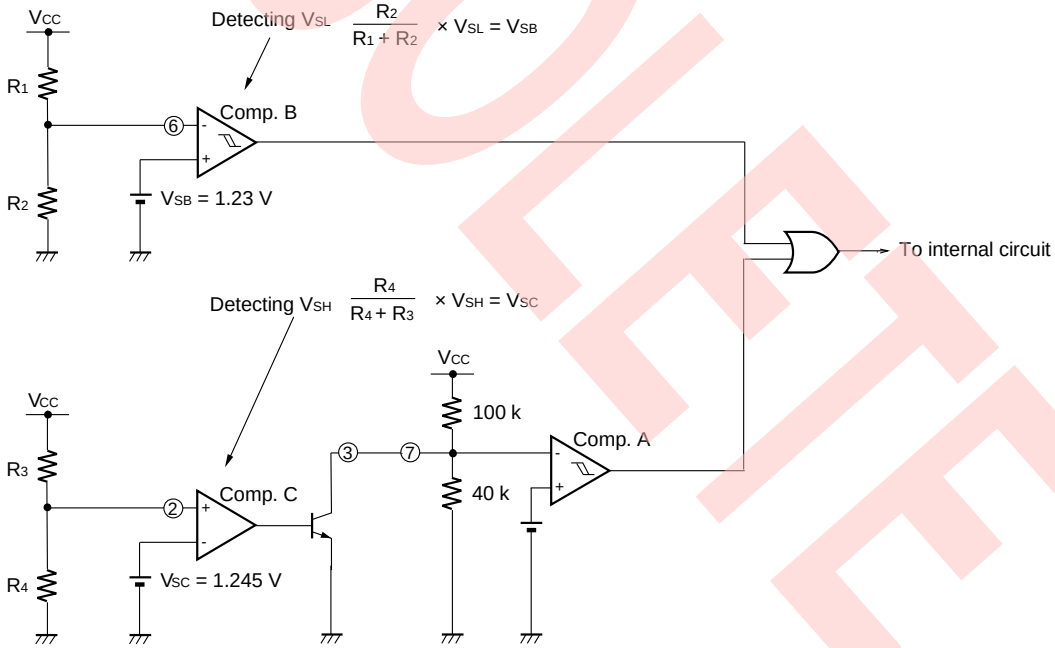
2.9 Detecting Low Voltage and Excess Voltage

This section describes how to detect any low voltage or excess voltage by means of the MB3771.

Related data sheet (s): Application Examples - Detecting Low Voltage and Excess Voltage (V_{CC} = 5 V)

Detecting Low Voltage and Excess Voltage

Figure 48. Equivalent Circuit for Detecting Low Voltage and Excess Voltage



R_1 and R_2 are used to determine the value of V_{SL}. R_3 and R_4 are used to determine the value of V_{SH}.

Comp. C has no hysteresis characteristics so that no hysteresis is given to V_{SH}.

When outputs from Comp. A and Comp. B are both at the L level, the reset will provide an H output. This assumes the $V_{SL} < V_{CC} < V_{SH}$ relationship.

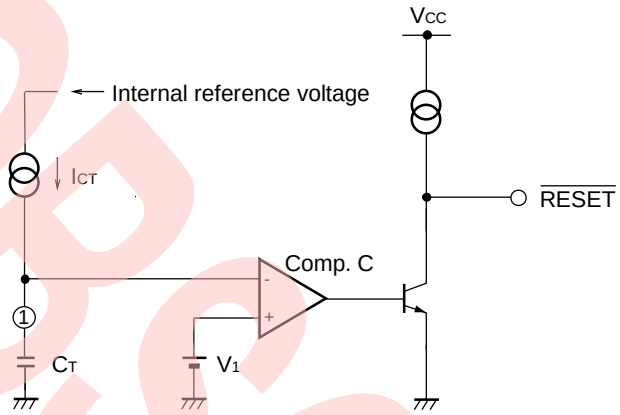
When V_{CC} exceeds the value of V_{SH}, Comp. C turns on the transistor at pin 3, reduces the voltage at pin 7 to a value close to GND, reverses the output of Comp. A, and changes the reset to the L level. If V_{CC} is not higher than the value V_{SH}, the transistor at pin 3 is off, so that pin 7 is essentially open. At a rising value of V_{CC}, therefore, you should take care when making the value of V_{SL} lower than V_{CC} (4.2V typically), which is detected by the 100 kΩ and 40 kΩ resistors.

2.10 Reset Output

This section describes how to determine the timing for rest output, as well as related fluctuations.

Reset Output

Figure 49. Equivalent Circuit for Internal Reset



The width (TPO) of the $\overline{\text{RESET}}$ output pulse may be determined as follows.

$$T_{PO} = C_T \cdot V_1 / I_{CT}$$

You can get the following equation if you use typical values: that is, the threshold value (V_1) is nearly equal to 1.24 V and the charging current (I_{CT}) at C_T is nearly equal to 1.2 µA.

$$T_{PO}\ [ms] \approx 100 \cdot C_T\ [\mu F]$$

Assuming that the value of C_T is constant, it is possible to determine the fluctuations of T_{PO} from the charging/discharging current I_{CT} and threshold voltage V_1. Fluctuations in charging/discharging current are dependent mainly on fluctuations in the diffused resistance R inside the IC and fluctuations in reference voltage, as well as errors in the hfe value of the transistors comprising the current mirror.

Meanwhile, fluctuations in threshold voltage are dependent mainly on fluctuations in resistance and reference voltage. Generally speaking, fluctuations in TC resistance are plus or minus 20 % (or 30 %) when Ta = 25 °C; they are plus or minus 40 % when Ta is between minus 40 °C and plus 85 °C. The relative error of the transistor's hfe is approximately plus or minus 10 %. For the MB3771, fluctuations in reference voltage are plus or minus 1.6 % when Ta = 25 °C; they are approximately plus or minus 3.2 % when Ta is between minus 40 °C and plus 85 °C.

Assuming that the value of C_T is constant, the values of T_{PO} may be determined as follows.

$$T_{PO}\ (min.)\ [ms] \approx (100 \cdot 0.5) \cdot C_T\ [\mu F]$$

$$T_{PO}\ (max.)\ [ms] \approx (100 \cdot 1.5) \cdot C_T\ [\mu F]$$

If the value of C_T has a fluctuation of plus or minus 20 %, the values of T_{PO} are as follows.

$$T_{PO}\ (min.)\ [ms] \approx (100 \cdot 0.5) \cdot (C_T \cdot 0.8)\ [\mu F]$$

$$T_{PO}\ (max.)\ [ms] \approx (100 \cdot 1.5) \cdot (C_T \cdot 1.2)\ [\mu F]$$

Note: If the value of C_T is decreased to reduce the time setting, it will be impossible to neglect the delay time (approximately 2 µs) occurring inside the IC. You should choose an appropriate C_T value that will involve no influence on delay time.

2.11 Handling Unused Terminals

How to handle unused terminals in the MB3771 is summarized in Table 2.

Handling Unused Terminals

Table 2. Handling Unused Terminals in the MB3771

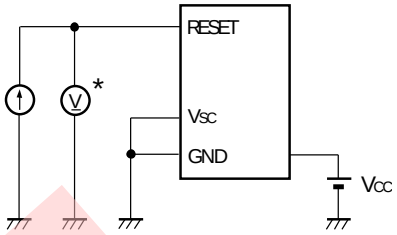
Terminal Name	Description
C_T terminal	OPEN
V_{SC} terminal	GND
OUT_C terminal	OPEN
V_{SA} / $\overline{RESIN}$ terminal	V_{CC}
V_{SA} terminal	OPEN
RESET terminal	OPEN

2.12 Q&A Set Regarding the MB3771

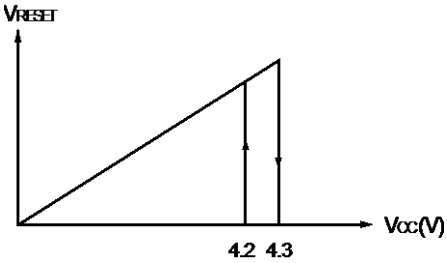
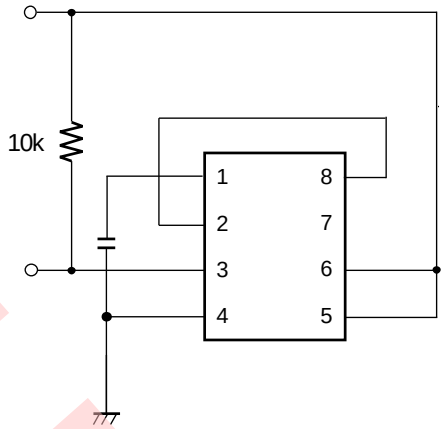
This section provides a set of questions and answers regarding the MB3771.

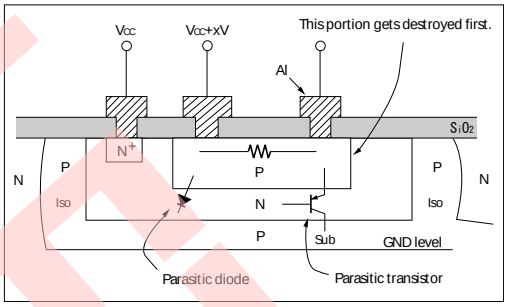
Q&A Set Regarding the MB3771

Q&A Set Regarding the MB3771			
Q1	Without V_{CC} input, voltage is sometimes found to be applied to the V_{SB} or V_{SC} terminal. Does this cause the IC to malfunction?	A1	The V_{SB} and V_{SC} terminals have nothing to with the power voltage. The maximum rating is between minus 0.3 V and plus 20 V. Applying voltage of up to 20 V will not cause a malfunction or destroy the IC. In the case of V_{SA}, however, applying a voltage higher than the value of V_{CC} plus 0.3 V or a voltage of 20 V or more would eventually destroy the unit.
Q2	Without V_{CC} input, voltage is sometimes found to be applied to the OUT_C terminal. Does this cause the IC to malfunction?	A2	The withstand voltage is up to 18 V, although there is no specific standard.
Q3	The maximum value of I_{RESET} is 20 mA according to the standard, but any surge current will temporarily cause a current of 20 mA or more. Does this cause the IC to malfunction?	A3	The potential capability is approximately twice the recommended operating conditions. No momentary short-circuit will cause any destruction or similar problem. There is no standard or guarantee regarding the current value and time constant.
Q4	I have no information concerning the definition of an output sink current. I am wondering why the electrical characteristics include 20 mA (min.) and 40 mA (typ.), although I_{RESET} is specified as 20 mA (max.) in the recommended operating conditions. The same is true of I_{OUTC}. Why is it 15 mA (typ.) in the electrical characteristics against 6 mA (max.) under the recommended operating conditions?	A4	The electrical characteristics for I_{RESET} state as follows: "When the $\overline{RESET}$ terminal encounters a short of a 1 V power supply, the value of a resulting current is typically 40 mA." By contrast, the recommended operating conditions allow a current of up to 20 mA on a constant basis. If the maximum value is exceeded, problems in reliability and/or other characteristics will result. The same is applicable to T_{OUTC}.

<table>
<tr><th colspan="4">Q&A Set Regarding the MB3771</th></tr>
<tr><td>Q5</td><td>Input current I_{ILB} is probably a current that begins to flow out at the IC when 0 V is applied to the V_{SB} terminal. If so, why does the standard specify an inflow of 20 nA (typ.)? Likewise, why does the standard specify an inflow of 50 nA (typ.) regarding I_{ILC}?</td><td>A5</td><td>The table below is the standard for flowing out. You should consider as follows.
<table>
<tr><th>Symbol</th><th>Minimum</th><th>Typical</th><th>Maximum</th><th>Unit</th></tr>
<tr><td>I_{ILB}</td><td>-250</td><td>-20</td><td>-</td><td>nA</td></tr>
<tr><td>I_{ILC}</td><td>-500</td><td>-50</td><td>-</td><td>nA</td></tr>
</table></td></tr>
<tr><td>Q6</td><td>What is the output delay time for V_{SA}?</td><td>A6</td><td>AS with V_{SB}, the delay time is 2 µs (typ.) and 10 µs (max.).</td></tr>
<tr><td>Q7</td><td>When V_{CC} falls below 0.8 V, what is the output? And how does the IC work internally?</td><td>A7</td><td>At a V_{CC} value of 3.5 V or less, what is guaranteed is only the L output for the reset. Nobody knows how the IC operates internally. The L output for the reset guarantees a V_{CC} value of up to 1.2 V. At a V_{CC} value of 1.2 V or less, the $\overline{\text{RESET}}$ terminal is state of high impedance, and the output voltage becomes undefined. However, the voltage at the $\overline{\text{RESET}}$ terminal is nearly equal to V_{CC} in the experiment on the undermentioned circuit chart when V_{CC} = 0.8 V (typ.); the conditions are shown below. Also refer to the data sheet: Standard Characteristic Curves - Output ($\overline{\text{RESET}}$) Voltage vs. Power Voltage.
 

V_{CCL}: It is the value of V_{CC} available when the * portion in the diagram has reached 0.4 V.</td></tr>
<tr><td>Q8</td><td>At a power voltage of 0 V, what is the status of the $\overline{\text{RESET}}$ terminal?</td><td>A8</td><td>At a power voltage of 0 V, the $\overline{\text{RESET}}$ terminal provides a voltage of 0 V, which is high impedance. Until the value of V_{CC} goes up to approximately 0.8 V (1.2 mA maximum), the voltage at the $\overline{\text{RESET}}$ terminal also increases (because the internal transistor fails to be turned on if the value of V_{CC} is too low).</td></tr>
<tr><td>Q9</td><td>What is the standard about the L output level for the $\overline{\text{RESET}}$ terminal?</td><td>A9</td><td>It is V_{OLR}. Refer to the data sheet: Standard Characteristic Curves - Output ($\overline{\text{RESET}}$) Voltage vs. Output Current (V_{OLR} - I_{RESET}).</td></tr>
<tr><td>Q10</td><td>How do you measure the output delay time (tPD)? What is its potential value?</td><td>A10</td><td>You can measure the delay in reset output while turning on and off pin 6 by referring to the data sheet: Application Examples - Using Forced Reset. The potential value ranges from minus 50 % to 100 % (from 1 µs to 4 µs).</td></tr>
<tr><td>Q11</td><td>What is the behavior of t_{PO} in the data sheet: Application Examples - Using Forced Reset?</td><td>A11</td><td>The same time output of t_{PO} is produced either when the power supply is turned on or when there is a forced reset (using V_{SB} terminal). T_{PO} [ms] = C_T [µs] × 10^2</td></tr>
</table>

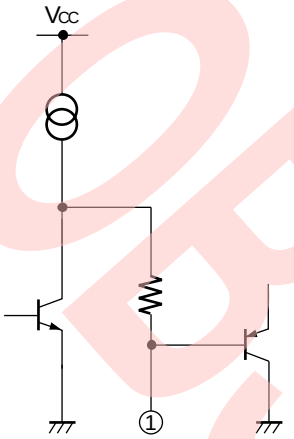
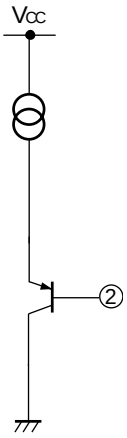
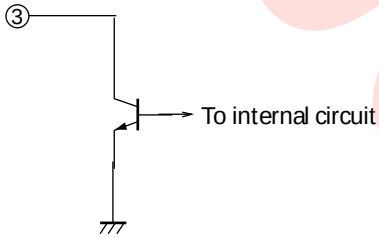
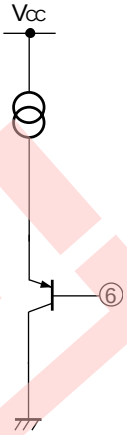
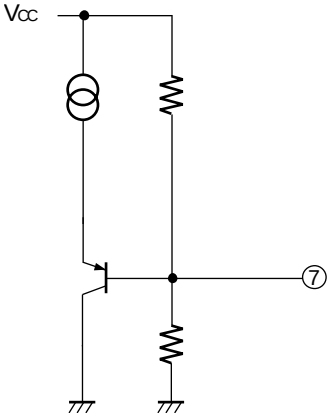
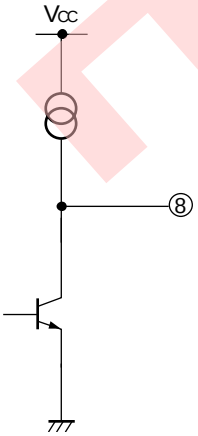
Q&A Set Regarding the MB3771			
Q12	How is the reset output in the data sheet: Application Examples - Non-reverse Reset Output?	A12	Pin 8 operates the same way as mentioned in the data sheet's Basic Operation. Pin 3 provides a reverse output against Pin 8.  
Q13	How is the delay time when you use the Non-reverse Reset Output?	A13	It is the sum of the delay time in Comp. A and the delay time in Comp. C.
Q14	Is it possible to monitor another power supply whose GND is isolated from the MB3771?	A14	It is not possible to monitor any power supply not sharing GND, because the MB3771 monitors the comparator input voltage with respect to its own GND.
Q15	Why is the detection voltage set at 4.2 V?	A15	Most microcomputers involve recommended operating conditions including a power voltage of 5 V plus and minus 10 %. Because no reset output should be produced at 4.5 V, the upper limit of V_{SAH} must be not higher than 4.5 V. Our value setting was made by giving some allowance to the above value and by assuming that a microcomputer itself will potentially withstand 4.2 V. You should use an external resistor that meets the system requirements.

Q&A Set Regarding the MB3771			
Q16	When used alone, ICs will work normally. When they are assembled into a system, however, the $\overline{\text{RESET}}$ terminal will remain at the L level (or show an unstable operation). What are probable causes? And how can you remove them?	A16	1. Because the reset terminal on the system side has a low impedance, there may be an excess pull against the current. Also refer to the data sheet: Standard Characteristic Curves - Output ($\overline{\text{RESET}}$) Voltage vs. Output Current (V_{OLH} - I_{OH}). If this occurs, you can remove the problem by giving a resistor pull-up to the $\overline{\text{RESET}}$ terminal. The resistance is determined by the potential current of the reset output transistor. You should choose a resistance level that will prevent the maximum current from exceeding 20 mA. 2. Additionally, there may have been a malfunction under the influence of power noise resulting from microcomputers or other components. In this case, you can reduce the noise-caused momentary voltage drop by either taking the delay trigger method or inserting a bypath capacitor (approximately 0.1 µF) between the IC's power terminals.
Q17	What will happen if you apply a voltage equal to or higher than V_{CC} to V_{SA}?	A17	At the V_{SA} terminal, a resistor is used to divide the V_{CC} voltage. In case the resistor receives any voltage equal to or higher than V_{CC}, the separated conjunction will degrade, resulting in a forward current flowing to V_{CC}. Remember that this will eventually cause an IC malfunction. 

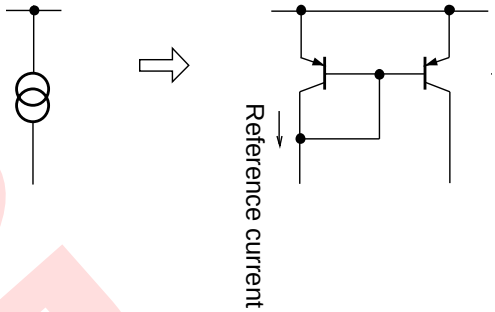
2.13 Equivalent Circuits for MB3771 Input / Output Unit

The following are equivalent circuits for the MB3771 input/output unit.

Equivalent Circuits for MB3771 Input / Output Unit

<table>
<tr>
<td><C_T terminal>
 
</td>
<td><V_{SC} terminal>
 
</td>
</tr>
<tr>
<td><OUT_C terminal>
 
</td>
<td><V_{SB} / $\overline{RESIN}$ terminal>
 
</td>
</tr>
<tr>
<td><V_{SA} terminal>
 
</td>
<td><$\overline{RESET}$>
 
</td>
</tr>
</table>

Note: A circuit having current symbols is a constant current circuit of the current mirror type using PNP transistors, as shown below.



3 MB3773 Applications

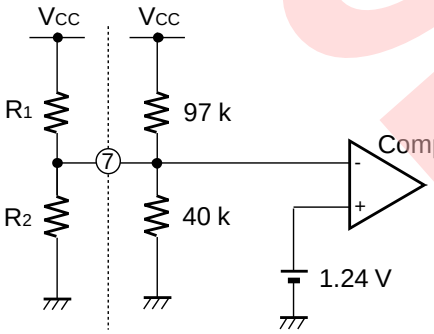
3.1 Equations for Calculating External Fine-tuning Types

It is possible to externally adjust the VSA detection voltage.

Related data sheet(s): Application Examples - Power Supply Monitor with External Adjustment

Equations for Calculating External Fine-tuning Types

Figure 50. Equivalent Circuit for Calculating External Fine-tuning Types



Note: The internal IC resistance is plus or minus 30 % in absolute accuracy and plus or minus 2 % in relative accuracy (potential capability: 1 %).

In Figure 50, R_A is a combined resistance between the 97 kΩ and external R_1 resistance; R_B is a combined resistance between the 40 kΩ and external R_2 resistance.

$$R_A = R_1 \cdot 97\ k\Omega / (R_1 + 97\ k\Omega)\ [\Omega]$$

$$R_B = R_2 \cdot 40\ k\Omega / (R_2 + 40\ k\Omega)\ [\Omega]$$

The detection voltage may be calculated as follows.

$$\text{Detection voltage } V_{SL} = \frac{R_A + R_B}{R_B} \times V_S \quad [V]$$ (At a falling value of V_{CC})

$$\text{Detection voltage } V_{SH} = \frac{R_A + R_B}{R_B} \times (V_S + V_{HYS}) \quad [V]$$ (At a rising value of V_{CC})

The above calculation assumes that the threshold level of comparator S is V_S = 1.23 V (typ.) and that the width of hysteresis is V_{HYS} = 28 mV (typ.).

If you choose appropriate values of R_1 and R_2 so that they meet the R_1 << 97 kΩ and R_2 << 40 kΩ relations, you get simpler equations for determining the detection voltage.

$$\text{Detection voltage } V_{SL} \fallingdotseq \frac{R_1 + R_2}{R_2} \times V_S \quad [V]$$ (At a falling value of V_{CC})

$$\text{Detection voltage } V_{SH} \fallingdotseq \frac{R_1 + R_2}{R_2} \times (V_S + V_{HYS}) \quad [V]$$ (At a rising value of V_{CC})

Note: The minimum of power voltage for the MB3773 is 3.5 V. Therefore, the detection voltage you are setting must be higher than 3.5 V. The method of external adjustment using either R_1 or R_2 is not recommended because of poor accuracy in detection voltage.

3.2 Monitoring Power Voltage with Delayed Trigger

This section describes how to monitor the power voltage with a delayed trigger by means of the MB3773.

Related data sheet(s): Application Examples - Power Supply Monitor with Delayed Trigger

Monitoring Power Voltage with Delayed Trigger

Figure 51. Equivalent Circuit for Monitoring Power Voltage with Delayed Trigger

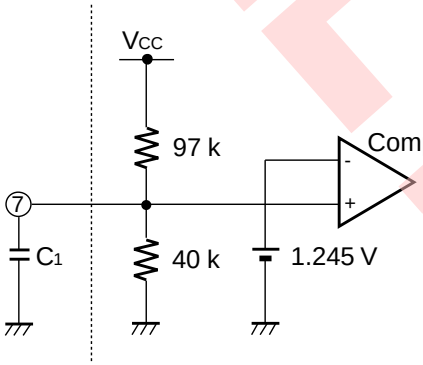
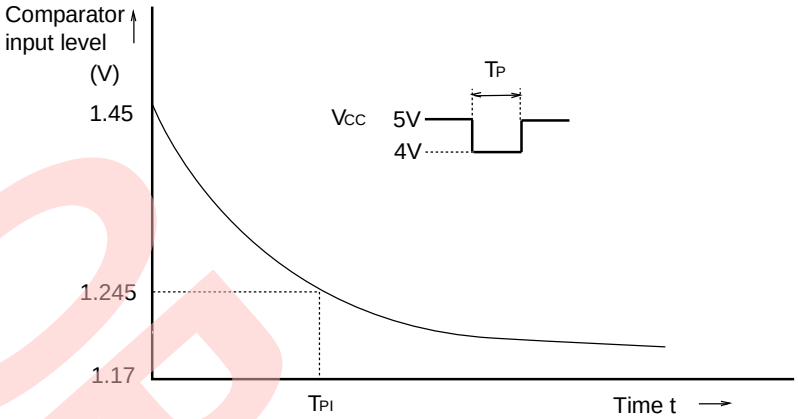


Figure 52. Change in Voltage Level at Pin 7



When the value of V_{CC} changes from 5 V to 4 V, part of the charge stored in capacitor C is discharged to GND through the 40 kΩ resistor (refer to Figure 51).

The voltage level at pin 7 changes as shown in Figure 52. The detection time TPI may be determined by the following equation.

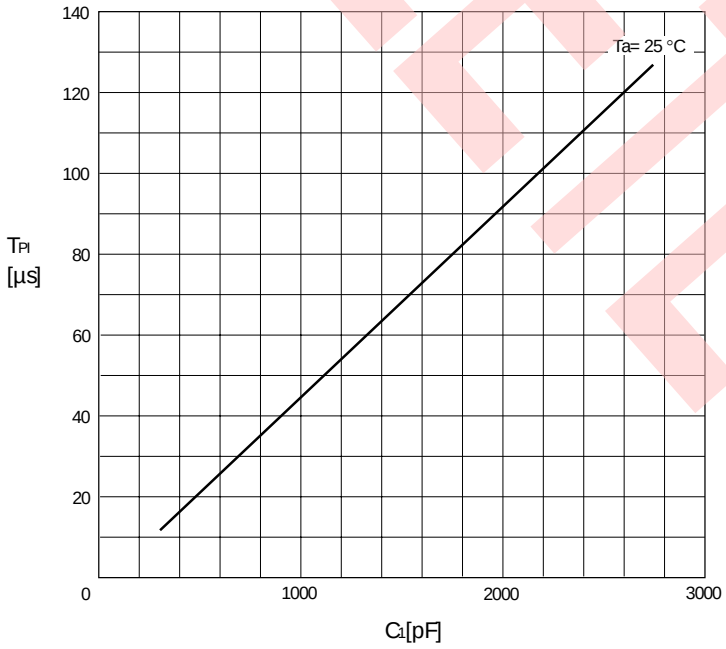
$$TPI\ [\mu s] \approx 5 \cdot 10\text{-}2 \cdot C1\ [pF]$$

[Example]

When C_1 = 1000 pF, T_{PI} is equal to 50 µs.

Tip: Measurements of detection time T_{PI} are plotted below. It should be noted that these are for reference only; they are not guaranteed values.

Figure 53. Measurements of Detection Time T_{PI} (reference only)

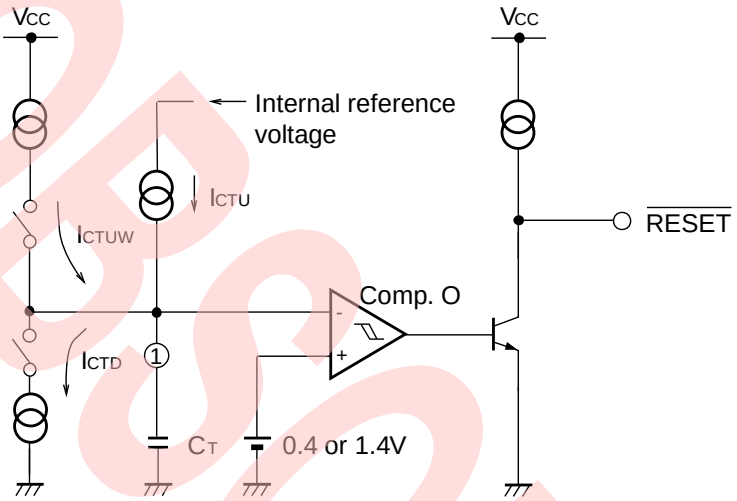


3.3 Equations for Calculating Timing Setting and Related Fluctuations

This section describes how to determine the timing for power-rising reset hold time (T_{PR}), watch-dog timer monitor time (T_{WD}), and watch-dog timer reset time (T_{WR}), as well as related fluctuations.

Equations for Calculating Timing Setting and Related Fluctuations

Figure 54. Equivalent Circuit for Internal Reset



The values of T_{PR}, T_{WD}, and T_{WR} may be determined by the following equations.

$$T_{PR} = C_T \times V_1 / I_{CTU}$$

$$T_{WD} = C_T \times (V_1 - V_2) / I_{CTD}$$

$$T_{WR} = C_T \times (V_1 - V_2) / I_{CTUW}$$

If you use typical values shown in, you can get the following equations.

$$T_{PR}\,[ms] \fallingdotseq 1000 \times C_T\,[\mu F]$$

$$T_{WD}\,[ms] \fallingdotseq 100 \times C_T\,[\mu F]$$

$$T_{WR}\,[ms] \fallingdotseq 20 \times C_T\,[\mu F]$$

Table 3. Typical Values

Parameter	Typical Value
Rising threshold voltage	V_1 = 1.4 V
Falling threshold voltage	V_2 = 0.4 V
Power-ON reset charging current	I_{CTU} = 1.2 µA
Watch-dog timer discharging current	I_{CTD} = 10 µA
Watch-dog timer charging current	I_{CTUW} = 50 µA

Assuming that the value of C_T is constant, it is possible to determine the fluctuations of T_{PR}, T_{WD}, and T_{WD} from the charging/discharging currents I_{CTU}, I_{CTD}, and I_{CTUW} and the threshold voltage V_1 and V_2. Fluctuations in charging/discharging current are primarily dependent on fluctuations in the diffused resistance R inside the IC and fluctuations in reference voltage, as well as errors in the hfe value of the transistors comprising the current mirror.

Meanwhile, fluctuations in threshold voltage are dependent mainly on fluctuations in resistance and reference voltage.

Generally speaking, fluctuations in IC resistance are plus or minus 20 % (or 30 %) when Ta = 25 °C; they are plus or minus 40 % when Ta is between minus 40 °C and plus 85 °C. The relative error of the transistor's hfe is approximately plus or minus 10 %. For the MB3773, fluctuations in reference voltage are plus or minus 1.5 % when Ta = 25 °C; they are approximately plus or minus 2.5 % when Ta is between minus 40 °C and plus 85 °C.

If the value of C_T has a fluctuation of plus or minus 20 %, the values of T_{PR} are as follows.

$$T_{PR}\ (\text{min.})\ [\text{ms}] \fallingdotseq (1000 \times 0.5) \times (C_T \times 0.8)\ [\mu\text{F}]$$

$$T_{PR}\ (\text{max.})\ [\text{ms}] \fallingdotseq (1000 \times 1.5) \times (C_T \times 1.2)\ [\mu\text{F}]$$

The values of TWD and TWR may be determined in the same way.

Note: If the value of C_T is decreased to reduce the time setting, it will be impossible to neglect the delay time (approximately 2 µs) occurring inside the IC. You should choose an appropriate C_T value that will involve no influence on delay time.

3.4 Configuration of CK Input Circuit Unit

This section describes how the CK input circuit unit of the MB3773 is configured.

Configuration of CK Input Circuit Unit

Figure 55 shows an equivalent circuit for detecting the falling edge in the CK signal input unit. The circuit is designed to detect the falling edge of the CK signal and transmit its pulse.

The standard value for the CK input pulse width T_{CKW} is at least 3 µs.

Figure 55. Equivalent Circuit for Detecting Falling Edge in CK Signal Input Unit

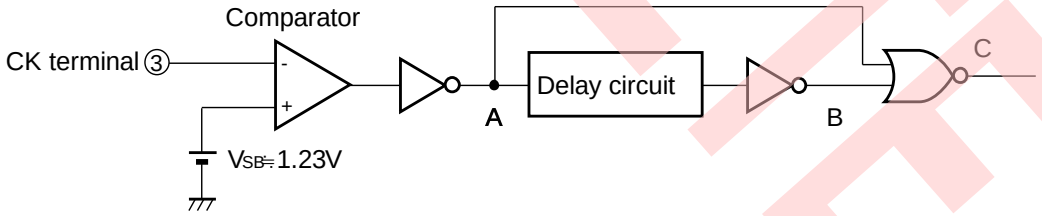
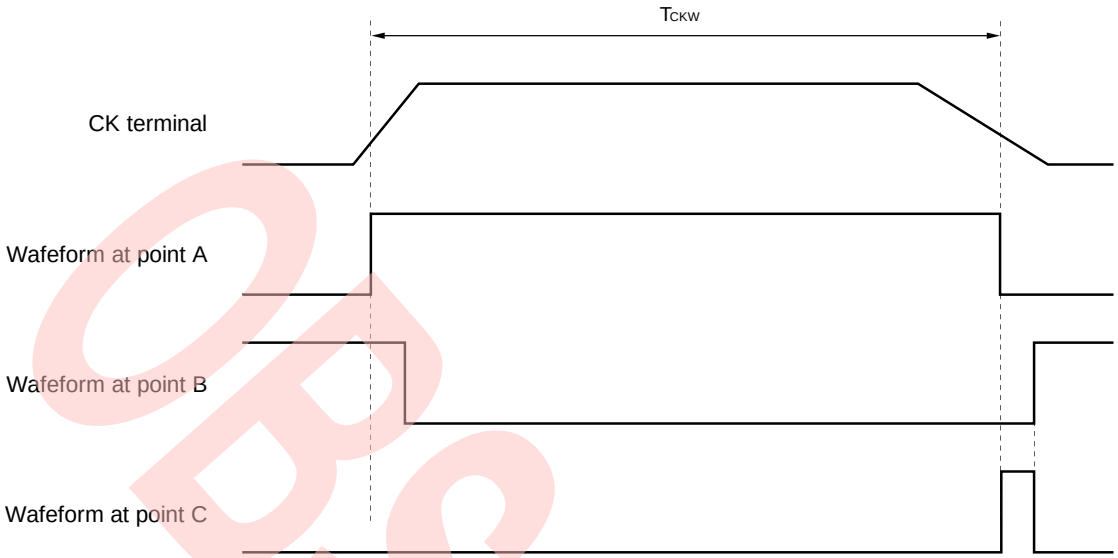


Figure 56. Equivalent Circuit for Detecting Falling Edge in CK Signal Input Unit (waveforms)



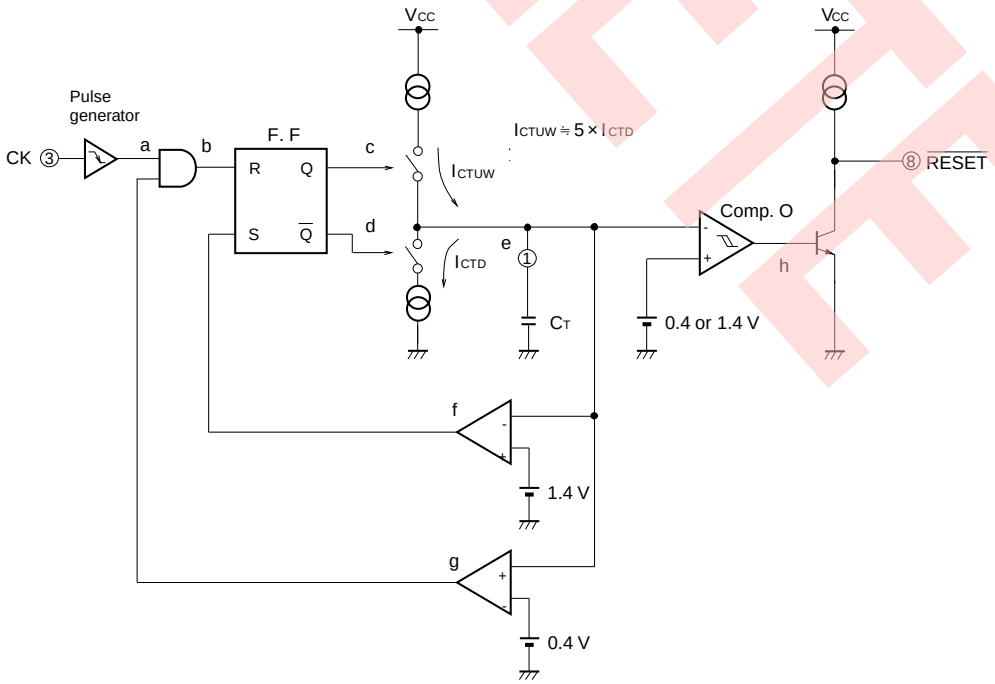
3.5 How the Watch-dog Timer Works

This section describes how the MB3773 watch-dog timer works.

How the Watch-dog Timer Works

See Figure 57, which shows an equivalent circuit for the watch-dog timer.

Figure 57. Equivalent Circuit for Watch-dog Timer

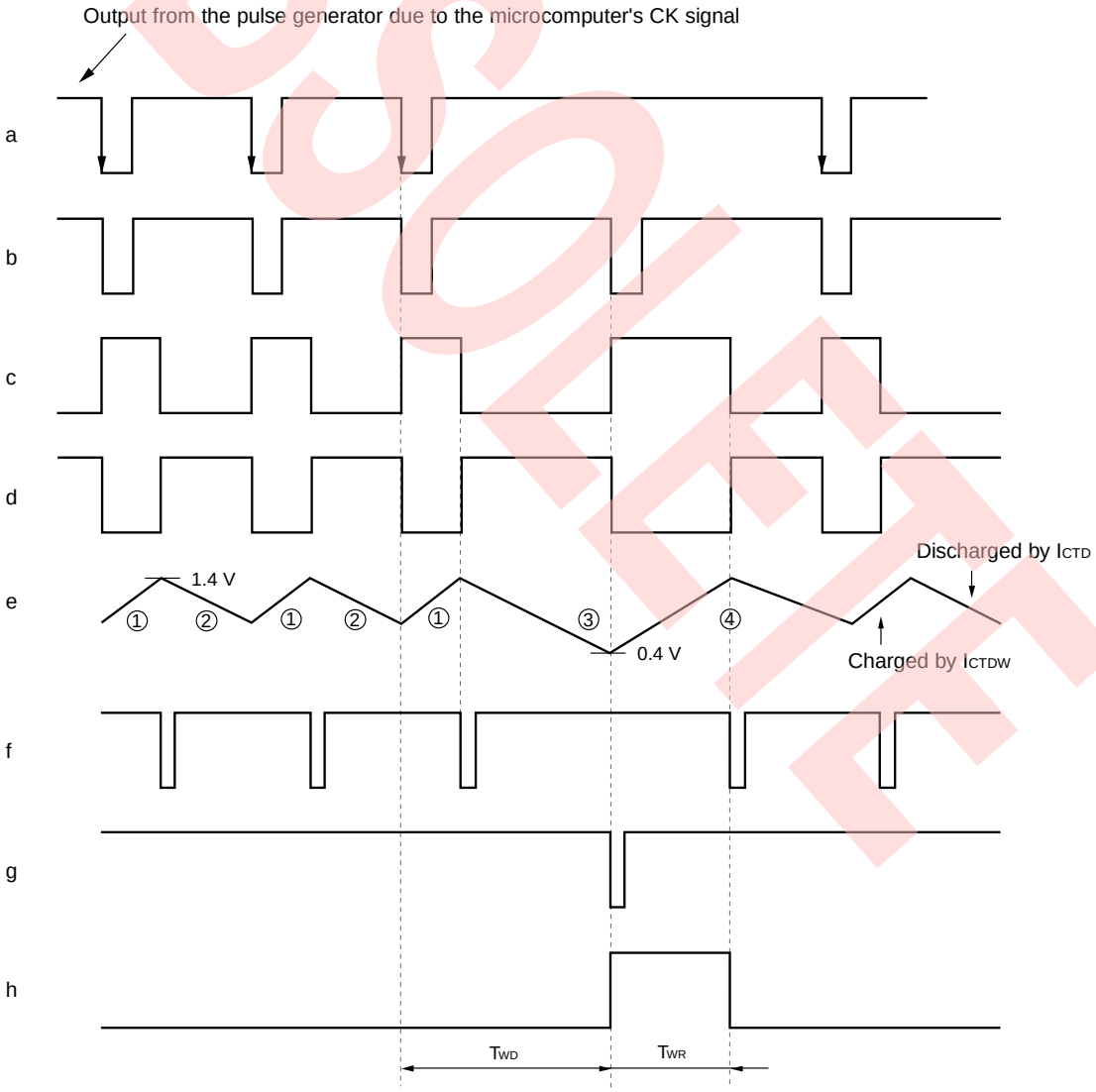


The watch-dog timer works in the following sequence.

1. When the clock input pulse changes its level from H to L, the Q output from the flipflop at point c changes its level from L to H. In turn, this turns on the upper switch and turns off the lower switch. A current, I_{CTUW}, begins to flow, thus charging the C_T element.
2. When the voltage (C_T voltage) at point e reaches 1.4 V, the level at point f changes to L. In turn, this turns on the lower switch and turns off the upper switch. A current, I_{CTD}, begins to flow, thus charging the C_T element.
3. Suppose that there is no input of clock pulses for a specified period of time. If the C_T element continues discharging until the voltage at point e lowers to 0.4 V, the level at point e changes to L, thus charging the C_T element. At this point, Comp. C produces an H output at point h, so that the level at $\overline{\text{RESET}}$ changes to L.
4. When the charging current I_{CTUW} causes the voltage at point e to rise to 1.4 V or more, the level at point h changes to L, thus canceling the reset.

A timing chart for the watch-dog timer is shown in Figure 58.

Figure 58. Timing Chart for Watch-dog Timer



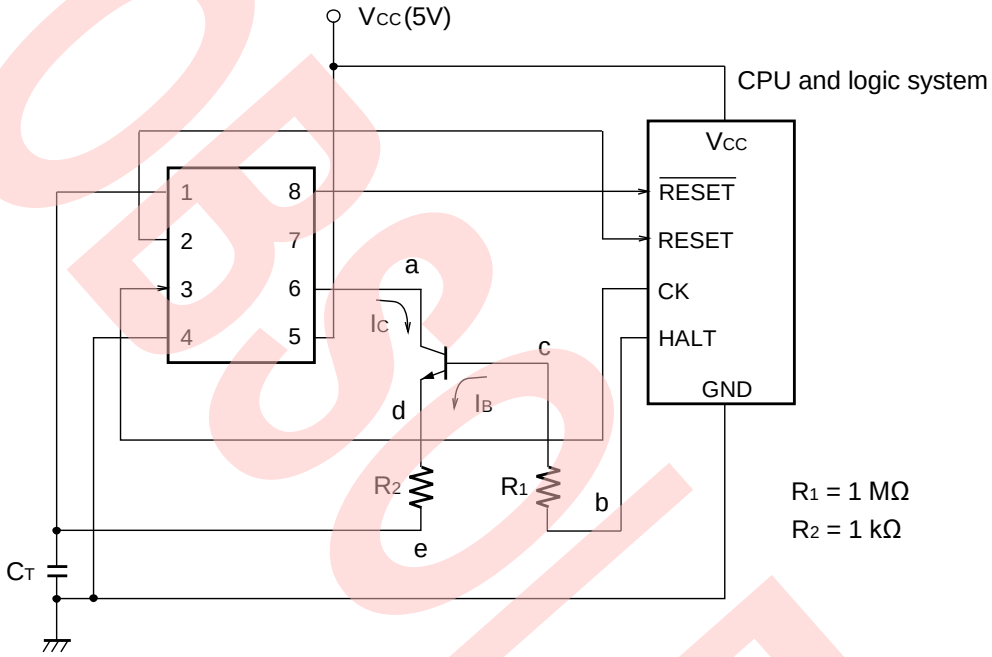
3.6 How to Stop Watch-dog Timer

This section describes how to stop the MB3773 watch-dog timer.

Related data sheet(s): Application Examples - How to Stop Watch-dog Timer

How to Stop the Watch-dog Timer

Figure 59. How to Stop Watch-dog Timer (using NPN trasistors)



See Figure 59. When the HALT output from the logic system changes its level to H, the watch-dog timer stops operating.

Let's suppose that the value of V_{REF} at point a is nearly equal to 1.24 V and that the logic output at point b is nearly equal to 5 V. When the voltage at point b reaches 5 V, the transistor is turned on, causing a flow of charging current I_C.

In response to the charging current I_C, the C_T level at point e increases (let's use the following assumption: the value of I_C is by far higher than the value of I_{CTD}, which is nearly equal to 10 µA). As point e rises, point d also rises and continues rising until the V_{CE} of the transistor becomes saturated.

Assuming that the value of V_{CE} is nearly equal to 0.1 V, the voltage at point a is nearly equal to 1.24 V. The voltage at point d may be determined as follows.

(Voltage at point d) = (Voltage at point a) - V_{CE} = 1.4 V

When this value is reached, the I_C increase stops, eliminating the R_2-based voltage drop.

Under normal conditions, when there are no more clocks sent from the microcomputer, the voltage at point e reduces its level gradually and a reset output occurs when the e smaller than or equal to 0.4 V relationship is met. When HALT changes to the H level, the watch-dog timer stops operating because the voltage at point e is maintained at approximately 1.14 V.

3.7 Cautions Regarding Watch-dog Timer Stop Circuit [1]

Different possible circuits for stopping the watch-dog timer are available as shown in the data sheet (Diagrams a through d). You can choose the one most appropriate to your system conditions.

Related data sheet(s): Application Examples - How to Stop Watch-dog Timer

3.7.1 Cautions Regarding Watch-dog Timer Stop Circuit [1]

Circuit Examples: Diagrams a and b in the Data Sheet

When you use Diagram a or b, be sure to keep the watch-dog timer operating as long as the power-ON reset has been applied because of a power rise or momentary voltage drop.

Diagrams a and b provide sample circuits applicable only under the system requirement: "at the time of a power-ON reset, the HALT will produce no watch-dog timer stop signals." If the HALT provides an input of watch-dog timer stop signals at the time of a power-ON reset, the level at the CT terminal will be set to a value equal to or lower than V_{REF} (1.24 V) before the level reaches the reset cancel voltage (1.4 V). (For details, see section 1.8 "Cautions Regarding Watch-dog Timer Stop Circuit [2]".)

Circuit Examples: Diagrams c and d in the Data Sheet

Diagrams c and d provide sample circuits that contain two-input NAND elements to eliminate the need for the considerations of Diagrams a and b.

See Diagram c. At the time of a power-ON reset, even if the HALT provides an output of watchdog timer stop signals at the H level, the other terminal of the NAND element receives an input at the L level until the power-ON reset is terminated. Therefore, the C_T terminal will never be set at any level lower than the value of V_{REF}. When using this circuit, you don't need to worry about the timing conditions for the power-ON reset and watch-dog timer.

3.8 Cautions Regarding Watch-dog Timer Stop Circuit [2]

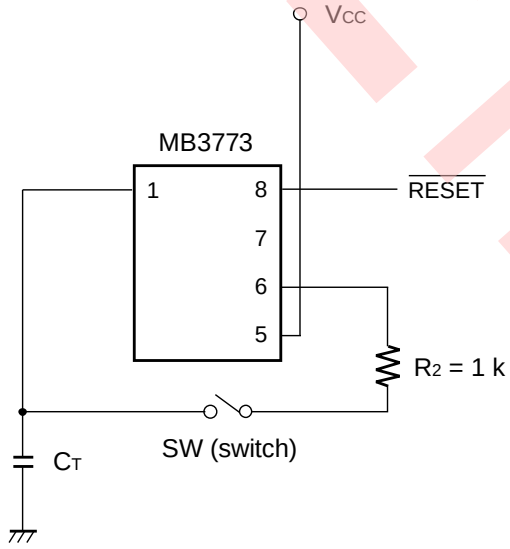
Different possible circuits for stopping the watch-dog timer are available as shown in the data sheet (Diagrams a through d). If you only want to monitor voltage by stopping the watch-dog timer, you can choose the most appropriate one.

Related data sheet(s): Application Examples - How to Stop Watch-dog Timer

3.8.1 Cautions Regarding Watch-dog Timer Stop Circuit [2]

See Diagrams a and b as sample circuits in the data sheet. It appears that the Figure 60 circuit will operate in the absence of transistors. In reality, however, it is impossible to normally detect the voltage without using switch control.

Figure 60. Sample Circuit Failing to Detect Voltage



What Takes Place from the Circuit Figure 60

1. When the V_{CC} voltage is increased with the switch turned on, the $\overline{RESET}$ terminal will remain at the L level.
2. At a power voltage of 5 V, when the switch is turned on, the watch-dog timer stops. Under this condition, if the value of V_{CC} lowers, the $\overline{RESET}$ terminal provides an output at the L level; however, the $\overline{RESET}$ terminal will remain at the L level even if V_{CC} recovers itself.

Reasons for What Takes Place from the Figure 60 Circuit

The above phenomena can be attributed to the following:

1. See the diagram of an actual circuit shown in Figure 61. The IC at pin 1 contains a resistor (r). When the internal transistor at pin 1 is turned on, the C_T terminal provides a voltage value (0.8 V according to a sample), which is produced from the reference voltage (nearly equal to 1.24 V) through the external resistor (R_2) and the internal resistor (r) at pin 1. Because pin 8 provides no output at the H level unless the voltage at point a reaches 1.4 V, the L level will remain as long as the transistor is on.
2. See Figure 62, which shows the timing of internal operation available when the value of V_{CC} is reduced with the switch turned on. Usually, the internal transistor at pin 1 is turned on when V_{CC} is not higher than V_{SL}; it is turned off when V_{CC} is not lower than V_{SH}. However, the flipflop will provide no reset input unless the voltage at pin 1 (voltage at the C_T terminal) is equal to or lower than 0.25 V. Therefore, the internal transistor at pin 1 will remain on even after V_{CC} reaches V_{SH}. (For details of the timing applicable when V_{CC} is reduced with the switch turned on, see section 3.9 “Operations of Comparator and Latch”.)
3. From "1." and "2." above, switch control is necessary when you use the Figure 60 circuit. Be sure that the transistor is turned off when V_{CC} is not higher than V_{SL}; it is turned on when V_{CC} is not lower than V_{SH}.

Figure 61. Actual Circuit

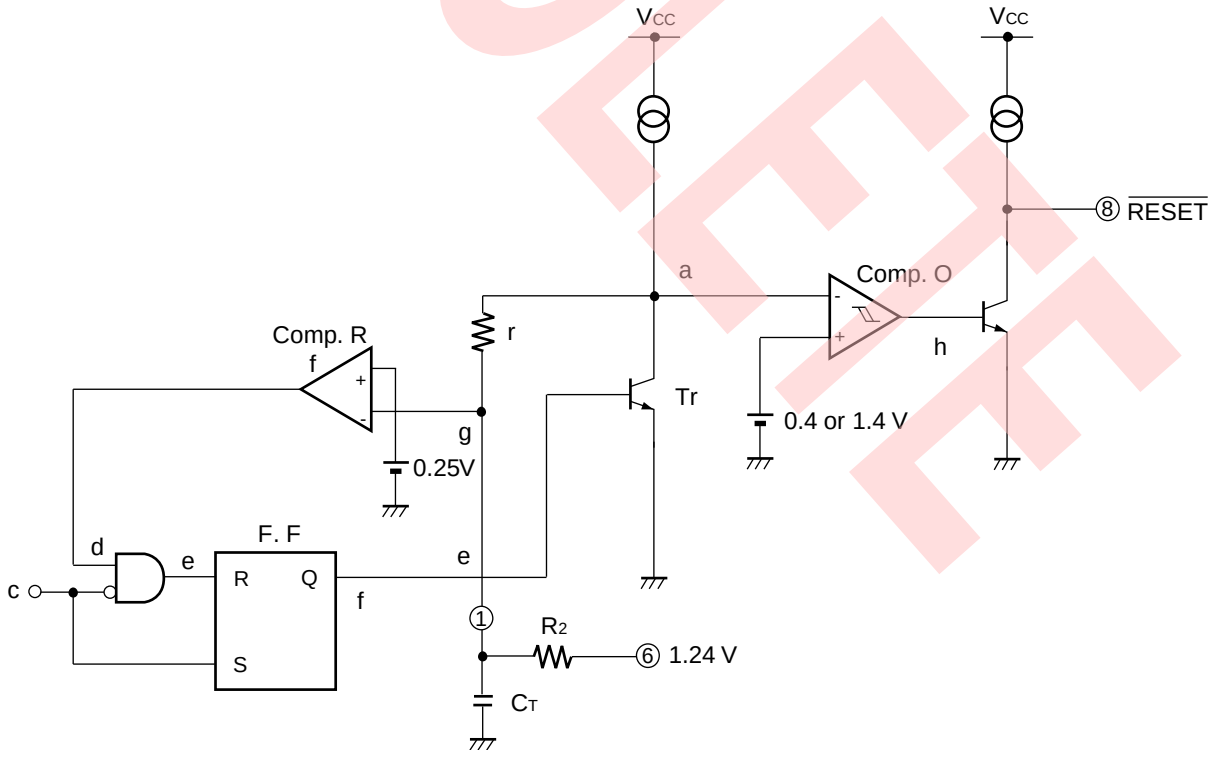
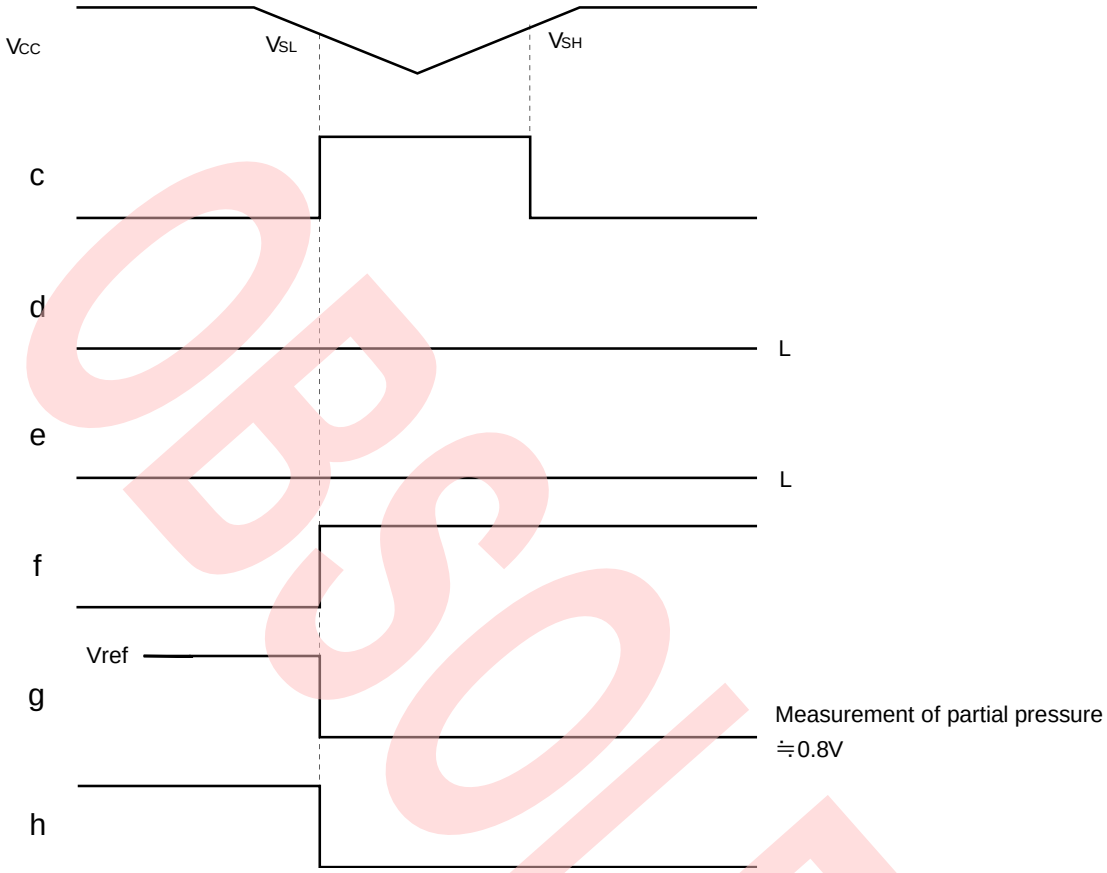


Figure 62. What Takes Place Internally when V_{CC} is Reduced with Switch On



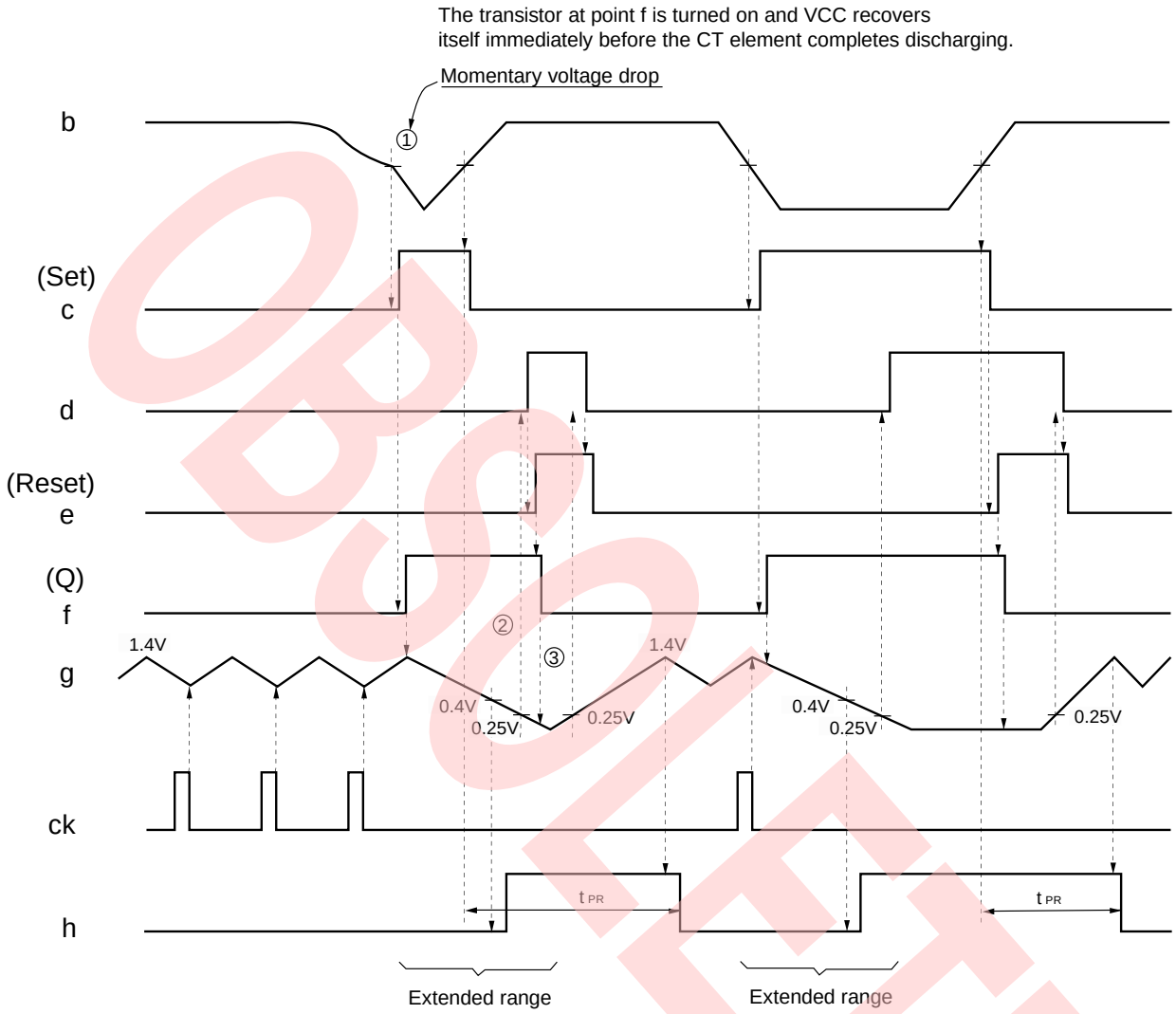
3.9 Operations of Comparator and Latch

This section describes the operations of the comparator (Comp.) and latch.

Operations of Comparator and Latch

Figure 63 shows the operations timing of the comparator and latch (For the circuit chart, see Figure 61).

Figure 63. Operations Timing of Comparator and Latch

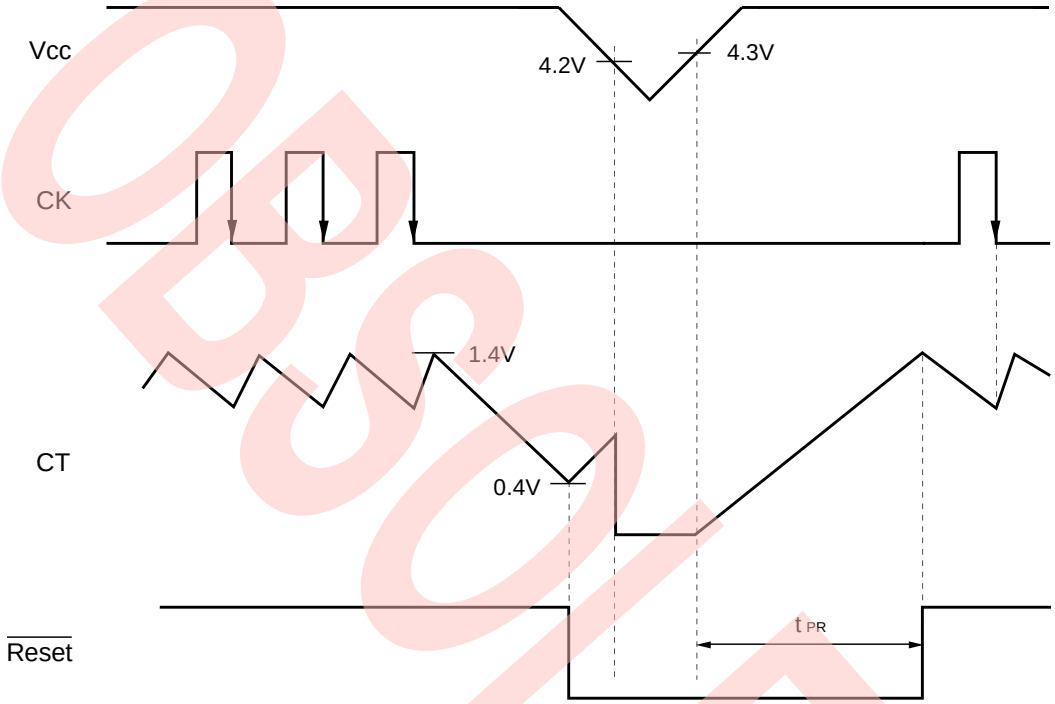


1. As the power voltage drop, C_T begins discharging.
2. The latch is reversed when the C_T voltage becomes lower than the V_{TH} (nearly equal to 0.25 V) of the internal comparator.
3. As a result of "2.", C_T is switched to charging (in the case of a momentary voltage drop as shown in Figure 63).
4. Comp. R and the latch operate the following way. Even in situations where V_{CC} recovers itself before C_T completes full discharging, the discharge process will continue until the C_T level reaches V_{TH} (nearly equal to 0.25 V). Due to this operation, it is possible to maintain a required value for the tPR time even when the power supply encounters a momentary voltage drop.

3.10 Power Drop in Resetting Watch-dog Timer

If there is a power drop while the reset for the watch-dog timer is effective, the reset output provides the hold time as shown in this section.

Power Drop in Resetting Watch-dog Timer



3.11 Handling Unused Terminals

How to handle unused terminals in the MB3773 is summarized in.

Handling Unused Terminals

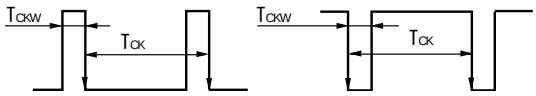
Table 4. Handling Unused Terminals in the MB3773

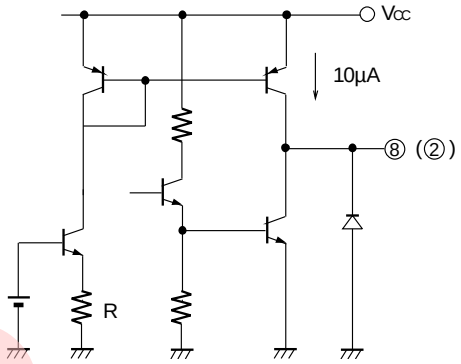
Terminal Name	Description
C_T terminal	OPEN
RESET terminal	OPEN
CK terminal	OPEN
V_{REF} terminal	OPEN
V_S terminal	OPEN
$\overline{RESET}$ terminal	OPEN

3.12 Q&A Set Regarding the MB3773

This section provides a set of questions and answers regarding the MB3773.

Q&A Set Regarding the MB3773

Q&A Set Regarding the MB3773			
Q1	What is the value of power current I_{CC} if the measurement condition "with the watch-dog timer in operation" is not effective?	A1	Because of a bipolar IC, there is no significant difference. It is almost the same as the value obtained when the watch-dog timer is in operation.
Q2	What do the following terms specifically refer to: CK input pulse width (T_{CKW}) and input interval (T_{CK})?	A2	They are illustrated below. 
Q3	What will happen if CK goes down to 3 µs?	A3	The pulse generator will become unable to catch up with the clock speed any longer. That is, any clock signals whose width is not greater than 3 ms will be neglected. The minimum value of "CK input pulse width" is specified as 3 ms in the standard; potentially, however, pulses will be produced from clock signals whose width is not smaller than 1 µs.
Q4	Is it alright to shoot the C_T or V_{REF} terminal to the V_{CC} terminal?	A4	The IC will not be destroyed immediately when the V_{CC} voltage is applied, although there is no specific standard regarding the maximum rating for the C_T and V_{REF} terminals. The approach is not recommended, however, because continuous use might result in degraded characteristics. Be sure that the C_T terminal receives a value not higher than V_{REF} and that the V_{REF} terminal will receive no voltage.
Q5	If the V_S terminal at pin 7 is given a pull-up to prevent the detection of a voltage drop, what is the guaranteed voltage range for making the RESET terminal at pin 2 the L level?	A5	It is up to 3.5 V. If the power voltage is below 3.5 V, it is not guaranteed that the internal comparator operates normally. Therefore, you should set the detection voltage at a value higher than 3.5 V. This is different from the standard for the minimum power voltage of 1.2 V (max.) that guarantees the reset.
Q6	There is a standard for the minimum power voltage of 1.2 V (max.) that guarantees the reset. Does this mean that you can set a minimum of 1.2 V?	A6	You should set the detection voltage at a value higher than 3.5 V. Only the reset output unit guarantees the L level even if the power voltage goes down to 1.2 V. In this case, the internal reference voltage is not kept at 1.24 V; the comparator is not working normally, either. Therefore, voltage detection is not possible.
Q7	Regarding the adjustment of detection voltage with an external resistor: 1. Is the V_{REF} term in the equation a fixed value? 2. What are the causes for fluctuations? A look at a graph regarding temperature characteristics does not reveal any significant change. 3. Is it possible to limit the detection voltage to a range between 4.5 V and 4.7 V by using a metal film resistor (approximately plus or minus 1 %) as the external resistor?	A7	1. Fluctuations exist ranging from 1.215 V to 1.275 V. 2. Fluctuations in reference voltage are dependent on the device parameters and configuration of actual circuits. They include fluctuations in the diffused resistor inside the IC and relative errors of the hfe value of the transistors comprising the current mirror. Because the MB3773 reference voltage circuit is based on the band gap reference system, no significant potential changes are observed, as shown in the Standard Characteristic Curves data sheet. However, a great deal of allowance is given, because temperature testing was not carried out as part of the shipment testing. 3. Only when there are no resistance fluctuations, the fluctuations in V_{SL} and V_{SH} are considered to be roughly within the allowable range specified by the existing standard.

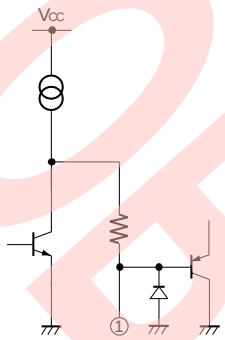
Q&A Set Regarding the MB3773			
Q8	What is the degree of fluctuations in the reset terminal output current of 10 µA? And what are the causes for it?	A8	Current fluctuations are estimated at approximately plus or minus 50 %. The internal pull-up circuit for the reset terminal is a constant current circuit of the current mirror type using PNP transistors. Causes for the current fluctuations include the following: relative error of the resistor R, error of the resistor R's upper potential, and error of the PNP transistor current. The combined value is approximately from minus 50 to 100 % (reference value ranging from 5 µA to 20 µA) 
Q9	When used alone, ICs will work normally. When they are assembled into a system, however, the RESET terminal will remain at the L level (or show an unstable operation). What are probable causes? And how can you remove them?	A9	1. Because the reset terminal on the system side has a low impedance, there may be an excess pull against the current. (Also see the data sheet: Standard Characteristic Curves - High Level Output Voltage vs. High Level Output Current.) If this occurs, you can remove the problem by giving a resistor pull-up to the reset terminal. The resistance is determined by the potential current of the reset output transistor. You should choose an appropriate resistance that will prevent the maximum current from exceeding 20 mA. 2. Additionally, there may have been a malfunction under the influence of power noise resulting from microcomputers or other components. In this case, you can reduce the noise-caused momentary voltage drop by either taking the delay trigger method or inserting a bypath capacitor (approximately 0.1 µF) between the IC's power terminals.

3.13 Equivalent Circuits for MB3773 Input / Output Unit

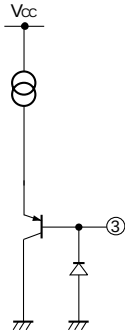
The following are equivalent circuits for the MB3773 input/output unit.

Equivalent Circuits for MB3773 Input / Output Unit

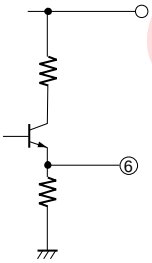
<C_T terminal>



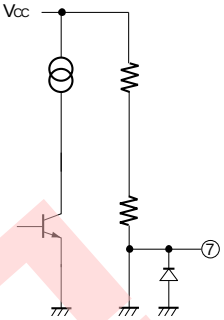
<C_K terminal>



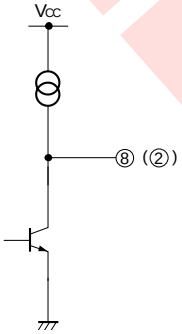
<V_{REF} terminal>



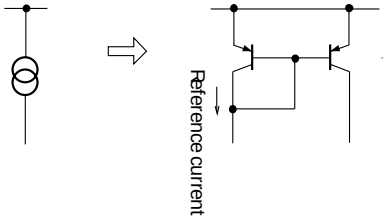
<V_S terminal>



<RESET and $\overline{\text{RESET}}$ terminals>



Note: A circuit having current symbols is a constant current circuit of the current mirror type using PNP transistors, as shown below.



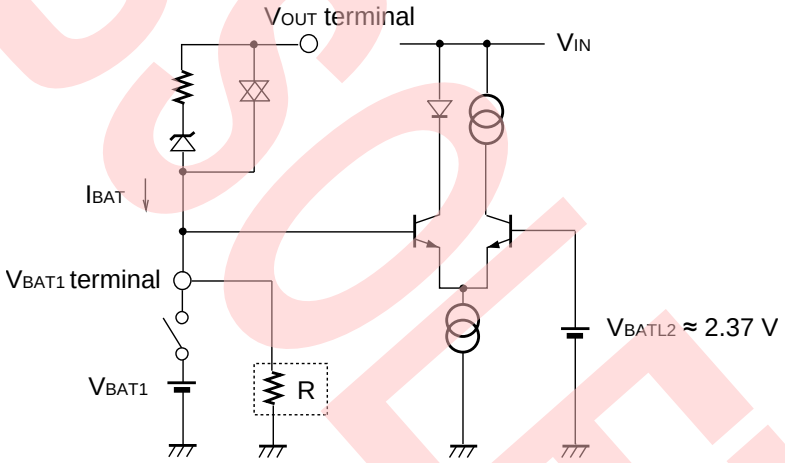
4 MB3790 Applications

4.1 How to Produce Alarms in the Case of a Battery Replacement

This section explains how to produce alarms for the case of battery replacement using the MB3790.

4.1.1 How to Produce Alarms During Battery Replacement

Figure 64. Equivalent Circuit (for producing alarms during battery replacement)



If the terminal V_{BAT1} is open for such reasons as a battery replacement, the alarm output becomes undefined. Even in open condition, it is possible to produce alarms for indicating a simple reduction in battery level by applying a pull-down of resistor R to the terminal V_{BAT1} in parallel with the battery. In this case, it would be desirable to increase the value of R in order to limit the increase in the current consumption of the battery. The choice of the maximum value is explained below.

When V_{IN} = 5 V

The standard value of the current I_{BAT1} from the V_{BAT1} terminal is 100 nA (max.), assuming that V_{BAT1} = 3 V and Ta = 25 °C. (This remark refers to the value of I_{BAT} as shown in the data sheet. I_{BAT} is likely to rise as the temperature increases.) Under the condition of V_{BAT1} = 0 V, we assume that the external resistor R is connected to V_{BAT1}, as shown in Figure 64 (there is no specific standard). It is necessary to choose the value of R in such a way that the increase in voltage at R due to I_{BAT1}' (the current from the V_{BAT1} terminal) does not exceed V_{BAT2} (= 2.37 V).

$$R \times I_{BAT} < V_{BATL2}$$
$$R < V_{BATL2} / I_{BAT1}'$$

If I_{BAT1}' is approximately 100 nA, the following relations are applicable.

$$R < 2.37\ V / 100 \cdot 10^{-9}\ A$$
$$\underline{R < 23.7\ M\Omega}$$

We assume that the maximum resistance is not higher than 100 MW for Ta = 25 °C (however, this is only an empirical value and we can not guarantee it).

When V_{IN} = 0 V

No alarms are produced, as the comparator does not operate.

4.2 Analog Switches

This section explains how to use analog switches.

4.2.1 Analog Switches

Figure 65. Equivalent Circuit (for primary and secondary batteries)

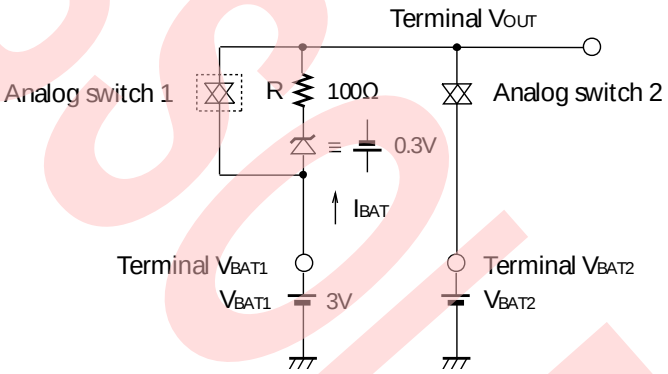
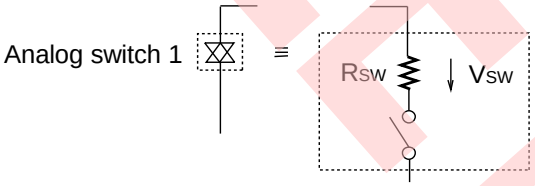


Figure 66. Equivalent Circuit for Analog Switch 1



At analog switch 1, the ON resistance R_{SW} is nearly equal to 10 kΩ.
V_{SW} stands for the voltage drop at R_{SW}.

When Using Primary and Secondary Batteries Together (CONTROL terminal in "H" status)

Make sure that the analog switch 1 is off so as to prevent a current flow from the secondary to the primary battery.

When Using Only the Primary Battery (CONTROL terminal in "L" status)

1. In Figure 65, the analog switch 1 and the diode are connected in parallel so to improve the characteristics with respect to the voltage difference between input and output (the SBD is used to minimize the voltage drop within the IC).
   - Analog switch path: 10 kΩ resistance (for the ON case)
   - Diode path: 0.3 V + 100 kΩ resistance

2. Figure 66 shows an equivalent circuit that is available when analog switch 1 is turned on. The input current I_{BAT} through battery 1 is extremely low and all of it flows into the analog switch when the voltage drop at analog switch 1 is not higher than 0.3 V because of ON resistance R_{SW}. If the value of I_{BAT} increases while the voltage drop at RSW reaches 0.3 V, a part of the current flows into the diode. Because of this mechanism, the following equation valid:

   (Voltage drop at R_{SW}) = (Voltage drop at 100 Ω resistance) + 0.3 V

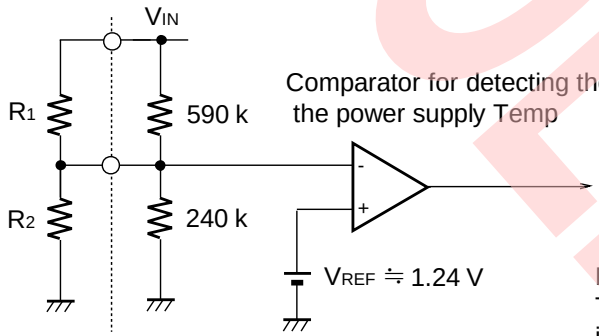
3. The standard contains an item "Battery 1 output voltage difference DV_{B1}." When the value of I_{BAT} is extremely small (as low as 10 µA), the SBD is off. This causes a difference in electrical potential of 0.1 V (= 10 µA x 10 kΩ) between the terminals V_{OUT} and V_{BAT1}. When I_{BAT} = 100 µA, the current is approximately 30 µA on the side of analog switch 1 and 70 µA on the side of SBD + 100 Ω, which leads to a difference in the electric potential between the terminals V_{OUT} and V_{BAT1} of approximately 0.3 V. Even if the current increases 100 times, the difference in electrical potential increases only three times.
4. Make sure that the terminal V_{BAT2} stays open.

4.3 How to Fine-tune the Voltage Detection Level for the Power Supply

This section explains how to fine-tune the power voltage detection level.

How to Fine-tune the Voltage Detection Level for the Power Supply

Figure 67. Equivalent Circuit (for fine-tuning power voltage detection level)



Note:
The resistance of the IC-internal resistors is provided with a absolute accuracy of plus or minus 30 % and a relative accuracy of plus or minus 2 % (however, this is only an empirical value and we can not guarantee it).

In Figure 67, R_A stands for the combined resistance of 590 kΩ and the external resistance R_1, while R_B stands for the combined resistance of the 240 kΩ and the external resistance R_2.

$$R_A = R_1 \cdot 590\ k\Omega / (R_1 + 590\ k\Omega)\ [\Omega]$$

$$R_B = R_2 \cdot 240\ k\Omega / (R_2 + 240\ k\Omega)\ [\Omega]$$

The detection voltage can be calculated as follows.

Detection voltage $V_{INL} = (R_A + R_B) / R_B \times (V_{REF} - \Delta V)$ [V]	(For a falling value of V_{CC})
Detection voltage $V_{INH} = (R_A + R_B) / R_B \times V_{REF}$ [V]	(For a rising value of V_{CC})

The above calculation assumes that the threshold level of the comparator is V_{REF} (which is nearly equal to 1.24 V (typ.)) and that the width of the hysteresis is ΔV = 29 mV (typ.). [ΔV is calculated as follows: DV_{IN} x 240 / (590 + 240).]

Choosing the values of R_1 and R_2 in such a way that the conditions of R_1 << 590 kΩ and R_2 << 240 kΩ are met produces simpler equations for determining the detection voltage.

Detection voltage $V_{INL} \approx (R_1 + R_2) / R_2 \times (V_{REF} - \Delta V)$ [V] (For a falling value of V_{CC})

Detection voltage $V_{INH} \approx (R_1 + R_2) / R_2 \times V_{REF}$ [V] (For a rising value of V_{CC})

Note: The minimum input voltage for the MB3790 is 4.0 V. It is therefore necessary to set the detection voltage to a value higher than 4.0 V.

4.4 Capacitance Connected to the Terminal C_T

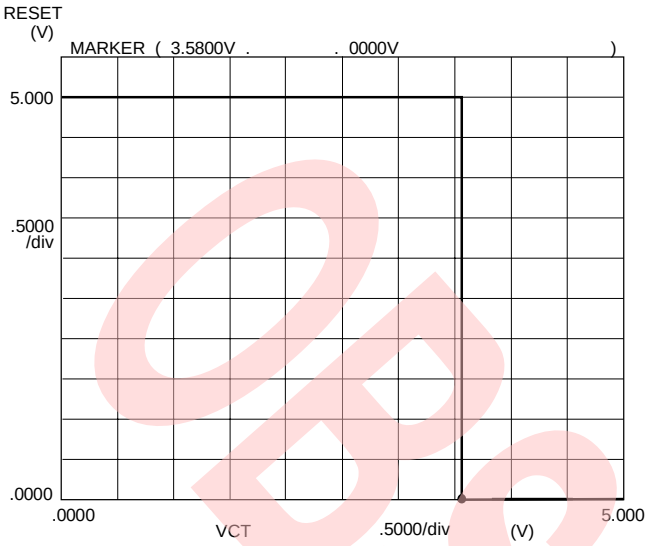
The capacitance that is connected to the terminal C_T should have a value that causes little leakage. Otherwise, the voltage at the terminal C_T can not exceed the value of Vth (= 3 V), and the reset may fail to be canceled.

Capacitance Connected to the Terminal CT

The charging current to the terminal C_T is approximately 3 µA. Choose a capacitance with little leakage. If a capacitor with high leakage is used, such as an electrolytic capacitor, t_{PO} will be prolonged or the terminal C_T might not be charged.

The plot below shows reference data (as measured for a single sample). Figure 68 shows the voltage threshold at the terminal C_T. Figure 69 shows the relationship between the leak current and the voltage at the terminal C_T. Figure 68 shows clearly that the reset fails to be canceled if the voltage at the terminal C_T does not exceed Vth (which is 3.28 V in this example). Figure 69 shows that subtracting a current of approximately 3 µA from the terminal C_T causes a drop in the voltage at the terminal C_T, which means that the capacitor will not be charged.

Figure 68. Threshold Vth of Voltage at the Terminal C_T



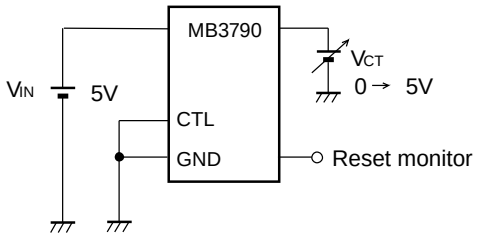
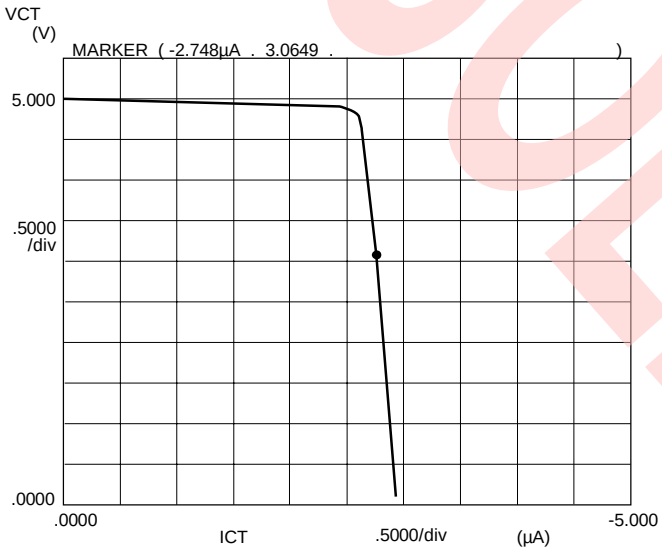
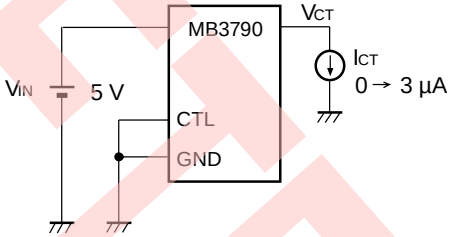


Figure 69. Relationship Between Leak Current and Voltage at the Terminal C_T





4.5 How to Adjust the Time for Detecting the Voltage of the Power Supply

This section explains how to adjust the time for detecting the voltage of the power supply.

Related data sheet(s): Application Examples - Adjusting the Supply Voltage Detection Level Set Time

How to Adjust the Time for Detecting the Voltage of the Power Supply

Figure 70. Equivalent Circuit (for adjusting the time for detecting the voltage of the power supply)

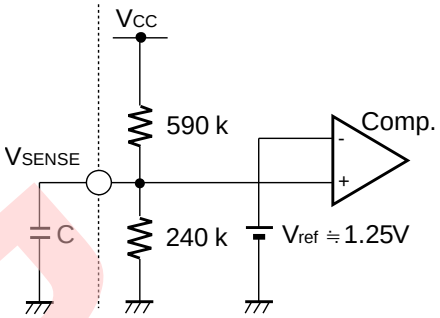
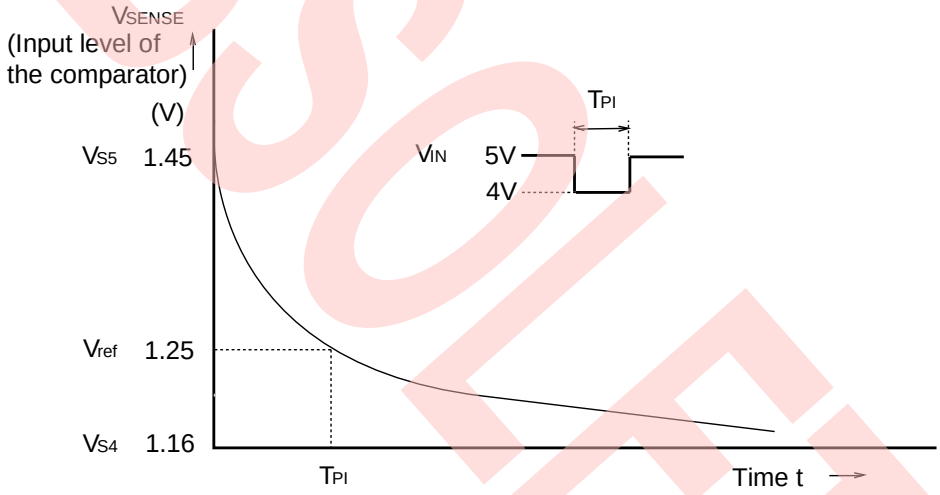


Figure 71. Change in the Voltage at Terminal V_{SENSE}



When the value of V_{IN} changes from 5 V to 4 V, part of the charge that is stored in capacitor C is discharged to GND through the 240 kΩ resistor (see Figure 70).

In this case, the voltage V_{SENSE} will change as shown in Figure 71. The detection time t_{PI} can be described by the following equation. V_{S5} is the voltage at the terminal V_{SENSE} for V_{IN} = 5 V and V_{S4} is the voltage at the terminal V_{SENSE} for V_{IN} = 4 V.

$$(V_{ref} - V_{S4}) = (V_{S5} - V_{S4}) \times e^{-tPI / CR}$$

The detection t_{PI} can be described by the following equation.

$$t_{PI} = -C \times R \times \ln \frac{(V_{ref} - V_{S4})}{(V_{S5} - V_{S4})}$$

$$= 2.8 \times 10^5 \times C$$

$$t_{PI}\ [\mu s] \approx 0.28 \times C\ [pF]$$

[Example]

For C = 1,000 pF, t_{PI} is close to 280 µs.

Note:

1. Note that the above equation might change for differing waveforms of V_{IN}.
2. Generally, the resistance is provided with a absolute accuracy of plus orminus 30 % and a relative accuracy of plus or minus 2 %. For the actual values of t_{PI}, validate the numbers experimentally.

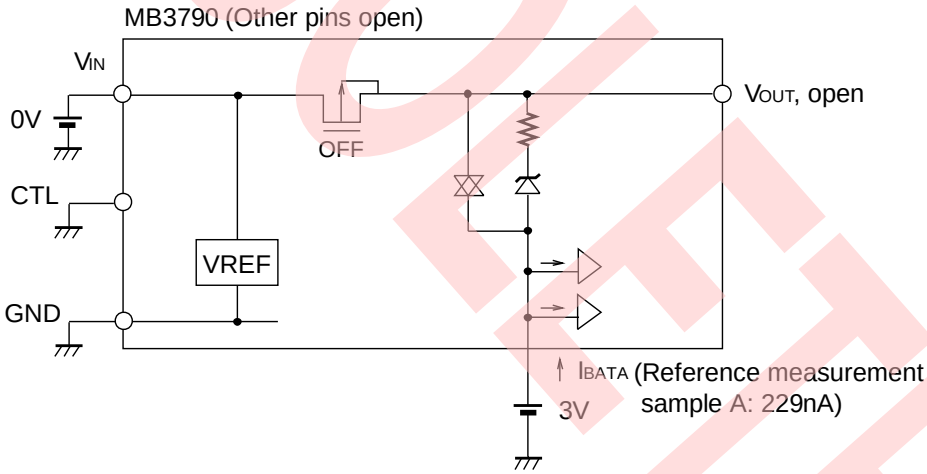
4.6 Current Consumption (I_{BATA} and I_{BATB}) in the Primary Battery

Among the electrical characteristics used in the data sheet, there are the items "Input currents I_{BATA} and I_{BATB} of Battery 1." These values are defined as explained below.

4.6.1 Current Consumption (I_{BATA} and I_{BATB}) in the Primary Battery

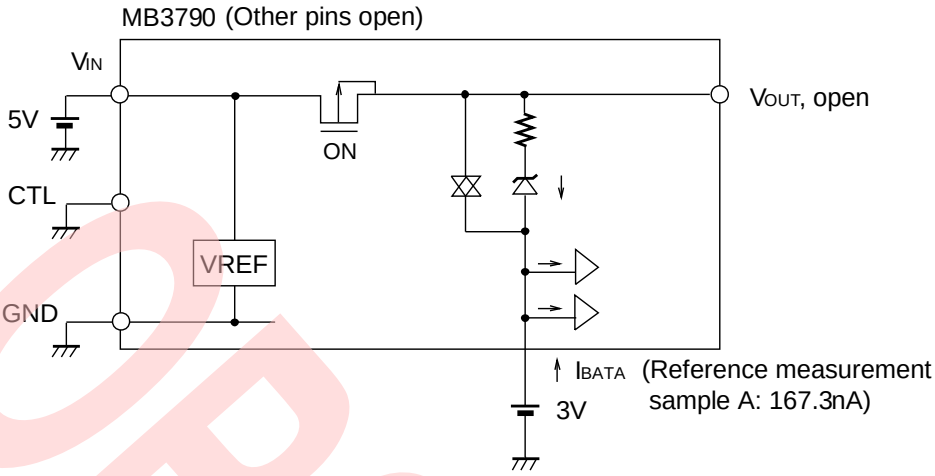
I_{BATA}: In the circuit below, I_{BATA} stands for the current from the primary battery for V_{IN} = 0 V. In other words, this is the current consumption of the IC itself during a backup.

This current flows mainly because of the input bias current of the comparator. It has a maximum value of 500 nA, as specified by the standard, and flows into the IC.



I_{BATB}: In the circuit below, I_{BATB} stands for the current from battery 1.

The input bias current of the comparator and the leak current of the SBD lead to a current flow at the terminal I_{BAT}. The standard specifies a maximum incoming current of 500 nA and a maximum outgoing current of 100 nA.



Note: When using a lithium-based primary battery for V_{BAT1}, take extra care to ensure that there is no backward current to the battery.

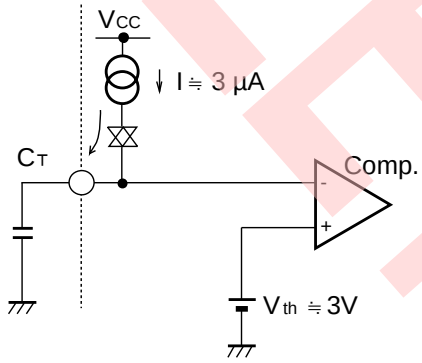
Tip: The above requirements for I_{BATA} and I_{BATB} refer to the current that is consumed in the IC when there is no load at the terminal V_{OUT}. It should be noted that the value of I_{BAT} will also increase if there is an output current and a load at V_{OUT}.

4.7 How to Calculate the Reset Pulse Width (t_{PO})

This section explains how to calculate the reset pulse width (t_{PO}).

How to Calculate the Reset Pulse Width (tPO)

Figure 72. Equivalent Circuit [for calculating the reset pulse width (t_{PO})]



When the voltage at V_{OUT} exceeds the value of V_{INH}, the 3 µA constant current power supply begins to charge the capacitor that is connected to the terminal C_T. The reset is canceled when the charging reaches the threshold voltage Vth of the comparator (See Figure 72).

The reset pulse width (t_{PO}), which is actually the time required for charging the terminal C_T to 3 V, can be described by the following equation.

$$I \times t_{PO} = C_T \times V_{th}$$

$$t_{PO}\ [ms] = \frac{V_{th}}{I} \times C_T$$

The following equation can be obtained when using typical values and assuming that Vth and I are close to 3 V and 3 µA, respectively.

$$t_{PO}\,[ms] \fallingdotseq 10^{-3} \times C_T \quad [pF]$$

[Example]

For C_T = 1000 pF, t_{PO} is close to 1 ms.

Note: The standard value for t_{PO} of 50 % to 200 %, as used in the data sheet, does not account for fluctuations in the external capacitance C_T.

4.8 Charging the Secondary Battery from the Primary Battery

This section covers the question whether the voltage in the primary battery decreases if the secondary battery, being at 0 V, is charged from the primary battery.

Charging the Secondary Battery from the Primary Battery

When V_{IN} is open and a discharged secondary battery is connected to the primary battery, a current will flow from the primary to the secondary battery (See Figure 73).

Figure 73. Analog Switch (charging the secondary battery from the primary battery)

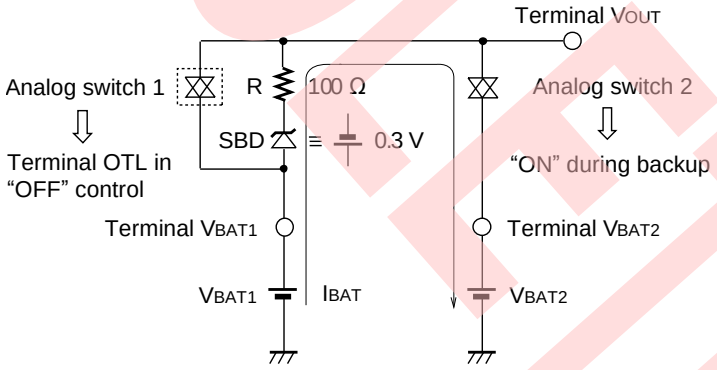
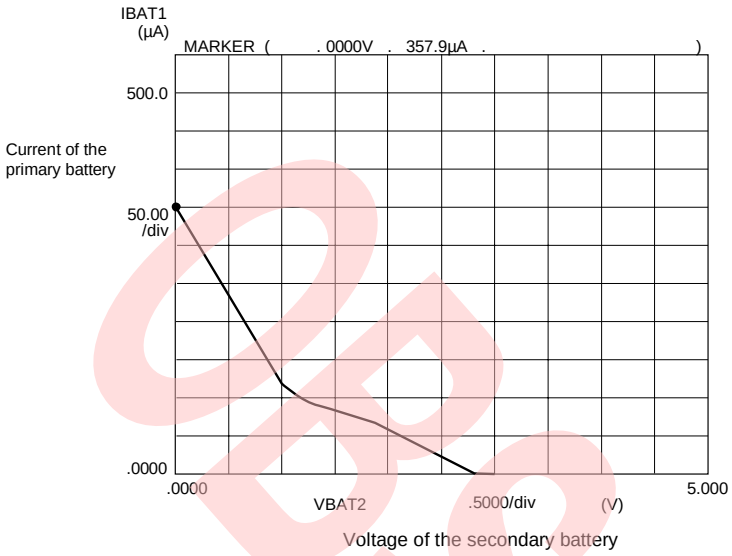
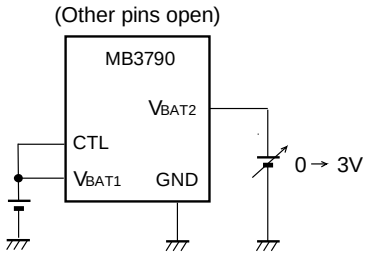


Figure 74 is a plot of data obtained for charging the secondary battery from the primary battery.

Figure 74. Data Obtained for Charging the Secondary Battery from the Primary Battery





Measurement circuit

When the primary battery is at 3 V and the secondary battery is at 0 V, a current flows from the primary to the secondary battery. Assuming that V_{BAT1} = 3 V and V_{BAT2} = 0 V, the charging current can be described by the following equation, since it is known that a resistor of 100 Ω and an analog switch which presumably has a resistance of 10 kΩ are located between V_{BAT1} and V_{BAT2}.

$$I_{BAT1} \fallingdotseq \frac{3\,V}{10\,k\Omega + 100\,\Omega} \fallingdotseq 300\,\mu A$$

Figure 74 shows measured data for a sample of 357 μA.

Discharging continues until the voltage of the secondary battery is nearly equal to that of the primary battery. At the end of this process, both batteries will have half the initial charge of the primary battery (discharging stops when the voltage of the secondary battery is approximately equal to that of the primary battery minus 0.3 V). The time for the entire process varies depending on the capacitance and charging characteristics of the primary battery. Consult the manufacturer of the primary battery for details.

Batteries are shipped in discharged status. Prior to using them, they have to be charged by the system immediately after connection. Moreover, when replacing a small-capacity primary battery, it is recommended to charge the secondary battery in advance. It should also be kept in mind that a secondary battery with high leakage will decrease the charge in the primary battery.

4.9 Major Reasons for Drop in Battery Charges

In some cases, the terminal V_{OUT} might provide only an output of about 2 V during a backup although the battery contains a charge of 3 V. This section discusses the probable reasons for this behavior.

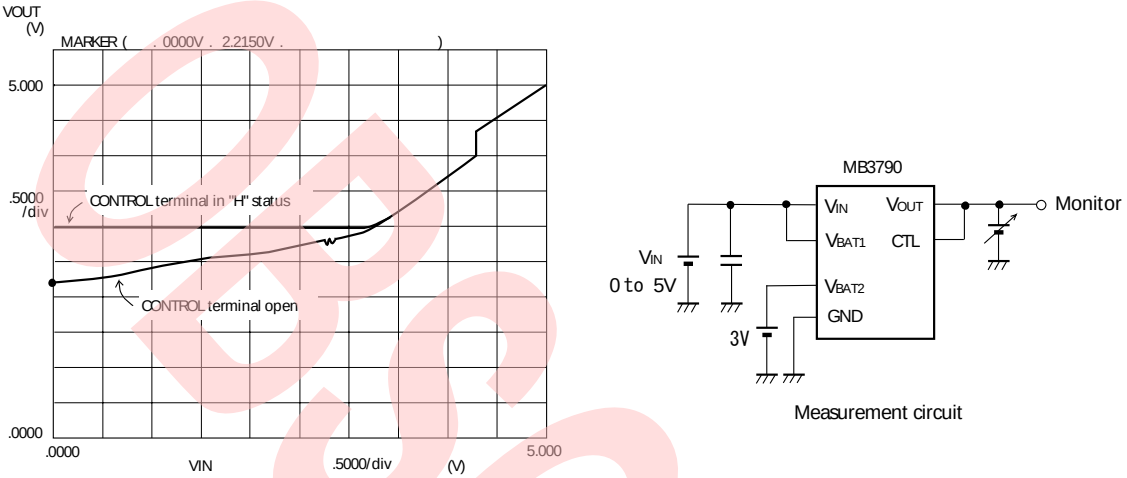
4.9.1 Major Reasons for Drop in Battery Charges

Provided that there are no problems with the IC, the following two reasons might be responsible.

When the CONTROL Terminal is Open

The circuit becomes unstable when the CONTROL terminal stays open. Even when the battery charge is 3 V, the value of V_{OUT} might decreases to be only about 2 V (See Figure 75).

Figure 75. V_{OUT} in Dependence of V_{IN}



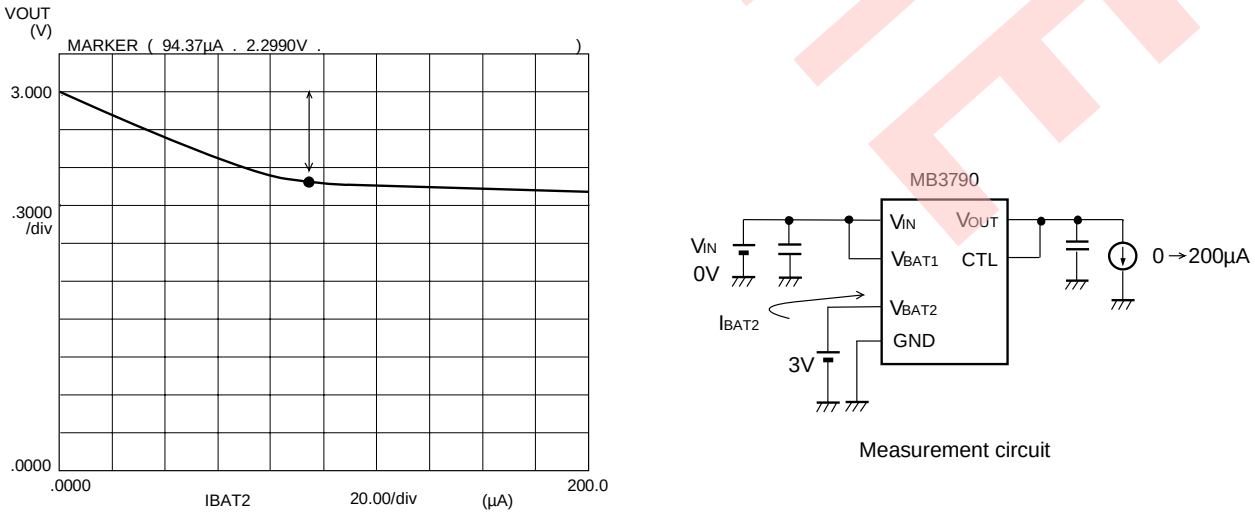
When There is Excessive Current Pull

Especially when the terminal V_{OUT} is connected not only to the SRAM but as well to other logical circuits, check how much current is being output from the terminal V_{OUT} (the standard value is up to 500 µA).

Figure 76 shows the measured change in V_{OUT} voltage when the current at V_{OUT} changes from 0 to 200 µA, assuming that V_{IN} = 0 V and V_{BAT2} = 3 V in backup state. The graph shows the voltage drop depending on the current that is obtained from the terminal V_{OUT}.

Note: As the reset terminal is internally connected to V_{OUT} as well, any current consumption at that terminal will cause a drop in the V_{OUT} voltage as well.

Figure 76. V_{OUT} in Dependence of I_{BAT2}

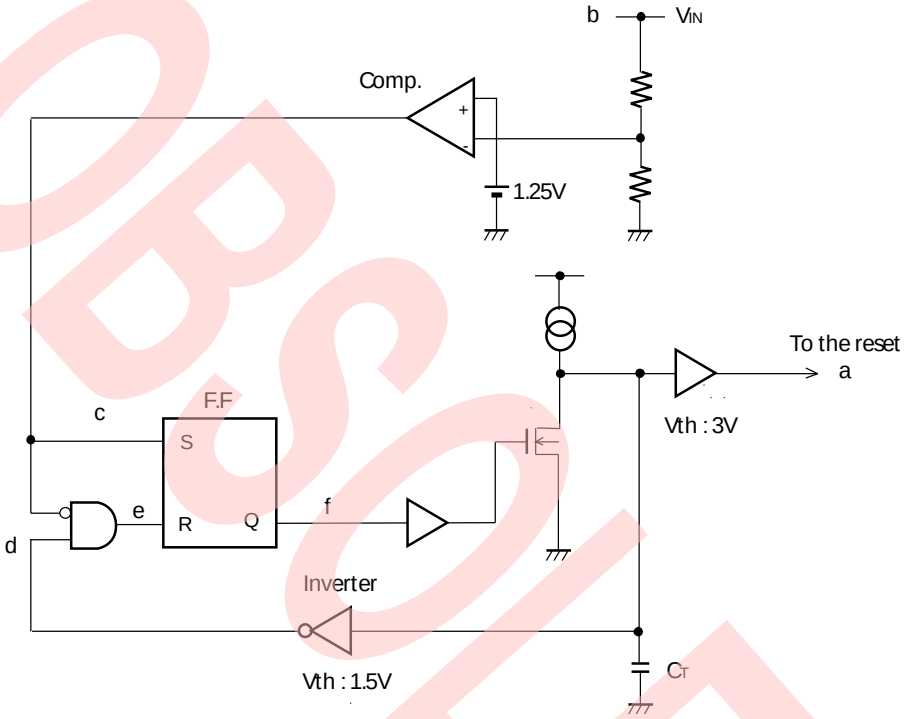


4.10 Operation at Input Pulse Width (t_{PI}) of Less than 5 µs

This section describes the operation of this IC at input pulse width (t_{PI}) of less than 5 µs.

Operation at Input Pulse Width (tPI) of Less than 5 µs

Figure 77. Block Diagram of the Operation at Input Pulse Width (t_{PI}) of Less than 5 µs



If the width of t_{PI} is lower than 5 µs, the reset output is undefined. However, it is not possible to have a "halfway" reset output. If there is a reset output, it is nearly equal to the width of t_{PO} as specified by C_T. While the effective value of t_{PI}, which specifies actually the minimum t_{PI} value for obtaining a reset output, is different from sample to sample, a value of 5 µs is guaranteed to work. (While there might be a reset output at a value of less than 5 µs, it is guaranteed that there will be a reset output for a value of 5 µs or more.)

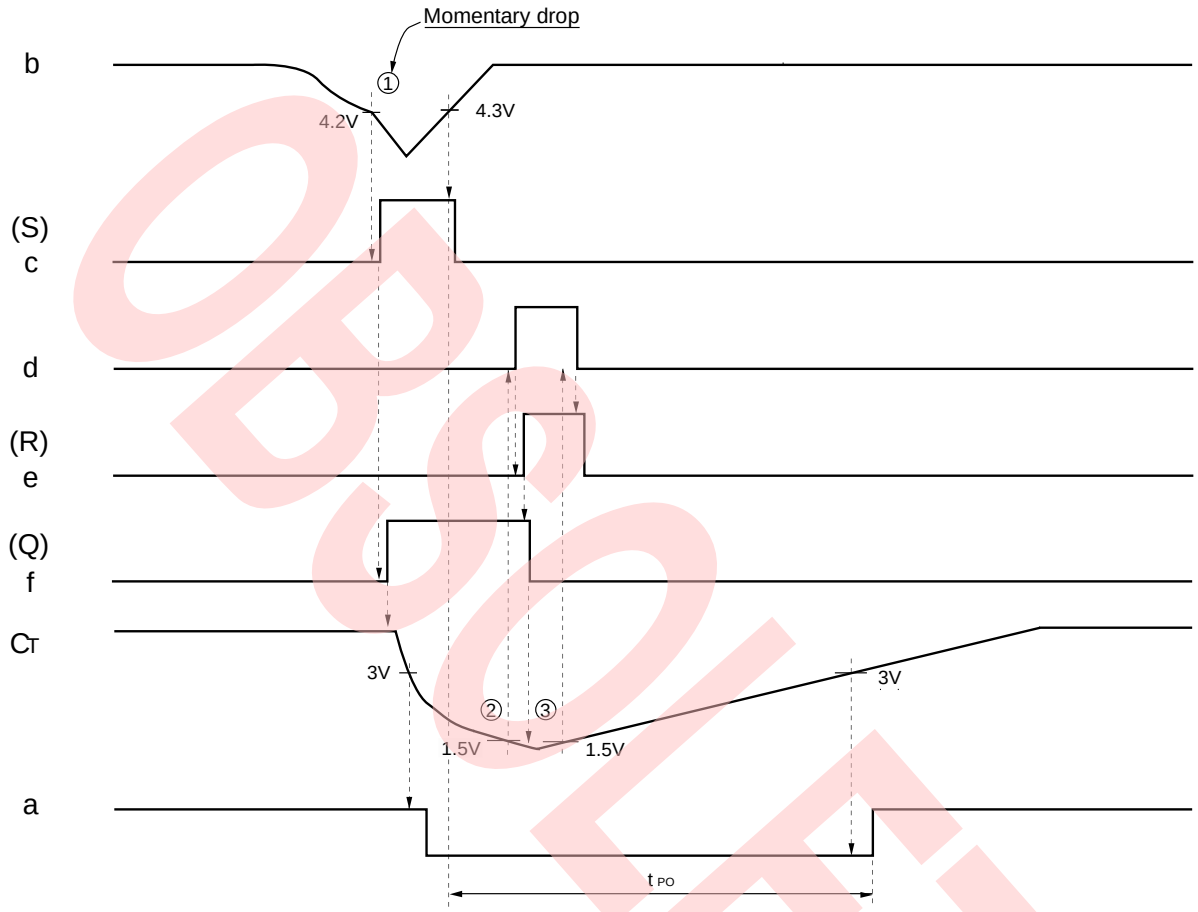
Since there is a built-in latch circuit, discharging continues till the C_T voltage went down to approximately 1.5 V, even if V_{CC} is recovered before C_T is discharged to 1.5 V. Therefore, a detected drop in V_{CC} will always produce a normal reset output.

Refer also to Figure 78, which shows the waveforms of the operation described by the block diagram in Figure 77.

In this example, capacitor C was connected to the terminal V_{SENSE} terminal in order to increase the value of t_{PI} (refer also to Section 4.5 “How to Adjust the Time for Detecting the Voltage of the Power Supply”). The capacitor C has no influence on the value of t_{PO}. There are no appropriate circuits for reducing the value of t_{PI}.

Figure 78. Waveforms for a Momentary Drop in V_{CC}

The transistor at point f is switched on and VCC is recovered immediately before the CT element is discharged to 1.5V.



1. As the voltage of the power supply decreases, discharging of C_T begins.
2. The latch is reversed as soon as the C_T voltage is lower than the voltage V_{TH} (approximately 1.5 V) at the internal inverter.
3. As a result of the switch of the latch, C_T is switched into charging mode (in the case of a momentary drop as shown in Figure 78).
4. The inverter and the latch operate in the following way: Even when V_{CC} is recovered before C_T is discharged to 1.5 V, the discharging process continues till the voltage at C_T is equal to V_{TH} (approximately 0.25 V). As a result of this operation, it is possible to maintain a required value for the time t_{PR} even if there is a momentary drop in the power supply.

4.11 Backup: How to Add a Super Capacitor to V_{OUT}

This section describes a method for implementing a backup output by adding a super capacitor to the terminal V_{OUT}.

Backup (how to add a super capacitor to V_{OUT})

Figure 79. Equivalent Circuit [1] (for implementing a backup by adding a super capacitor to the terminal V_{OUT})

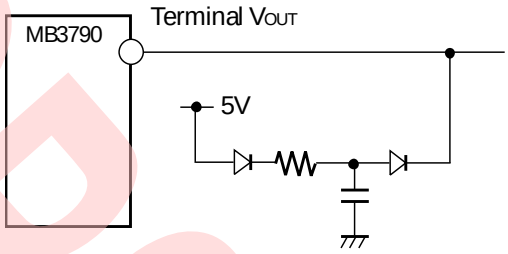


Figure 80. Equivalent Circuit [2] (for implementing a backup by adding a super capacitor to the terminal V_{OUT})

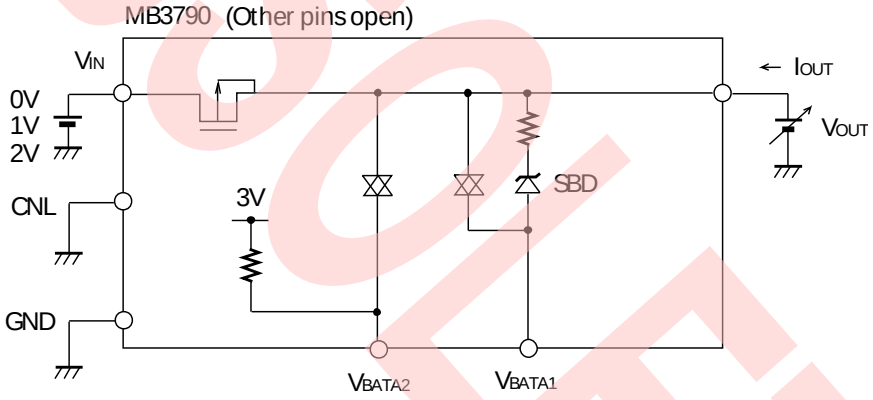


Figure 79 shows a method for a backup that consists of connecting a capacitor to the V_{OUT} terminal. An appropriate value for the resistance has to be selected depending on the connected capacitor and diode.

There is no standard that would specify the maximum value for V_{OUT}; however, the withstand voltage is approximately 6 V, comparable to V_{BAT}.

As soon as the voltage of V_{OUT} exceeds 3.5 V, there will be leak current. The leak current increases depending on the voltage at V_{IN}. It also varies from sample to sample. The circuit shown in Figure 79 tends to affect the backup time to a certain degree, since the voltage level at the terminal V_{OUT} is probably approximately 3.8 V.

Figure 81 and Figure 82 show the leak current, I_{OUT}, at V_{OUT}, for an input of V_{IN}. Figure 81 and Figure 82 show the results for different samples.

Figure 81. Measured Leak Current I_{OUT} at V_{OUT} for an Input of V_{IN} [1]

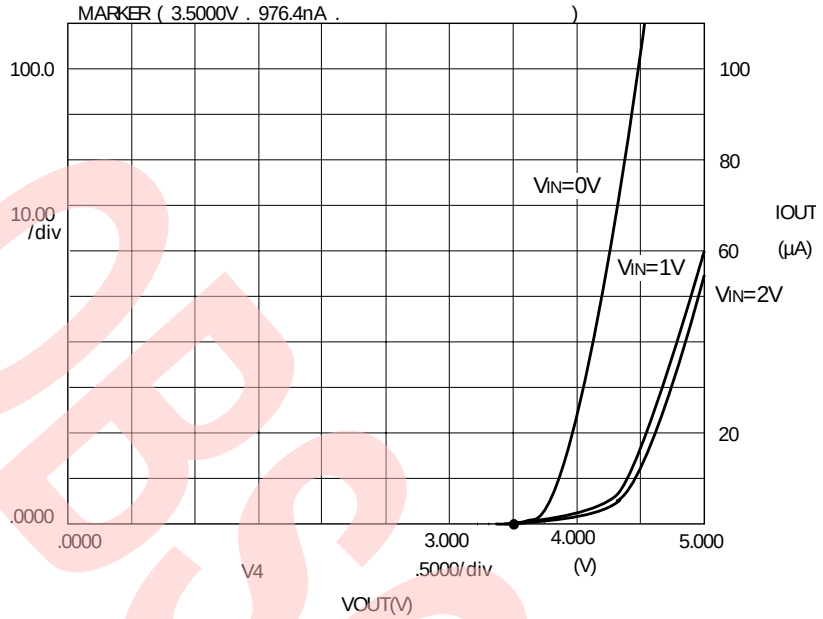
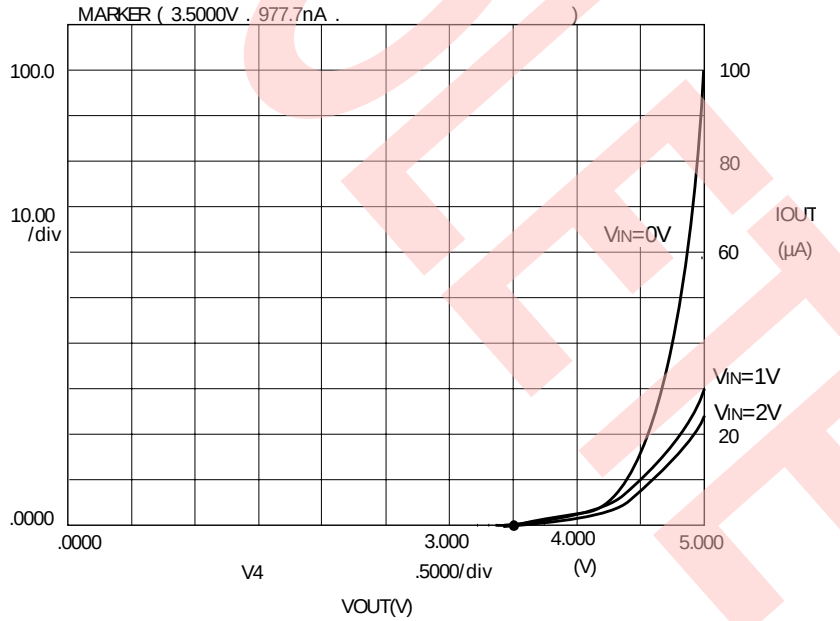


Figure 82. Measured Leak Current I_{OUT} at V_{OUT} for an Input of V_{IN} [2]

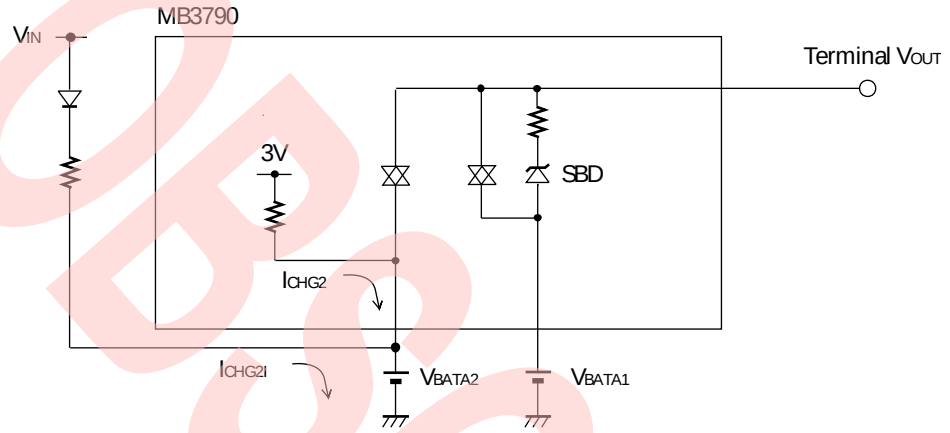


4.12 How to Charge the Secondary Battery to more than 3 V

This section explains how to charge the secondary battery to more than 3 V.

How to Charge Secondary Battery to more than 3 V

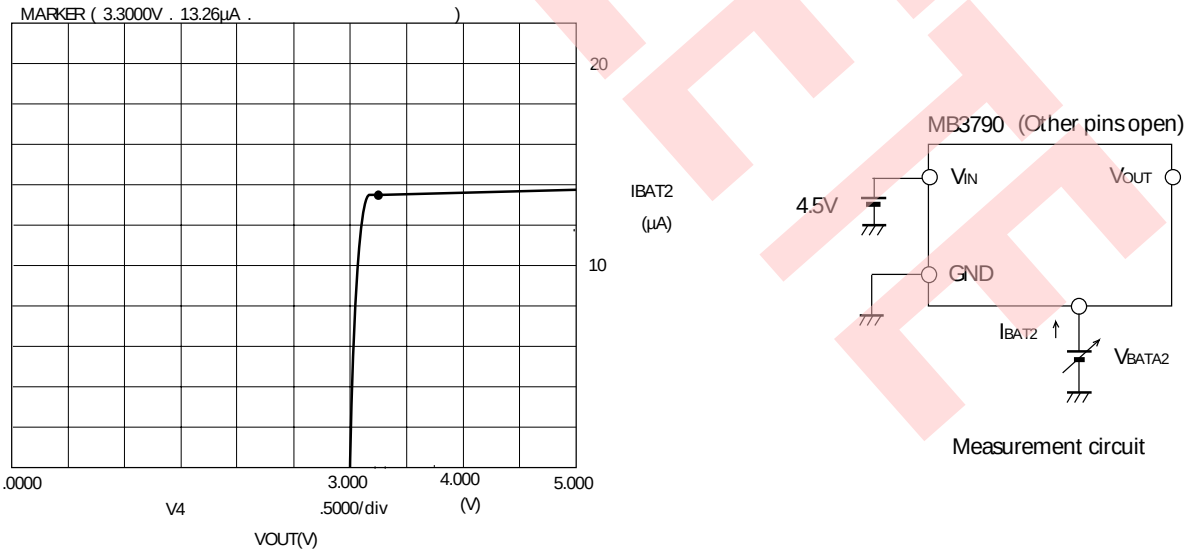
Figure 83. Equivalent Circuit (for charging the secondary battery to more than 3 V)



As shown in Figure 83, it is possible to charge V_{BAT} from V_{IN} through a diode and a resistor (R). It is necessary to select an appropriate resistor, since the required resistance varies depending on the capacitor (V_{BAT}) and the diode.

Note that the flow of leak current I_{BAT} into the IC will reduce the backup time. Figure 84 shows the measured leak current V_{BAT2} for V_{IN} values of more than 4.2 V. At 3.3 V or more, the value is approximately 13 µA.

Figure 84. Measured Leak Current V_{BAT2} for V_{IN} Voltages of more than 4.2 V



4.13 Relationship Between Capacitance and Output Delay Time

Connecting a larger capacitance to the terminal C_T will lead to a correspondingly longer discharging time. This section discusses the influence of a longer discharging time on the reset delay time.

Relationship Between Capacitance and Output Delay Time

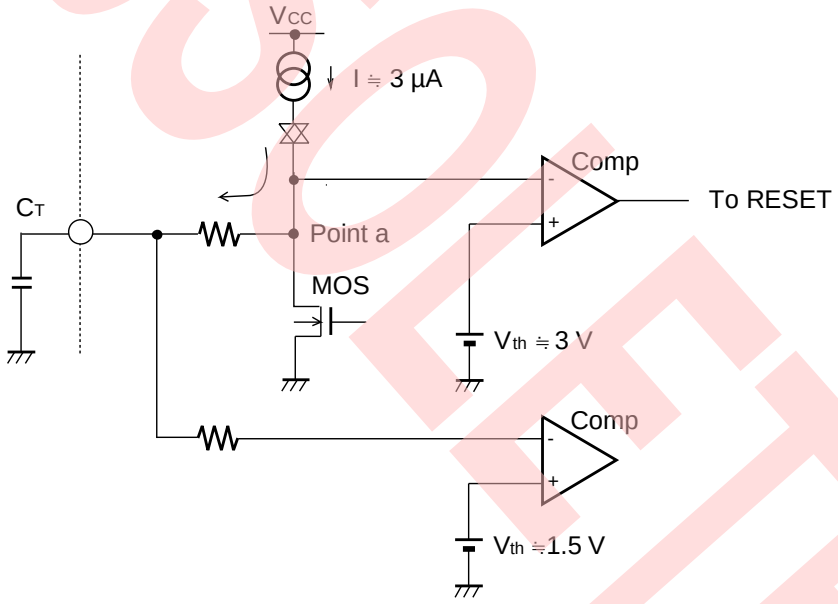
The MB3790 has a circuit configuration in which the capacitance that is connected to the terminal C_T does not affect the reset output delay time. In the block diagram included in the data sheet, the voltage at the terminal C_T directly goes to the comparator (with a Vth value of 3 V). As shown in Figure 85, there is actually a resistor inside the terminal C_T. This means that the voltage that is detected by the comparator for a Vth value of 3 V corresponds to the voltage at point a.

The MOS transistor is switched on when it detects a drop in V_{CC} (or the terminal V_{SENSE}). After determining the voltage at point a, the comparator with the Vth value of 3 V produces a reset output without waiting that C_T is discharged.

The standard specifies that the reset output delay time tpdR is a maximum of 10 µs.

If the voltage at V_{CC} drops to 0 V, the MOS transistor loses the capability of discharging (because of an increase in ON resistance). Note that the reset output will be delayed depending on the size of C_T.

Figure 85. Equivalent Circuit (setting the relationship between capacitance and output delay time)



4.14 Warning Remarks About Connecting a Diode to the V_{OUT} Terminal for Power Protection

This section contains some warning remarks about connecting a diode to the V_{OUT} terminal for power protection.

Warning Remarks About Connecting a Diode to the VOUT Terminal for Power Protection

[Observed behavior]

1. Suppose that a diode is connected to the V_{BAT1} terminal, as shown in Figure 86. Even if the voltage of the primary battery decreases, the voltage at the V_{BAT1} terminal (which corresponds to the voltage at point a in Figure 86) might not decrease in a high temperature setting, and there will be no alarm output.
2. As shown in Figure 87, an alarm is produced even in a high temperature setting if there is no diode.

Figure 86. Equivalent Circuit [1] (for connecting a diode to the terminal V_{OUT} for power protection)

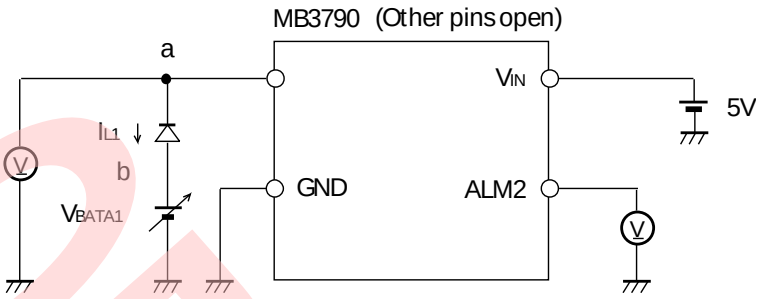
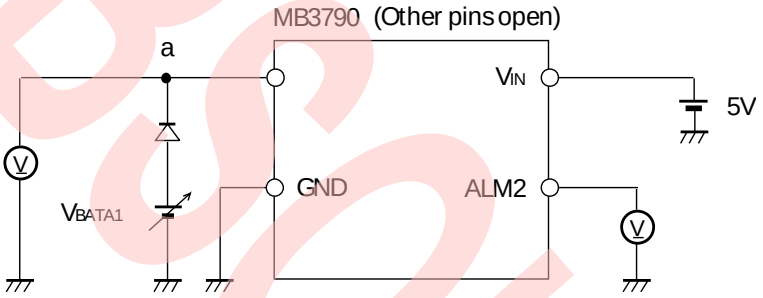


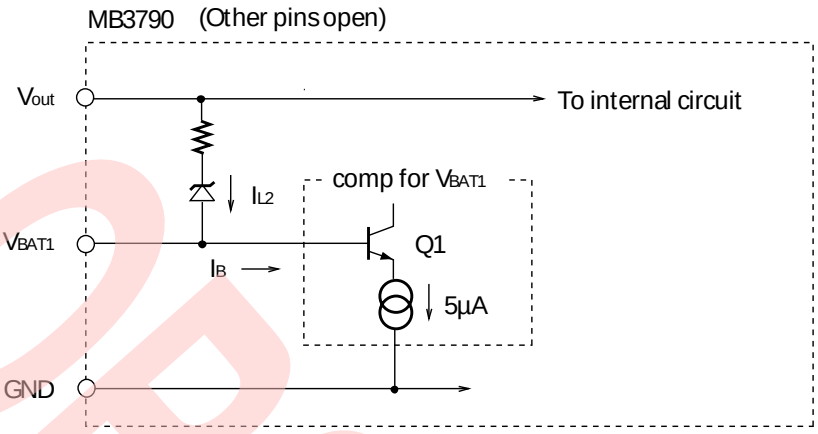
Figure 87. Equivalent Circuit [2] (when there is no diode connected to the terminal V_{OUT} for power protection)



[Probable Explanations for this Behavior]

1. The input unit of the terminal V_{BAT1} is configured as shown in Figure 88. When the V_{BAT1} terminal is open, a leak current (I_{L2}) flows through SBD under a backward bias. Due to I_{L2}, a base current is supplied to the NPN transistor (Q1).
2. Generally, the base current under which the NPN transistor (Q1) operates is large with respect to I_{L2}. For this reason, Q1 might not operate, which leads to an alarm output.
3. As the temperature rises, I_{L2} increases and Q1 will operate. In that case, there will be no alarm output.
4. At high temperatures, the MB3790 tends to increase the value of I_{L2}, which is approximately 20 nA at normal temperatures. (Refer also to the curves of the standard characteristics as included in the data sheet: Leak Current in Dependence of Ambient Temperature.)
5. If the value of I_{L2} increases because of a rise in the temperature, the voltage at terminal V_{BAT1} terminal also increases. This is because the increased I_{L2} increases the base current (I_B) in the NPN transistor (Q1). If the value of I_B exceeds a specified value, the voltage at the terminal V_{BAT1} will increase until it saturates. The saturation voltage differs (in the range between 3 V and 5 V) for different lots of the produced ICs, since the saturation level is affected by the characteristics of the NPN transistor.
6. If a diode is connected to the terminal V_{BAT} terminal as shown in Figure 86, a leak current (I_{L1}) with an amount of I_{L2} - I_B flows through the diode. Even when V_{BAT1} is set to 0 V at normal temperature, voltage saturates at point a, which means that the alarm stays in "H" status.

Figure 88. Equivalent Circuit (for the input unit of terminal V_{BAT1})



[Corrective Action]

Put a resistor with high resistance between the terminal V_{BAT1} (point a) and GND. The recommended value for this resistance is approximately 10 MW for Ta = 25°C. As the ambient temperature rises, reduce the resistance accordingly.

Note: Without a diode, there will be a leak current at high temperatures, which means that the battery might burst. Consult the battery manufacturer for details.

4.15 Handling Unused Terminals

Table 5 summarizes how to handle unused terminals in the MB3790.

Handling Unused Terminals

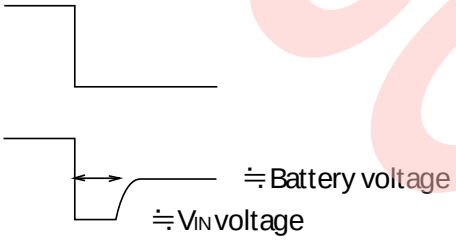
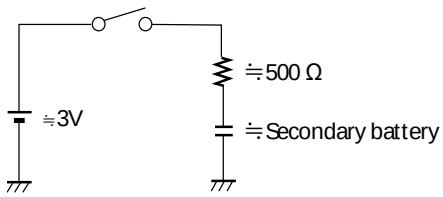
Table 5. Handling Unused Terminals in the MB3790

Terminal Name	Description
Terminal V_{BAT1}	GND or V_{IN} (This terminal can be opened for experimental purposes even if it is unused, but this will result in an undefined alarm output)
Terminal V_{BAT2}	OPEN
$\overline{ALARM1}$ / $\overline{ALARM2}$ terminal	OPEN
$\overline{RESET}$ / RESET terminal	OPEN
Terminal V_{SENSE}	OPEN
CTP terminal	-
CONTROL terminal	OPEN

4.16 Q&A Set Regarding the MB3790

This section provides a set of questions and answers regarding the MB3790.

Q&A Set Regarding the MB3790

Q&A Set Regarding the MB3790			
Q1	I am wondering whether we need to put a diode or resistor between the primary battery and the MB3790. Would it be better to add a protective circuit to account for a possible malfunction in the MB3790?	A1	That depends on the battery. Since it may not be possible to identify a malfunction mode of the MB3790, it would be safer to add a protective circuit. Please consult also the manufacturer of the battery on this topic. We have no particular recommendation for a circuit that would be especially suitable for this purpose.
Q2	As the value of V_{IN} decreases, the output of V_{OUT} is usually obtained by switching from the V_{IN} voltage to the battery. However, if there is a sharp drop in V_{IN}, it will take time before the switch becomes effective, and even after the value of V_{IN} decreased, V_{OUT} will continue to provide the voltage for V_{IN} for a short period. What would be the appropriate corrective action in this situation?  (At a V_{IN} fall rate of 2.5 V/ms, it takes about 20 ms before V_{OUT} supplies a voltage that is approximately equal to the battery voltage.)	A2	If the value of V_{IN} decreases, V_{OUT} follows V_{IN} because of the difference between the ON and OFF timing of the internal transistor of the IC. Increase the V_{IN} fall time by means of increasing the capacitance between V_{IN} and GND. (To provide a secure backup operation in the case of a momentary power failure requires that the time in which V_{IN} falls from 5 V to 0 V is at least 50 µs.)
Q3	I would like to connect the RESET terminal to the CS terminal of the SRAM. According to the data sheet, the RESET output voltage during a backup is up to 0.4 V. Most SRAMs use a certain current level for retaining data and require that the CS is not higher than 0.2 V. Can these SRAMS be connected as they are?	A3	The maximum value of 0.4 V assumes that there is a 3 mA current flowing into the RESET terminal (refer to the data sheet: "Standard Characteristics Curves - VCL Characteristics at RESET Terminal"). If the input current is not at least 5 mA, the value of 0.2 V can not be achieved. It is necessary to set up the individual configuration according to the input current that flows in the circuit.
Q4	While the standard states that the charging current I_{CHGH} for battery 2 requires V_{CHG} = 3.3 V, the output V_{CHG} for battery 2 is in fact 2.8 V (2.95 V maximum). These requirements seem to contradict each other.	A4	The standard refers to a leakage that occurs when a 3.3 V battery is forcibly connected to the terminal V_{BAT2}.
Q5	How long is the charging time for the secondary battery?	A5	Ask the battery manufacturer for the charging time that would be required for charging with the circuit as shown below. 

Q&A Set Regarding the MB3790			
Q6	The mode of the terminal V_{SENSE} is either OPEN or GND according to the data sheet "Application Examples - How to Produce Reset Signals Forcibly". Are "H" mode (V_{IN} voltage) or "L" mode supported as well? (H: V_{IN} voltage)	A6	The "H" or "L" mode is not supported. By setting up a direct connection (short) between the terminals V_{IN} and V_{SENSE}, a structure is created in which RESET changes to the H level only when the current at V_{IN} goes down to 1.24 V (this is because V_{IN} is directly connected to the input of the comparator). On the other hand, when the current at V_{IN} reaches 1.24 V, the reference voltage has decreased, and did not stay at a level of 1.24 V value. This makes monitoring the voltage of the power supply impossible.
Q7	I have a question about a malfunction of the alarm terminal. When there should theoretically be an "H" output under the condition V_{BAT1} = 3.3 V, why would there be an "L" output?	A7	We recommend to put 0.022 µF capacitors between the terminal V_{IN} and GND and between the terminal V_{OUT} and GND, as mentioned in the data sheet "Standard Connection Examples". Without these capacitors, the operation of the alarm terminal might be unstable, which would sometimes result in a malfunction.

4.17 Comparison Between the MB3780A and the MB3790

Table 6 shows a comparison between the MB3780A and the MB3790.

Comparison Between the MB3780A and the MB3790

Table 6. Comparison Between the MB3780A and the MB3790

Parameter		IC for Battery Backup	
		MB3780A	MB3790
Input voltage range		0 to 6 V	0 to 5.5 V
Process		Bipolar type	Bi-CMOS
Value for detecting a decrease in input voltage		4.2 V / 4.3 V	
Current in the input circuit under no-load condition		1 mA (standard)	50 µA (standard)
Output drive current		200 mA	
Difference between input and output voltage		200 mV	(RON=0.5 Ω)
Output current during backup		0.5 mA (maximum)	
Leak current during backup		0.5 µA or less	
Power-ON reset	Logic	Positive logic	Positive / negative logic
	Output mode	Open collector	CMOS
Function for detecting voltage decreases in the primary battery		2.65 V / 2.37 V	
Function for charging the secondary battery		Built-in function	
Compatibility with thin packages		SSOP20	

Note: The shaded areas indicate that there are differences between the parameters for the MB3780A

5 MB3793 Applications

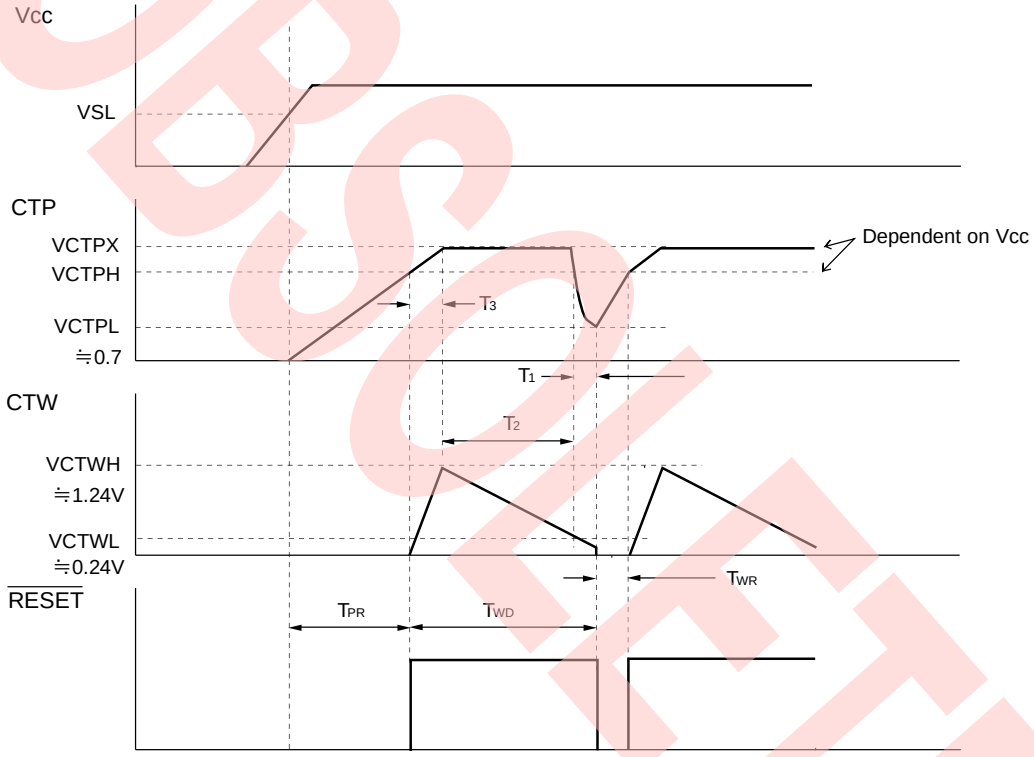
5.1 Meaning of Values A to D

The meaning of the values A to D are explained in the data sheet "Standard Connection Diagrams". These values are used for calculating various time settings. As these values depend on the voltage of the power supply, they vary from one series to another. This section describes how the values for A-D were obtained.

5.1.1 Meaning of the Values A to D

Figure 89 is a chart of the timing for the V_{CC}, CTP, CTW, and $\overline{RESET}$ signals.

Figure 89. Chart of the Timing for the V_{CC}, CTP, CTW, and $\overline{RESET}$ Signals



The mathematical relationships between the parameters are explained below.

Power-ON Reset Time, T_{PR}

This is the time that is required to charge capacitor CTP to the voltage of VCTPH at a constant current of I_{ctp1}.

$$T_{PR} = \frac{VCTPH}{Ictp1} \times CTP \fallingdotseq A \times CTP$$

Monitoring Time of the Watchdog Timer, T_{WD}

This value is the sum of three time values: time T_1, which is the time required to discharge capacitor CTW from voltage VCTWH to VCTWL at a constant current of I_{ctw1}; time T_2, which is the time required to let capacitor CTP charge from voltage VCTPX to VCTPL; and the time required to charge the capacitor from VCTPH to VCTPX at a constant current of I_{ctp2}.

$$T_{PR} \approx T_1 + T_2 + T_3$$

$$\approx \frac{(VCTWH - VCTWL)}{Ictw1} \times CTW + CTP \times R \times \log(VCTPX / VCTPL) + CTP \times \frac{(VCTPX - VCTPH)}{Ictp1}$$

$$\approx B \times CTW + C \times CTP$$

t should be noted that R refers to the resistance of the MOS transistor. A part with a model number that contains the extension -A is a circuit that allows a calculation with C = 0.

Reset Time of the Watchdog Timer, T_{WR}

This is the time that is required to charge capacitor CTP to the voltage of VCTPH from VCTPL at a constant current of about ten times I_{ctp1}.

$$T_{WR} = \frac{(VCTPH - VCTPL)}{10 \times Ictp1} \times CTP \approx D \times CTP$$

5.2 Clock Timing

This section explains the timing of the clock.

Related data sheet(s): "Timing Chart 1 - Basic Operation"

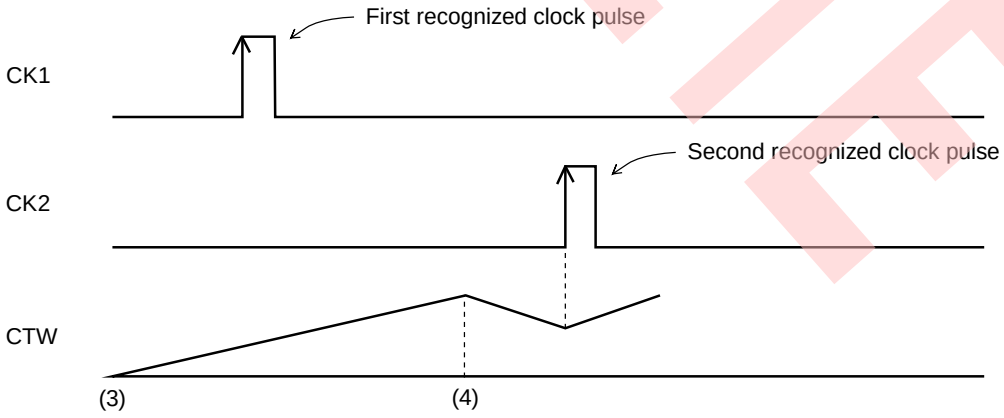
5.2.1 Clock Timing

The CK terminals (CK1 and CK2) provide a latch circuit for detecting any rise in signals. No operation occurs if the "H" level is maintained.

The latch circuit is designed in such a way as to read CK1 and CK2 in sequence: first CK1, then CK2.

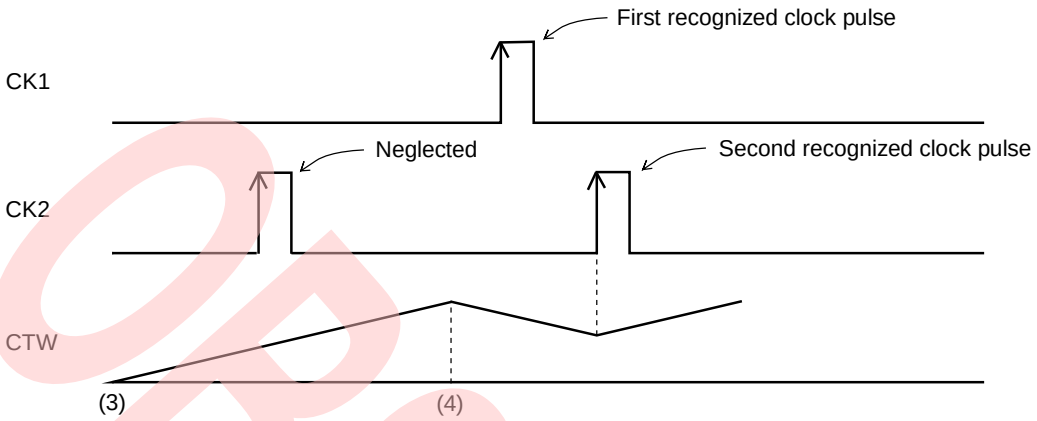
If there is a clock between points (3) and (4), the operation is as follows:

One Clock at CK1



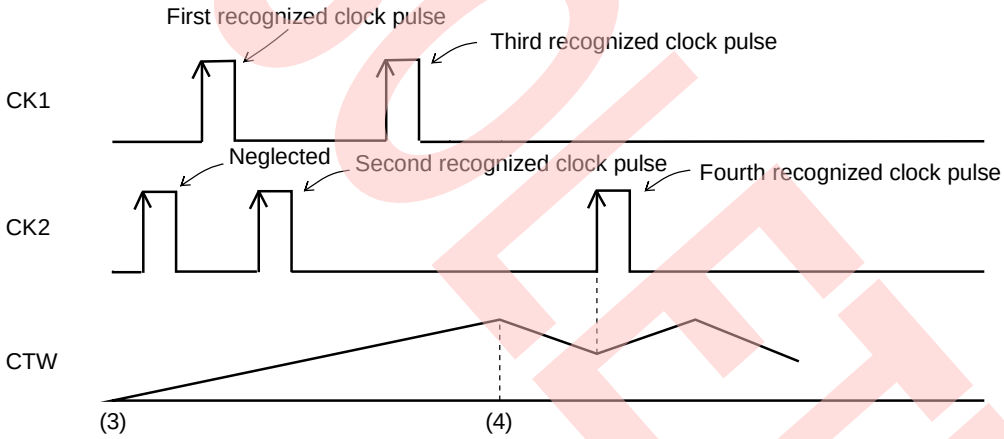
One Clock at CK2

Counting always begins with CK1.



More than One Clock

The second recognized clock pulse makes charging possible, but as the circuit is already in charging mode from the beginning, no change takes place.



Since the first clock pulse after the rising signal of INH comes from CK2, it is neglected. Counting begins with the next clock signal from CK1.

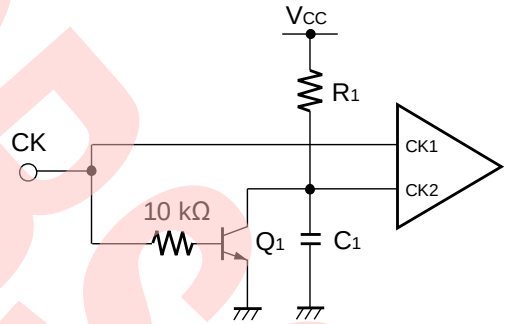
In the period between the points (7) and (8) mentioned in the data sheet " Timing Chart 1 Basic Operation", counting also begins with the clock pulse from CK1.

5.3 Recommended Circuit for Limiting f_{max}

This section presents a recommended circuit for limiting fmax.

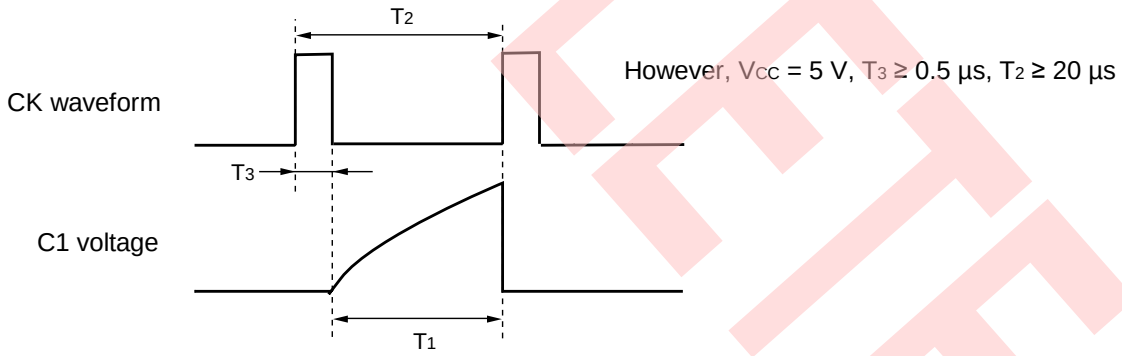
Recommended Circuit for Limiting fmax

Figure 90. Equivalent Circuit (recommended circuit for limiting f_{max})



During clock input at the CK terminal, an extremely low value of T_2 will prevent that the C_1 voltage reaches the clock input threshold of 1.9 V and a reset signal is produced. The value of T_1 can be determined according to the following equation.

$$T_1 \approx 0.7 C_1 R_1$$



Because of fluctuations, the value during the period described by

$$\approx 0.33\, C_1 R_1 \quad T_1 \leq (\approx 0.7 C_1 R_1)$$ will be undefined.

[Sample Settings]

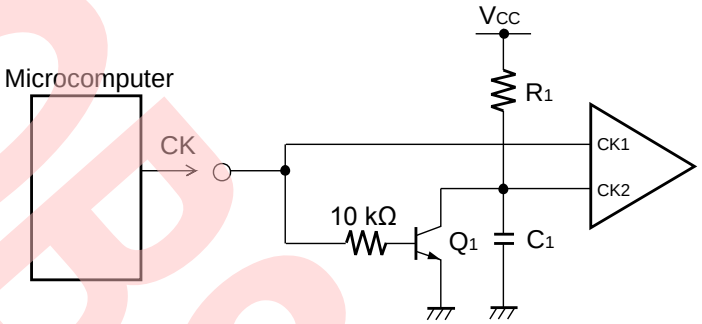
C	R	T_1
0.01 µF	10 kΩ	70 µs
0.1 µF	10 kΩ	700 µs

5.4 Timing for the Circuit Limiting f_{max}

This section explains the timing for the circuit limiting f_{max}.

Timing for the Circuit Limiting fmax

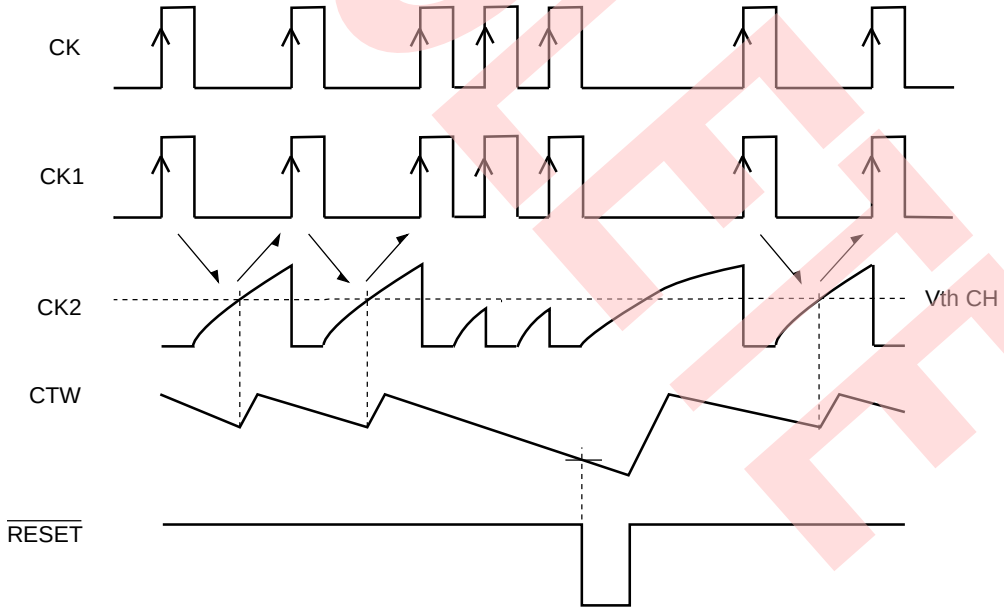
Figure 91. Equivalent Circuit (timing for the circuit limiting f_{max})



For CK monitoring, only a single system needs to be monitored as seen from the microcomputer, while two systems need to be monitored from the MB3793 side. Therefore, CTW is changed to charging mode each time there is a rising signal at CK2.

Note that for every two clocks pulses from the microcomputer side, CTW changes to the charging mode described in the data sheet "Timing Chart 3 - Single-Clock Input Monitoring".

Figure 92. Timing for the Circuit Limiting f_{max}



5.5 Handling Unused Terminals

Table 7 summarizes how to handle unused terminals in the MB3793.

Handling Unused Terminals

Table 7. Handling Unused Terminals in the MB3793

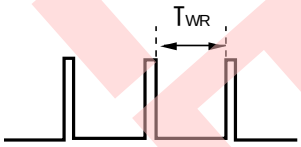
Terminal Name	Description
$\overline{\text{RESET}}$ terminal	OPEN
CTW terminal	GND
CTP terminal	OPEN
INH terminal	GND
CK1 terminal	GND or V_{CC}
CK2 terminal	GND or V_{CC} (Connected to the CK1 terminal if only the CK1 terminal is used)

[1. What Happens if the CTW Terminal is OPEN]

In this case, the reset output is undefined.

The Meaning of the Term "undefined" in this Connection is as Follows:

This term means that it is unknown whether the "H" or the "L" level is adopted or what voltage will be created. These facts depend on sample fluctuations and the used peripheral circuit. Generally, the output becomes undefined when a MOS-type input terminal is set OPEN. For your reference, we have included the results of experiments of samples in which the reset output changes from "H" to " L" levels in intervals of t_{WR} because of the capacitance within the terminal. Identical results were obtained, regardless of whether there was any clock input. We can, however, not guarantee the following operation:



[2. What Happens when the CTW Terminal is Grounded]

The reset terminal switches to the "H" level. The same operation takes place when the INH terminal changes to the "H" level.

[3. What Happens when the CTP Terminal is OPEN]

The reset terminal switches to the H level (the level of the CTP terminal is approximately equal to the voltage at V_{CC}).

If the tPR is 0 and if the voltage reaches 4.3 V during a rise in the voltage at V_{CC}, the reset is abruptly canceled. Likewise, the reset terminal is set to the "H" level if t_{WR} becomes 0 and there are no clock pulses.

[4. What Happens if the CTP Terminal is Grounded]

In this case, the reset terminal is set to the "L" level (The IC will not operate until there is a rise at the CTP terminal).

[5. What Happens if the INT Terminal is OPEN]

The reset output becomes undefined. (The experimental results for the samples show that the operation of the circuit is unstable when there is a change between the "H" and "L" level.)

[6. What Happens if the V_{CC} or GND Terminal are OPEN]

In this case, the reset terminal switches to the "L" level. The same operation takes place even if voltage is applied to the CK or INT terminal. (The reset terminal requires no pull-up resistance because of the CMOS output buffer.)

While the situations described under points 1 to 6 above are generally not recommended, there will nevertheless be no malfunction because of an excessive load on the IC. The situation described under point 2 can in fact effectively be used in order to use the MB3793 for monitoring the voltage of the power supply (that is, without using any watchdog timer). Refer also to Section 5.6 "Typical Circuit for Monitoring Only the Voltage of the Power Supply".

5.6 Typical Circuit for Monitoring Only the Voltage of the Power Supply

Figure 93 shows a typical circuit that might be used for only monitoring the voltage of the power supply. In this case, special considerations are required with respect to the watchdog timer, such as considering the effect of using other ICs. The timing of the circuit is shown in Figure 94.

Typical Circuit for Monitoring Only the Voltage of the Power Supply

Figure 93. Typical Circuit for Monitoring Only the Voltage of the Power Supply

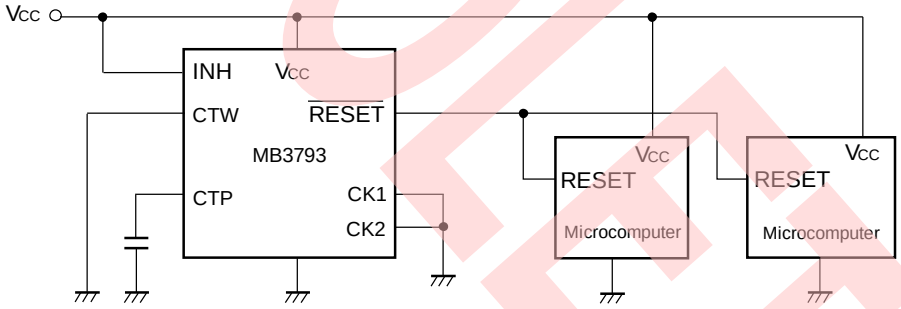
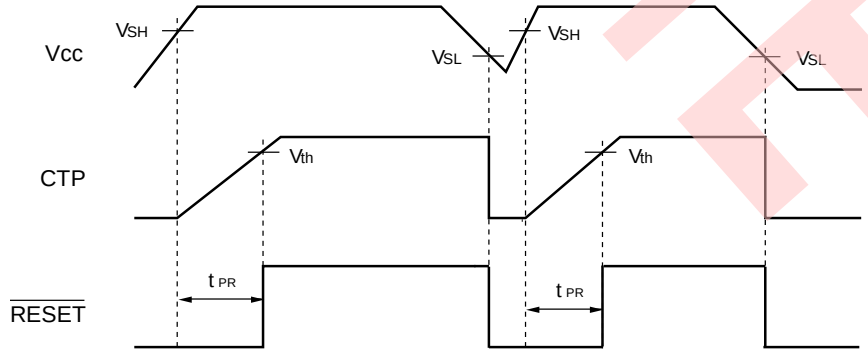


Figure 94. Chart of the Timing of a Circuit for Monitoring Only the Voltage of the Power Supply

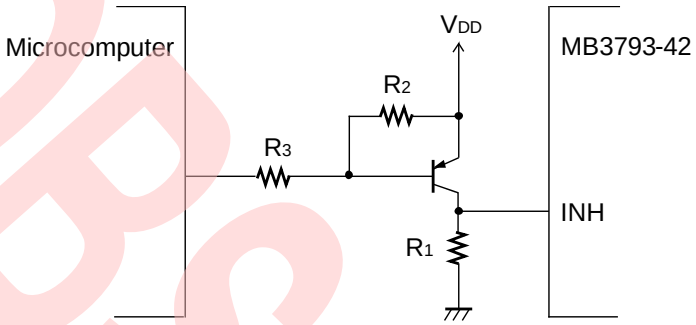


5.7 Specific Ways of Checking External Circuits of the MB3793-42

This section explains the recommended resistance values that are to be used if the INH input provides such an interface as shown in Figure 95. As R_2 and R_3 are already specified by the microcomputer and transistor, this section covers the question how to determine R_1.

5.7.1 Specific Ways of Checking External Circuits of the MB3793-42

Figure 95. Example of an External Circuit for INH Input



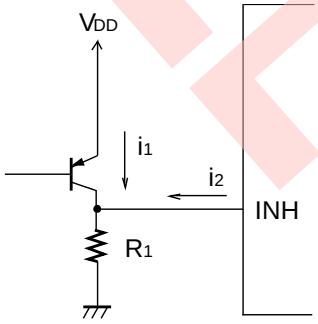
The following cases 1 and 2 describe how to choose the minimum and maximum values for R_1.
The optimum value can then be chosen considering current consumption and other parameters.

[1. When INH is in " L" Status (transistor is off)]

Assuming that i_1 stands for the transistor's leak current, i_2 for the leak current from INH, and V_{th} (min.) for the minimum threshold of INH, the value of R_1 should be chosen so that it meets the following requirement:

$$(i_1 + i_2) \times R_1 < V_{th} \text{ (min.)}$$

(For Ta = 25 °C, i2 (max.) is 1 µA and Vth (min.) is 0.8 V.)



[2. When INH is in "H" Status (the transistor is on)]

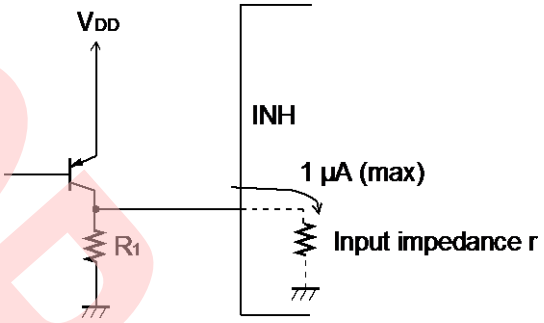
When 5 V are applied to INH and the input current is 1 µA (max.), the input impedance of INH, r, can be determined as follows:

$$r = \frac{5V}{1\mu A}$$

Assuming that IR stands for the combined resistance of R_1 and r, R_{ec} for the ON resistance of the transistor, and V_{th} (max.) for the maximum threshold of INH, the value of R_1 should be chosen so that it meets the following requirement:

$$\frac{IR}{IR + Rec} > V_{th}(max.)$$

(For Ta = 25°C, V_{th} (max.) is 3.5 V and r is approximately 5 MΩ.)



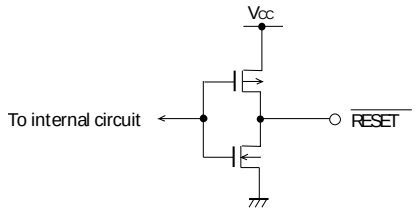
Tip: As there is little leakage from INH, it is also possible to directly connect INH and the microcomputer. However, an open drain can not be used.

5.8 Equivalent Circuits for the Use as Input / Output Unit of the MB3793

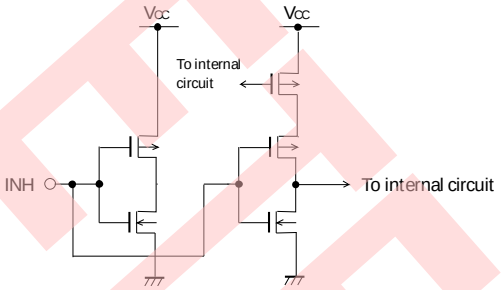
The following are equivalent circuits for the use as input/output unit for the MB3793.

Equivalent Circuits for the Use as Input / Output Unit of the MB3793

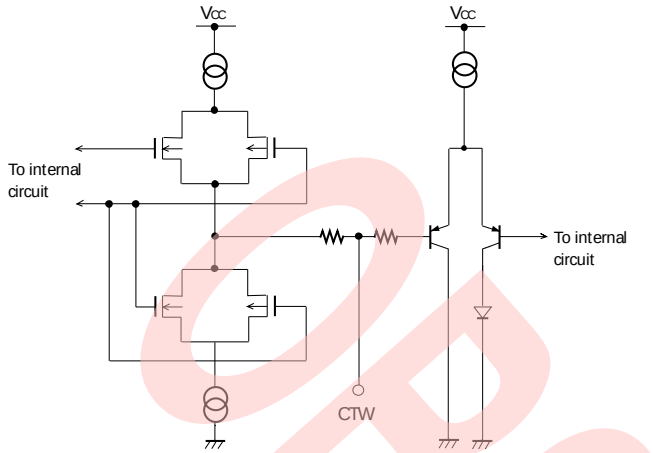
<RESET terminal>



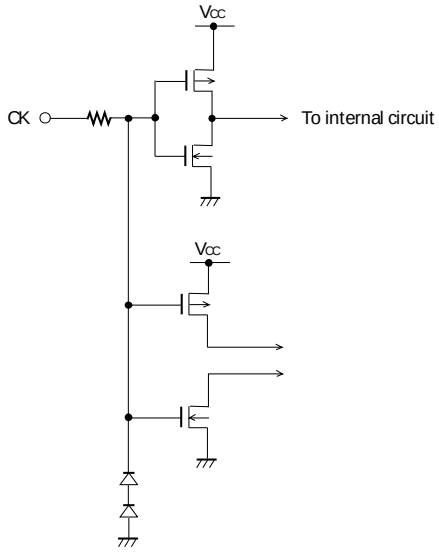
<INH terminal>



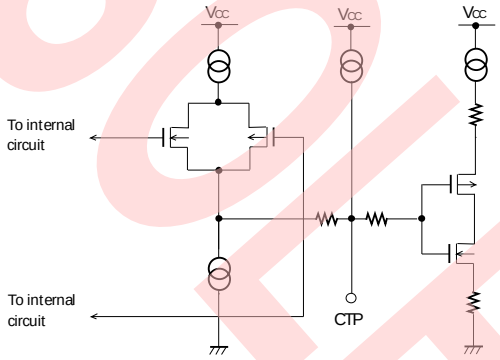
<CTW terminal>



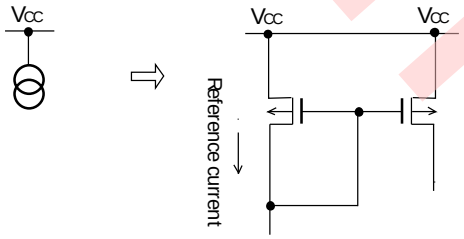
<CK terminal>



<CTP terminal>



Note: Circuits that are marked with a current symbol in the chart below are constant current circuits of current mirror type that use PNP transistors.



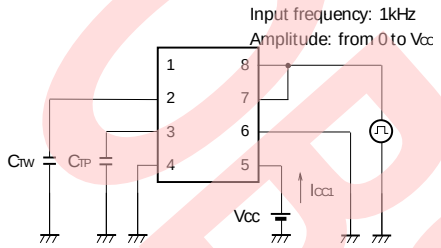
5.9 Circuits for Measuring the Electric Characteristics of the MB3793-42

This section describes circuits for measuring the electric characteristics of the MB3793-42.

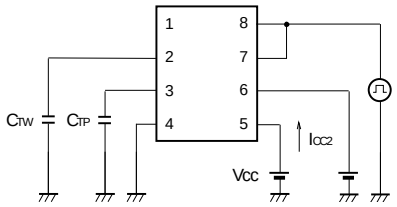
■ **Circuits for Measuring the Electric Characteristics of the MB3793-42**

V_{CC} = 5 V (MB3793-42) Ta = 25°C C_{TP} = 0.1 µF C_{TW} = 0.01 µF

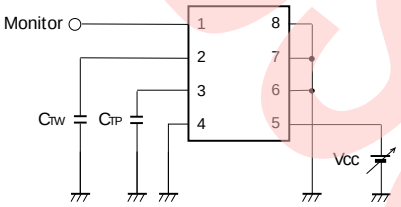
<Current I_{CC1} from the power supply>



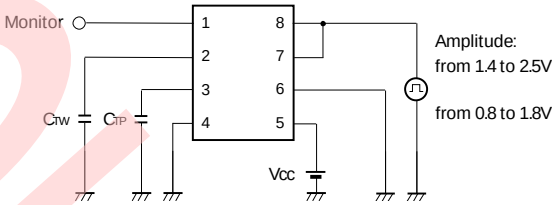
<Power ICC2 from the power supply>



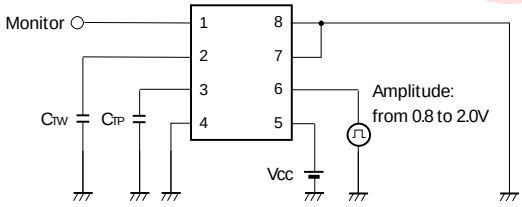
<Detection voltage V_{SL} / V_{SH} / V_{SHYS}>



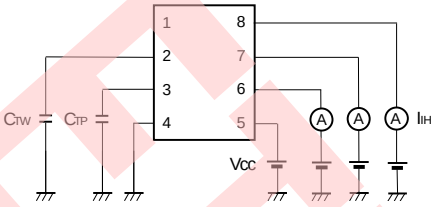
<Input current I_{IH}>



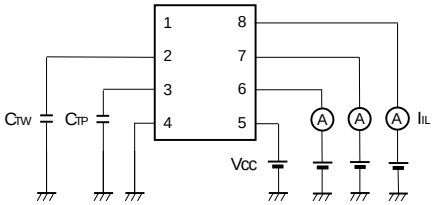
<Threshold voltage for input inhibition Vth_{IN}>



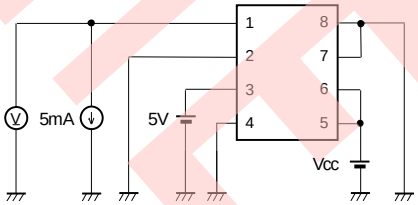
<Input current I_{IH}>



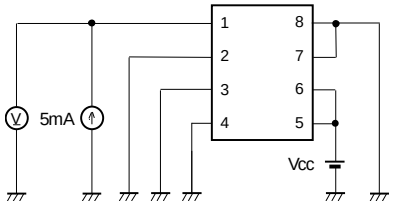
<Input current I_{IL}>



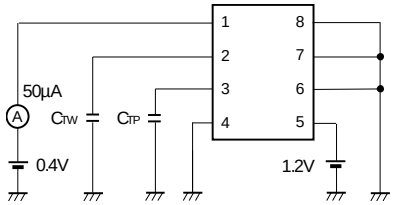
<Reset output voltage V_{CH}>

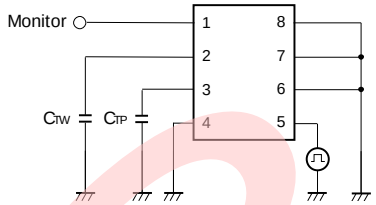
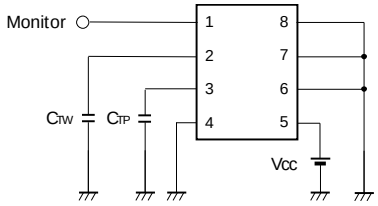
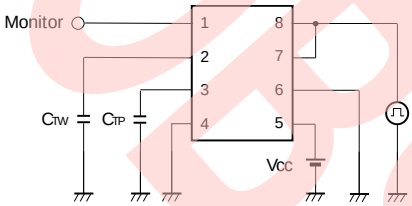
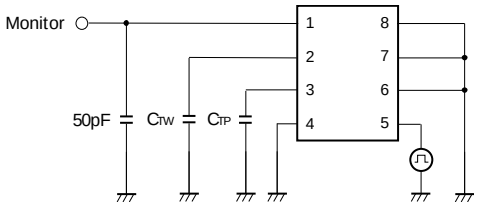


<Reset output voltage V_{CL}>



<Minimum voltage of the reset output for the power supply V_{CCL}>



<table>
<tr><th colspan="2">V_{CC} = 5 V (MB3793-42) Ta = 25°C C_{TP} = 0.1 µF C_{TW} = 0.01 µF</th></tr>
<tr><td><Hold time t_{PR} for a power-ON reset>
 
</td><td><Monitoring time t_{WP} of the watchdog timer>
<Reset time t_{WR} for monitoring with the watchdog timer>
 
</td></tr>
<tr><td><Pulse width tckw of the CK input>
 
</td><td><Transition time of the reset output t_{TLH}>
 
</td></tr>
</table>

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	TAOA	04/19/1999	Initial release. Published as Spansion AM41-10101-1E.
*A	5863658	TAOA	09/08/2017	Migrated from Spansion format to Cypress format.
*B	6399420	YOST	12/03/2018	Obsoleted.

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