AN2041

# Understanding PSoC® 1 Switched Capacitor Analog Blocks

**Author: Dave Van Ess**
**Associated Project: Yes**
**Associated Part Family: CY8C29x66, CY8C28xxx, CY8C27x43, CY8C24x23A,CY8C24x94**
**Software Version: PSoC® Designer™ 5.2**
**Related Application Notes: For a complete list of the application notes, click here.**

AN2041 explains the operation of PSoC® 1's versatile switched capacitor analog blocks, and provides practical examples of their use. Switched capacitor (SC) blocks are one of the two key components of PSoC 1's analog functionality, and can be reconfigured to perform many useful functions. This application note also explains the theory and application of these switched capacitor analog blocks.

## Contents

Introduction ..... 2
Moving Charge ..... 2
Active Switched Cap Circuits ..... 3
Theme and Variation ..... 3
- Non-Inverting Amplifier ..... 4
- Comparator ..... 4
- Integrator ..... 5
- Differentiator ..... 6
- Additional Switched Cap References ..... 6
- Comparator as 2-bit ADC ..... 7
- Real Analog-to-Digital Conversion ..... 7

Switched Capacitor PSoC Blocks ..... 8
- Type C Switched Capacitor Blocks ..... 8
- Type C Switched Cap Block Parameters ..... 9
- Type D Switched Capacitor Blocks ..... 9
- Type D Switched Cap Block Parameters ..... 10

SC Blocks and PSoC 1 Architecture ..... 11
PSoC 1 SCBlock User Module ..... 11
Additional Applications ..... 12
Summary ..... 15
Related Application Notes ..... 16
Appendix A: Control Registers for a Type C Switched Capacitor Block ..... 17
Appendix B: Control Registers for a Type D Switched Capacitor Block ..... 17
Appendix C: A Input Multiplexer Connections ..... 17
Appendix D: C Input Multiplexer Connections ..... 18
Appendix E: B Input Multiplexer Connections ..... 18
Appendix F: C Code: 2-Bit ADC Example Project ..... 19
Appendix G: SC-Block Applications Cook Book ..... 21
Worldwide Sales and Design Support ..... 28

## Introduction

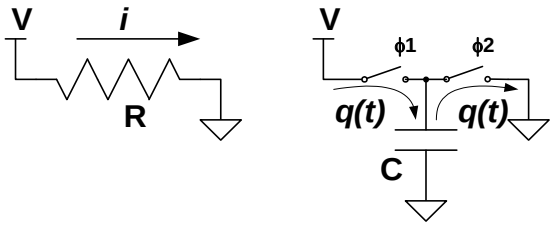
Analog circuit design involves the use of resistors, capacitors, and integrated active devices. It is the nature of integrated circuitry that small, accurate resistors are harder and more expensive to build than small, accurate capacitors. Because making capacitors is easier and cheaper, techniques are developed to use capacitors to build accurate analog circuitry. These techniques have led to the use of switched capacitor (SC) architectures. These architectures control the movement of charge between capacitors with the precise timing of switches, instead of relying on resistors. Switched capacitor analog blocks are made up of a set of switched capacitors surrounding an opamp. The switched capacitors allow configuration of the block in many different modes, including as a comparator, amplifier, integrator, differentiator, ADC, and more. This application note provides the following:

- A brief tutorial on switched capacitor techniques.
- A detailed description of the switched capacitor PSoC blocks.
- Examples of practical circuits using these blocks.
- Information on quick settings for a particular application – Appendix G: SC-Block Applications Cook Book

## Moving Charge

Analog circuit design is all about controlling the movement of charge between voltage nodes. Figure 1 shows charge movement using a resistor and using a switched capacitor. In the case of the resistor, current flow is created by the voltage differential across the resistance. In the case of the capacitor, current flow is created by electron accumulation from the higher voltage node and discharge into the lower voltage node.

Figure 1. Two Methods for Moving Charge




Equation 1 shows the current flow from a voltage potential to ground through the resistor, a manipulation of Ohm's law, as shown in Figure 1. This current is a linear, continuous movement of charge.

$$i = \frac{V}{R} \qquad \text{Equation 1}$$

In the case of the switched capacitor, current is moved by charging and discharging the capacitor. When the $\Phi_1$ switch is closed and the $\Phi_2$ switch is open, the capacitor charges to the full potential. The equation of the charge stored is shown in Equation 2.

$$q = CV \qquad \text{Equation 2}$$

When the $\Phi_1$ switch is opened and $\Phi_2$ switch is closed, all of this stored charge moves to the ground node. For each precise sequential pair of switch closures, a quantum of charge is moved. If these switches are controlled at the frequency $f_s$, the charge quanta also move at this frequency. Equation 3 shows the current due to the repetitive movement of charge across the switched capacitor.

$$i = q/t = f_s q = f_s CV \qquad \text{Equation 3}$$

Unlike in the case of the resistor, this current is not a continuous movement of charge. The charge moves in clumps (quanta). This is not a problem for a sampled system where the signal is sampled at the end of each sample cycle. The following equation shows that a switched capacitor is equivalent to a resistor when they have equivalent ratios of voltage drop against delivered current. We can then replace a series resistor with a parallel switched capacitor.

$$\frac{V}{i} = R = \frac{1}{f_s C} \qquad \text{Equation 4}$$

The equivalent resistance is inversely proportional to the capacitance and the switching frequency. The relative value of the resistance may be altered, merely by changing the switching frequency. The larger "C" is, the larger the charge quanta. This results in more current and a smaller equivalent resistance. Making "$f_s$" bigger causes more quanta to be transferred per unit time. This results in a higher current and a lower effective resistance.

The timing requirements for $\Phi_1$ and $\Phi_2$ are:

- Never close the $\Phi_1$ and $\Phi_2$ switches at the same time.
- Give the $\Phi_1$ switch time to open before closing the $\Phi_2$ switch.
- Give the $\Phi_2$ switch time to open before closing the $\Phi_1$ switch.
- When selecting a sampling rate, allow enough time for the circuitry to fully charge and discharge in the allotted phase cycle.

## Active Switched Cap Circuits

Simply moving charge is useful, but most circuits require gain. Figure 2 shows a simple architecture for a fixed gain amplifier. It consists of an opamp, an input capacitor ($C_A$), a feedback capacitor ($C_F$), and five switches.

Figure 2. Switched Cap Fixed Gain Inverting Amplifier

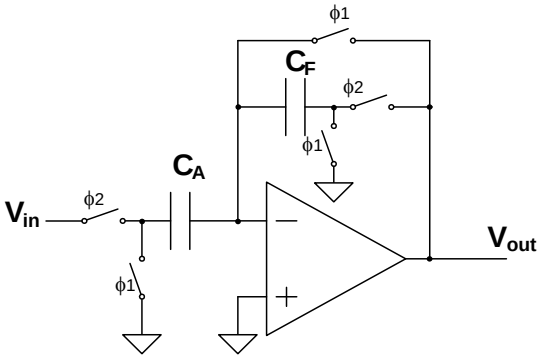
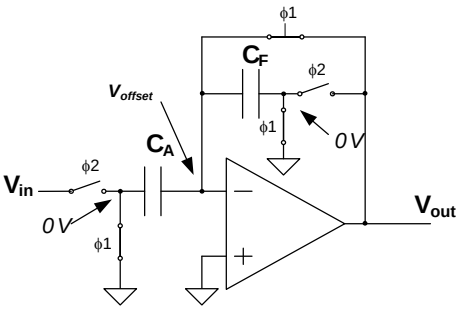



Figure 3 shows that three switches are closed during the $\Phi_1$ phase.

Figure 3. Configuration During $\Phi_1$ Phase

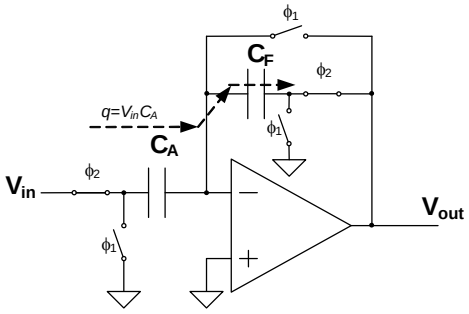



During $\Phi_1$ phase, the opamp is configured as a follower. The opamp's negative feedback drives the voltage at the inverting input towards ground. The voltage will not be exactly ground, because all opamps have input offset error ($V_{offset}$). The input side of $C_A$ is pulled to ground, as is the output side of $C_F$. The offset voltage is added to both capacitors. This removes the effect that this offset error may have on the output during the charge transfer phase. Because this offset removal happens without intervention during the acquisition phase, it is known as an "autozero" adjustment.

For a transition period between the phases, all of the switches are open. This period is brief and the charge stored on the capacitors does not change. This transition period is known as "dead band".

Figure 4 shows the configuration of the switches and the flow of current during $\Phi_2$ phase.

Figure 4. Configuration During $\Phi_2$ Phase




Equation 5 defines the amount of charge needed to excite the input capacitor to the input voltage $V_{in}$.

$$q = V_{in} C_A \qquad \text{Equation 5}$$

This charge will take the only available path: through the feedback capacitor. Therefore, the feedback capacitor receives the same charge transfer. Equation 6 describes the output voltage change due to this charge transfer.

$$V_{out} = -\frac{q}{C_F} \qquad \text{Equation 6}$$

Equation 7 combines Equation 5 and Equation 6 to produce the transfer function for this amplifier.

$$Gain = \frac{V_{out}}{V_{in}} = -\frac{C_A}{C_F} \qquad \text{Equation 7}$$

The result is an inverting amplifier with a gain set by the ratio of its two capacitors.

Note that the output voltage is only correct at the end of $\Phi_2$ phase. The output voltage will be near ground (at $V_{offset}$) during $\Phi_1$ phase. For this reason, the sampling of switched cap circuit outputs muse be timed properly.

The phase $\Phi_2$, in this case, is also referred to as signal acquisition phase as the input capacitor acquires the input signal. Phase $\Phi_1$ is referred to as charge transfer phase as the charge acquired by input capacitor is transferred to output.

## Theme and Variation

The switched cap topology can be modified to achieve more useful configurations. Some of these are described below.

Note that in the explanation to all the below circuits, following assumptions are made:

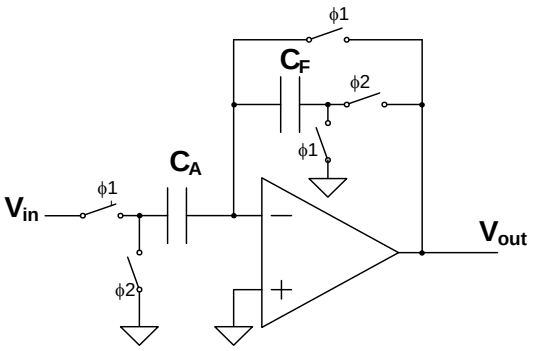
1. Zero input offset voltage
2. Mentioned voltages are referenced to analog ground (AGND).

3. The current direction is drawn assuming input voltage is greater than AGND value (which is same as opamp's non-inverting terminal voltage). If the input voltage is less than AGND, the current direction is reversed.

## Non-Inverting Amplifier

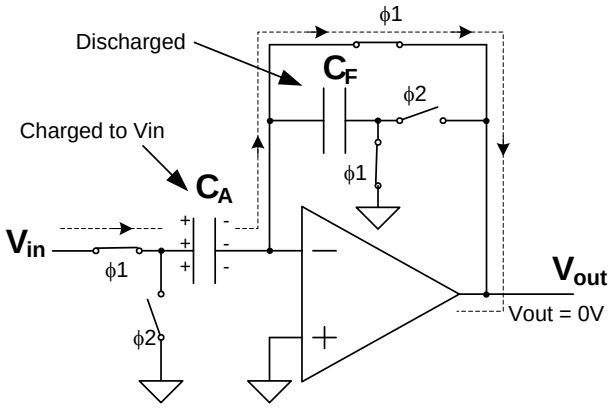
Initially, Figure 5 appears to be an exact copy of Figure 2. A closer examination shows that the input switches have swapped phase. That is, $\Phi_1$ is now the signal acquisition phase and $\Phi_2$ is the charge transfer phase. This configuration creates a non-inverting amplifier.

Figure 5. Switched Cap Non-Inverting Amplifier



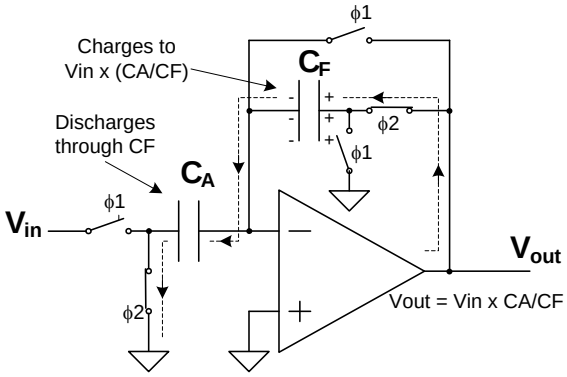

In this configuration, the input capacitor $C_A$ acquires $V_{in}$ during the acquisition phase $\Phi_1$ as shown in Figure 6.

Figure 6. Non-Inverting Amplifier in $\Phi_1$ Phase




The charge needed to pull the input back to ground during the transfer phase Φ2 moves in the opposite direction to that of the first example shown in Figure 4. Charge moving to $V_{out}$ is likewise in the opposite direction as shown in Figure 7.

Figure 7. Non-Inverting Amplifier in $\Phi_2$ Phase

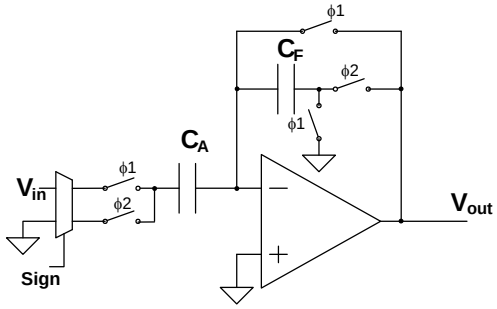



Thus, the output voltage is proportional to the input rather than inversely proportional. The result is a positive gain amplifier with a gain defined in Equation 8.

$$Gain = \frac{V_{out}}{V_{in}} = \frac{C_A}{C_F} \qquad \text{Equation 8}$$

Figure 8 shows the modification that allows the correct phasing for both positive and negative gain operation. A multiplexer controls the input switching phase through a "Sign" select signal.

Figure 8. Switched Cap Selectable Polarity Amplifier

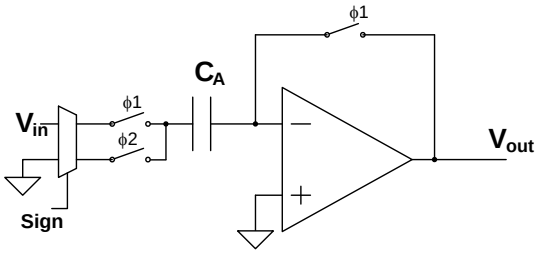



For the rest of these examples the "Sign" is assumed to be positive, that is, the $C_A$ acquires $V_{in}$ during $\Phi_1$ and moves back to zero during $\Phi_2$.

## Comparator

Building a comparator using SC block is relatively easy. Figure 9 shows a modification where the switch in series with the feedback capacitor is removed.

Figure 9. Switched Capacitor Comparator




This change removes the capacitor from the feedback loop, effectively setting the capacitor value to zero. Equation 8 states that the amplifier's gain is the ratio of the two capacitors. If the feedback capacitor is removed then the gain is infinite and the amplifier acts like a comparator.

See Figure 10 and Figure 11 for current path, capacitor and output voltage during Φ1 and Φ2 phase.

Figure 10. Comparator in $\Phi_1$ Phase

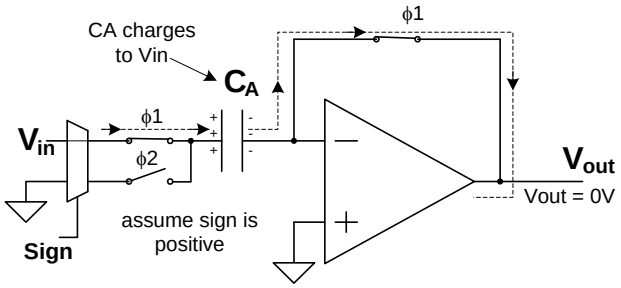
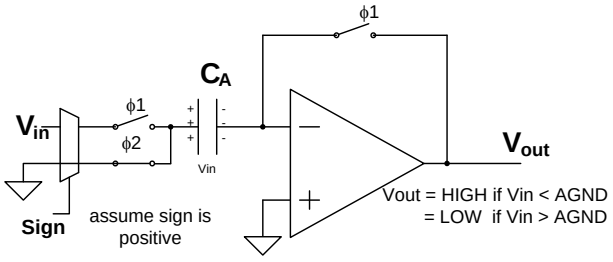


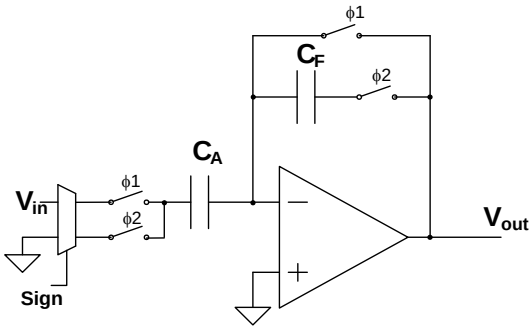

Figure 11. Comparator in $\Phi_2$ Phase




## Integrator

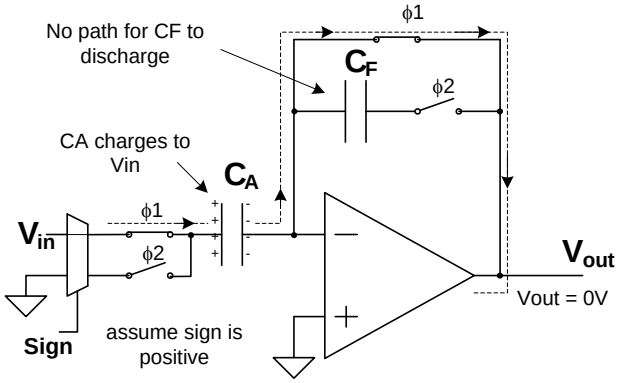
Integrators and differentiators can also be constructed using SC blocks. Figure 12 shows that removing the switch from $C_F$ to ground, prevents the charge on the feedback capacitor from being removed during the acquisition phase while still allowing the transfer of the input charge.

Figure 12. Switched Capacitor Integrator



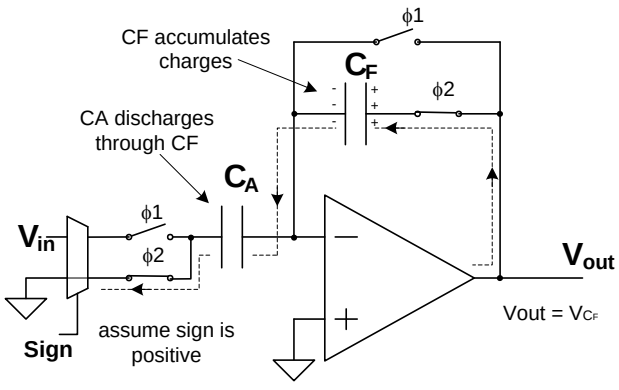

See Figure 13 and Figure 14 for integrator circuit in action.

Figure 13. Integrator in $\Phi_1$ Phase




During $\Phi_1$ phase, input capacitor $C_A$ charges to input voltage, whereas, feedback capacitor $C_F$ holds on to its charge.

Figure 14. Integrator in $\Phi_2$ Phase




During $\Phi_2$ phase, input capacitor $C_A$ discharges through $C_F$, thus transferring all its charge to $C_F$.

Equation 9 defines its operation.

$$V_{out} = V_{out}\, z^{-1} + Vin \frac{C_A}{C_F} \qquad \text{Equation 9}$$

Manipulating Equation 9 results in the transfer function shown in Equation 10.

$$Gain = \frac{V_{out}}{V_{in}} = \frac{C_A}{C_F} \frac{1}{(1 - z^{-1})} \cong \frac{1}{s}\left( f_s \frac{C_A}{C_F} \right) \qquad \text{Equation 10}$$

Equation 9 and Equation 10 state that this circuit is an adjustable integrator whose gain can be varied by changing the capacitor ratios or adjusting the sampling frequency.

## Differentiator

A differentiator may be created using a switched cap block. Figure 15 shows that the analog input is permanently connected to the input capacitor. This topology makes the feedback capacitor behave like a resistor and the input capacitor behave like a series capacitor.

Figure 15. Switched Capacitor Differentiator

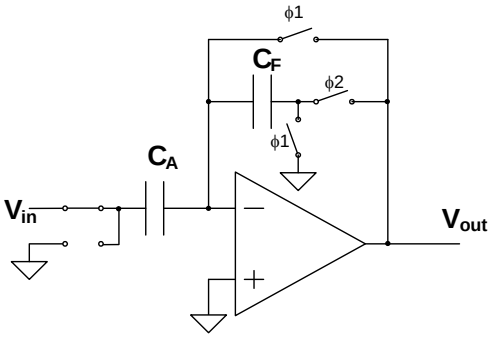
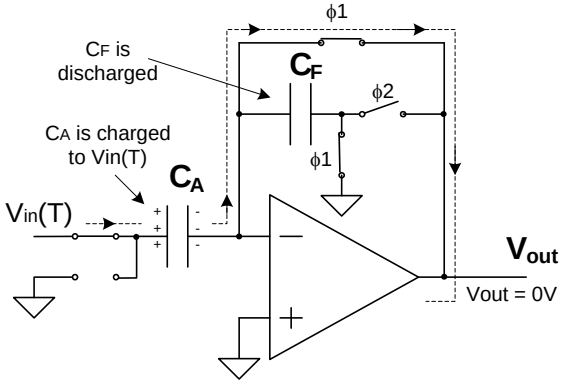


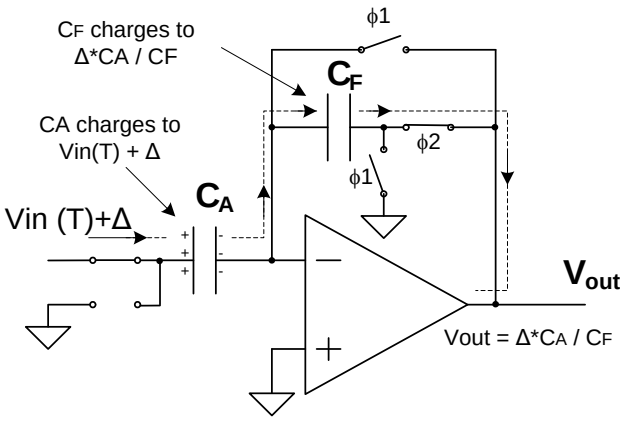

Figure 16 and Figure 17 shows the Differentiator operation in Φ1 and Φ2.

Figure 16. Differentiator in $\Phi_1$ Phase




During $\Phi_1$ phase, input capacitor acquires input voltage present at that particular instant, in this case, $V_{in}(T)$. The feedback capacitor $C_F$ is discharged.

Figure 17. Differentiator in $\Phi_2$ Phase




During $\Phi_2$, let us assume that the input voltage changes by Δ. This results in an increase in charge on the input capacitor $C_A$ by Δ * $C_A$. The same amount of charge is transferred to $C_F$ as the current path is same. This gives voltage across the feedback capacitor as $\Delta^*C_A/C_F$. Thus the output voltage is proportional to the change in an input voltage over time.

The differentiator operation can be mathematically modeled as given in equation 11.

$$\left(V_{in} - V_{in} z^{-1}\right) \cdot C_A = -V_{out} C_F \qquad \text{Equation 11}$$

Manipulating Equation 11 results in the transfer function shown in Equation 12.

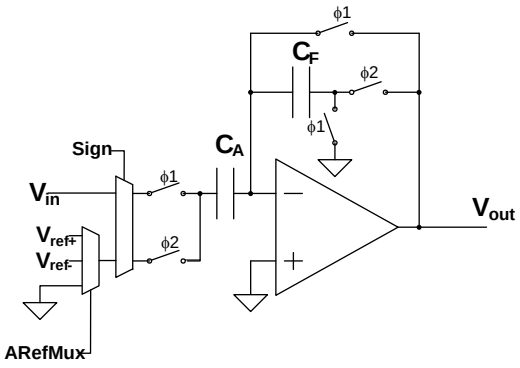
$$Gain = \frac{V_{out}}{V_{in}} = -\left(1 - z^{-1}\right) \frac{C_A}{C_F} \cong -s\left( \frac{1}{f_s} \frac{C_A}{C_F} \right) \qquad \text{Equation 12}$$

Equation 12 shows that this is an adjustable gain differentiator.

## Additional Switched Cap References

So far, all the examples have the input voltage referenced to analog ground. Analog ground may be a convenient reference point but others are also possible. Figure 18 shows a standard circuit with an improved reference selection.

Figure 18. Improved Switched Cap Reference Selection




**ARefMux** allows the selection of two other references besides analog ground. Equation 13 defines the output voltage for a switched cap amplifier given different reference configurations. The equations are for the cases where the reference is analog ground, $V_{ref+}$ or $V_{ref-}$.

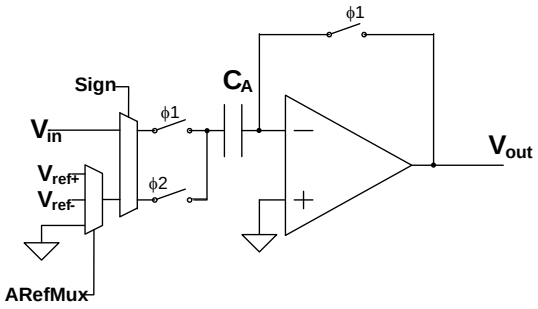
$$V_{out} = \frac{C_A}{C_F} V_{in}$$
$$V_{out} = \frac{C_A}{C_F}(V_{in} - V_{ref+})$$
$$V_{out} = \frac{C_A}{C_F}(V_{in} - V_{ref-})$$

Equation 13

## Comparator as 2-bit ADC

Combining the comparator in Figure 9 with the reference selection in Figure 18, results in a comparator with multiple compare points, as shown in Figure 19. This kind of comparator can be used as a simple 2 bit ADC.

Figure 19. Poor Man's 2-bit Switched Cap ADC




With proper control of ARefMux, it is possible to determine if $V_{in}$ is:

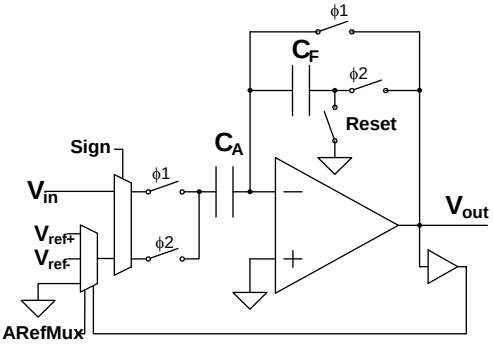
- Greater than $V_{ref+}$
- Less than $V_{ref+}$ but greater than ground
- Less the ground but greater than $V_{ref-}$
- Less than $V_{ref-}$

These four states make this circuit a 2-bit analog-to-digital converter (ADC).

## Real Analog-to-Digital Conversion

Slight modification of the reference selection allows this circuit to function as an analog to digital modulator. This modification allows the output of the switched cap block to control the reference selection, creating feedback and creating a digital signal that can be measured to determine the size of the analog input. Figure 20 shows that a comparator is added to the output and is connected to the reference selection mux.

Figure 20. Analog to Digital Modulator




Selecting the proper ARefMux value allows the output of the comparator to determine the reference voltage. The relationship is:

- The reference is set to $V_{ref+}$ when the comparator is high (positive output value).
- The reference is set to $V_{ref-}$ when comparator is low (negative output value).

The switches around the feedback capacitor are configured to make an integrator. The comparator control causes a reference, with the same polarity as the $V_{out}$, to be subtracted from the input. This negative feedback causes $V_{out}$ to move back towards zero.

Equation 14 describes $V_{out}$, given the following conditions:

- The initial condition of $V_{out}$ is zero.
- The switch cycle is preformed "n" times.
- $V_{out}$ is greater than zero (comparator is high) "a" of those times.

$$V_{out} = \frac{C_A}{C_F} n V_{in} - \frac{C_A}{C_F} a V_{ref+} - \frac{C_A}{C_F}(n-a) V_{ref-}$$

Equation 14

Given that the references are of equal but opposite polarity, solving for $V_{in}$ results in the following equation.

$$V_{in} = V_{ref}\frac{(2a-n)}{n} + \frac{1}{n}V_{out}\frac{C_F}{C_A} \quad ;\left(V_{ref} = V_{ref+} = -V_{ref-}\right)$$ Equation 15

$V_{in}$ is a function of $V_{ref}$ and $V_{out}$. As stated earlier, the negative feedback causes $V_{out}$ to move back towards ground every cycle. This makes $V_{out}$ less than $(C_A/C_F)*V_{ref}$. As "n" becomes larger, the contribution of $V_{out}$ to Equation 15 becomes negligible. This allows a simpler Equation 16.

$$V_{in} = V_{ref}\left(\frac{2a}{n} - 1\right) \quad ;\left(\frac{1}{n}V_{out}\frac{C_F}{C_A} < \frac{1}{n}V_{ref} \approx 0\right)$$ Equation 16

$V_{in}$ is not dependent on the ratio of the two capacitors. It is only the ratio of "a" and "n", and a function of $V_{ref}$. Measuring $V_{in}$ is just a function of counting the number of times the comparator is high ("a") during a sequence of "n" switch cycles. The range is $-V_{ref}$ (a = 0) to $+V_{ref}$ (a=n), and the resolution is $2V_{ref}/n$. Longer the period (larger "n") the better the resolution of voltage measurement.

## Switched Capacitor PSoC Blocks

The architecture previously discussed is quite versatile. It allows many different functions merely by altering the circuit's switch closures. This architecture is used as the basis for the SC blocks in the PSoC microcontroller and is implemented with Type C and Type D switched capacitor blocks.

### Type C Switched Capacitor Blocks

Figure 21 shows the Type C switched capacitor block. A larger copy of this diagram along with a map of the Control registers for the block is in Appendix A. The canonical version of Figure 21 may be found in the PSoC 1 Technical Reference Manual under Analog System > Switched Capacitor PSoC Block section.

Figure 21. Type C Switched Capacitor Block Architecture

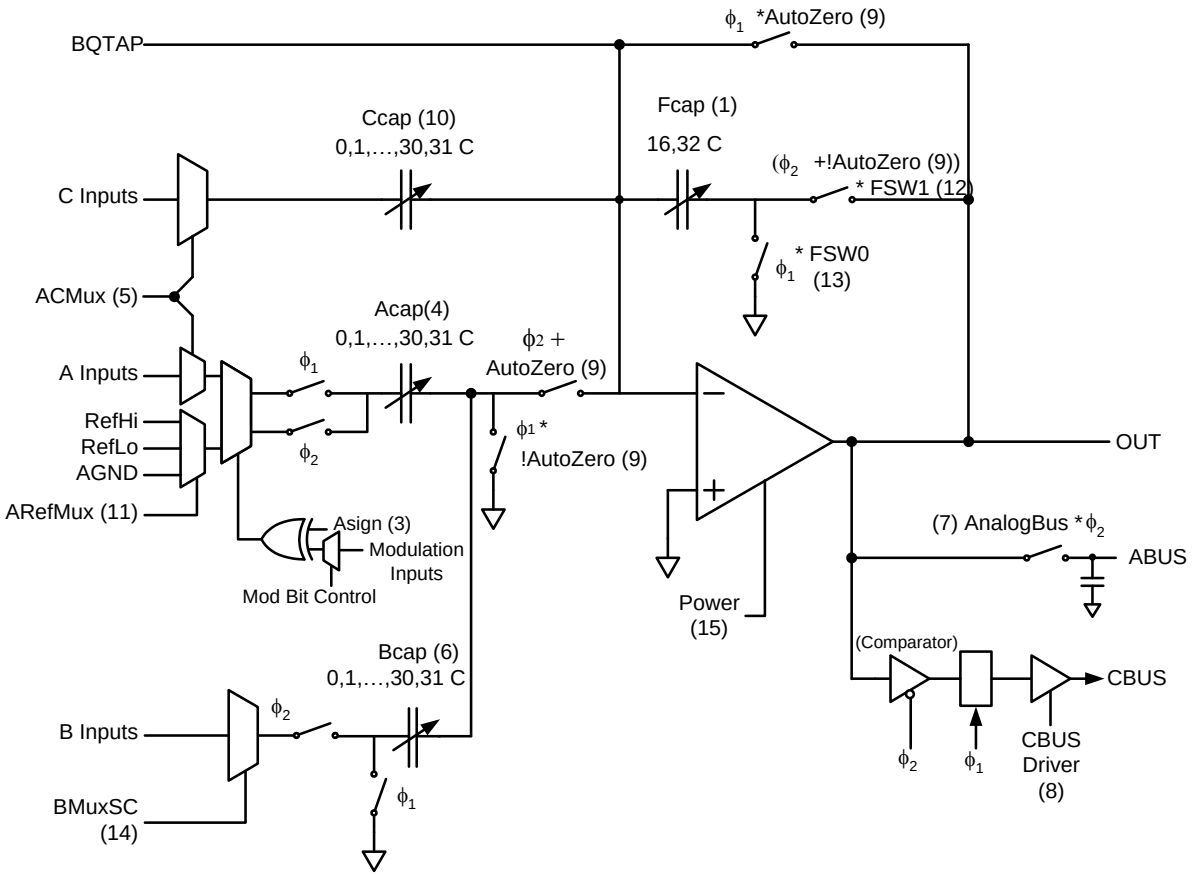



Figure 21 is similar to the architecture shown in Figure 18, with the following additions:

- A programmable **CCap** capacitor connects to the summing node of the opamp inverting input.
- A programmable **BCap** switched capacitor connects to the summing node of the opamp inverting input.
- An **AnalogBus** switch connects the opamp's output to an analog buffer.
- A **CompBus** switch connects the comparator to the digital blocks.

The BCap acts similar to the ACap except that it only samples its input on $\Phi_2$ and is always referenced to ground. It is generally used for multiple input amplifiers. The CCap primarily benefits filter design.

## Type C Switched Cap Block Parameters

PSoC 1's switched cap blocks are most easily configured using the user module interface in the PSoC Designer IDE. There are 15 different parameters for a type C switched cap block user module.

The parameters with descriptions of their operations are given as follows:

1. **FCap**
   A 1-bit field to set the value of FCap to either 16 or 32 units. Each unit of capacitance is approximately 50 fF.
2. **ClockPhase**
   A 1-bit field that, when set, swaps the $\Phi_1$ and $\Phi_2$ phases. It is primarily used to match the input signal sampling when input is taken from another SC block. This is important as the output of a switched capacitor is valid only during $\Phi_2$ phase and not on $\Phi_1$ phase, the acquisition phase.
3. **ASign**
   A 1-bit field to set the gain of the block to either positive or negative.
4. **ACap**
   A 5-bit field to set the value of ACap from 0 to 31 capacitance units.
5. **ACMux**
   A 3-bit field to select the inputs to the ACap and the CCap. Appendix C and Appendix D show the connection options.
6. **BCap**
   A 5-bit field to set the value of BCap from 0 to 31 capacitance units.
7. **AnalogBus**
   A 1-bit field that, when set, connects the output to an analog buffer. This buffer can be used to drive pins or other analog resources in the part.
8. **CompBus**
   A 1-bit field that, when set, connects the comparator output to the data inputs of PSoC 1's digital blocks.
9. **AutoZero**
   A 1-bit field that, when set, forces an autozero during the $\Phi_1$ signal acquisition phase.
10. **CCap**
    A 5-bit field to set the value of CCap from 0 to 31 capacitance units.
11. **ARefMux**
    A 2-bit field to select the voltage potential that the A input is referenced to. It can be AGND, $V_{ref+}$, $V_{ref-}$, or a voltage reference determined by the state of the output comparator.
12. **FSW1**
    A 1-bit field to select if FCap is connected. If set to zero, FCap is not connected, and the block functions as a comparator. If set to one, the FCap is in the feedback path, and the circuit functions as a gain stage or integrator.
13. **FSW0**
    A 1-bit field to select if FCap is discharged during $\Phi_1$. If set to one, the FCap is discharged and the circuit functions as a gain stage. If set to zero, the capacitor is not discharged and the circuit functions as an integrator.
14. **BMux(SCA)**
    A 2-bit field to set the inputs to the BCap. Appendix E shows the connection options.
15. **Power**
    A 2-bit field to set the power for the block. The options are: off, low, medium, and high.

## Type D Switched Capacitor Blocks

PSoC 1 also contains Type D switched capacitor blocks, which allow for the construction of more complex analog circuits. Figure 22 shows the type D switched capacitor block. A map of the Control resistors for Type D SC-block is given in Appendix BAppendix B. The canonical version of Figure 22 may be found in the PSoC 1 Technical Reference Manual under Analog System > Switched Capacitor PSoC Block.

Figure 22. Type D Switched Capacitor Block Architecture

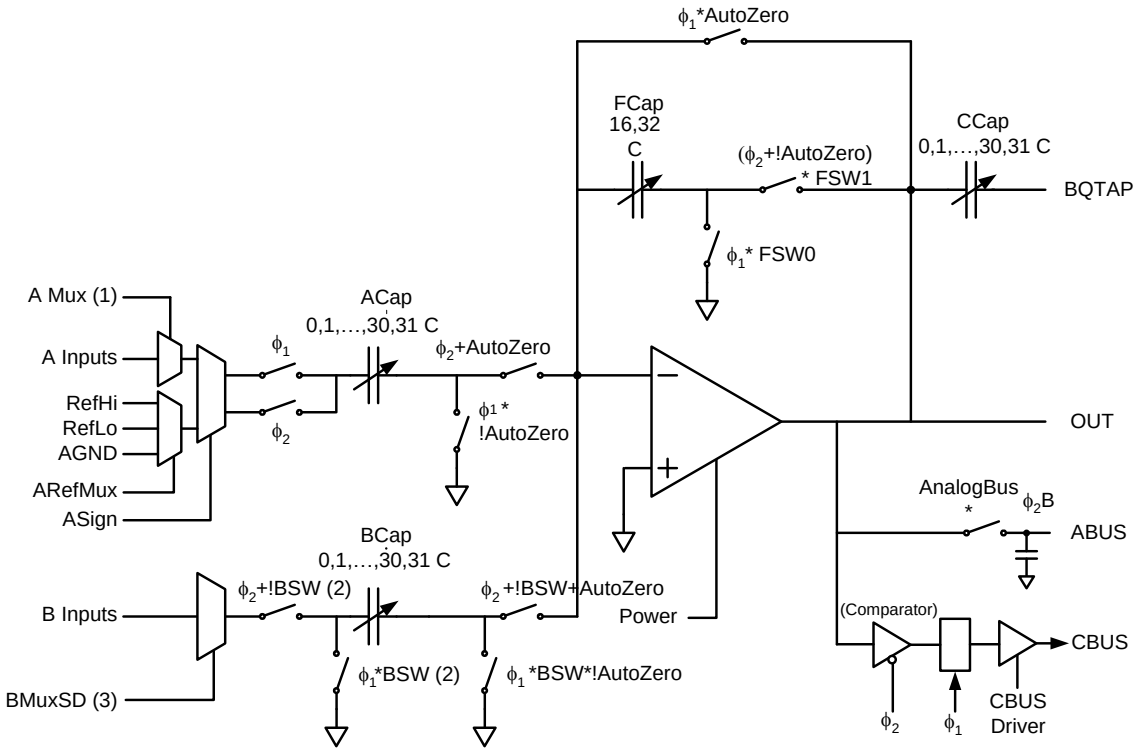



Figure 22 is similar to the Type C SC block shown in Figure 21 with the following differences:

- There is no multiplexed input to **CCap** but a connection to the output of the block. The other side of **CCap** connects to the summing node of the type C SC block next to it. It is used to build biquad filters.
- The control field BSW allows **BCap** to **f**unction as a switched capacitor or as just a capacitor.

### Type D Switched Cap Block Parameters

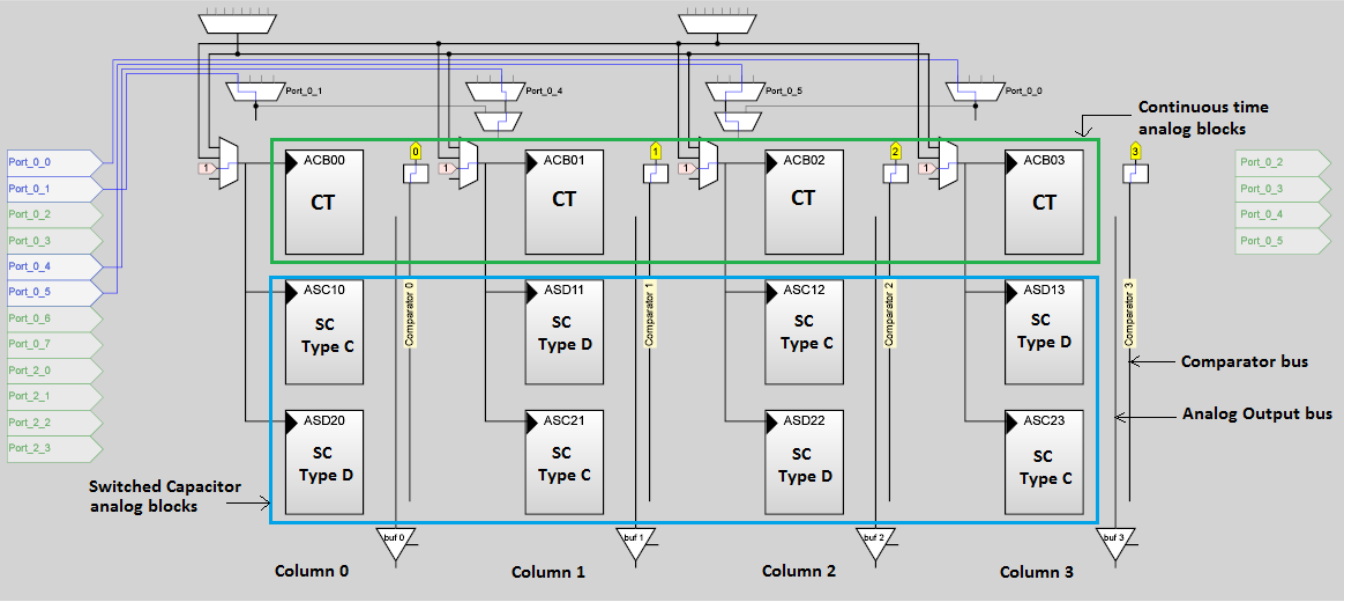
There are 16 different parameters for a Type D switched cap block. Thirteen are common with the Type C **SC** block and have already been discussed. The remaining three parameters with descriptions of their operations follow:

- **AMux**
  A 3-bit field to set the inputs to the ACap. Appendix C shows the connection options.
- **BSW**
  A 1-bit field. When set, BCap functions as a switched capacitor input. If not set, then BCap functions as a series capacitor.
- **BMux(SD)**
  A 1-bit field to set the inputs to the BCap. Appendix E shows the connection options.

## SC Blocks and PSoC 1 Architecture

Figure 23 shows the array of analog blocks for the CY8C27x43 family of parts.

Figure 23. PSoC 1 Analog Block Array




There are four columns of analog blocks, with each column having its own analog bus, comparator bus, and clock to generate the $\Phi_1$ and $\Phi_2$ clocks.

Each column contains one type “C” SC block and one type “D” SC block for a total of eight SCBlocks. The order of the C and D blocks is reversed in each column, so that each type C block is surrounded by type D blocks, and vice versa.

Different User Modules use different numbers of blocks. For example:

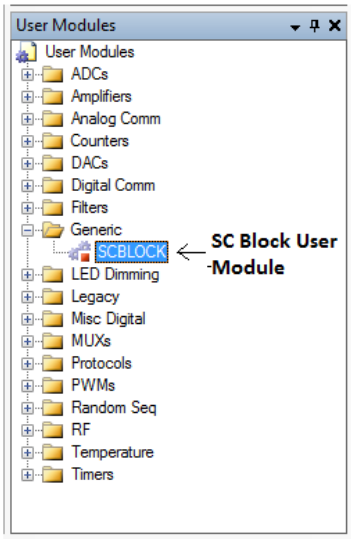
- The **DAC6** User Module uses one SC block.
- The **DAC8** User Module uses two SC blocks.
- The **DELSIG8**, **DELSIG11**, and **ADCINC12** ADC user modules each use only one SC block.
- The **LPF2** User Module uses two SC blocks.
- The **PWM8** is a digital only User Module and uses no SC blocks.

The PSoC 1 switched capacitor blocks are so versatile that one of the best ways to utilize them is to configure all settings of the block manually. To assist the user, a fully parameterized SC block User Module has been developed.

## PSoC 1 SCBlock User Module

The SCBlock User Module is found under the “generic” category of User Modules in PSoC Designer IDE.

Figure 24 SCBlock User Module in Catalog




This block may be placed in any of the eight available SC blocks.

## Additional Applications

Switched cap blocks can be used in many applications besides those described previously. Some additional examples are described in the following sections. The project containing all three examples shown is distributed along with this application note. Besides these examples, Appendix G: SC-Block Applications Cook Book gives settings for variety of applications using SC Block.

PSoC Designer Tool is used to create the projects for PSoC 1. If you are new to PSoC 1 Designer, it is recommended to go through online training material.

**Example 1: Differential Amplifier with Common Mode Output**

A common mode output signal is useful to many signal processing applications. It is also highly useful where the common mode feedback is used to drive a shield or signal guard. Figure 25 shows the architecture for a differential amplifier with a common mode output. The PSoC implementation is shown in Figure 26:

Figure 25. Differential Amplifier with Common Mode Output

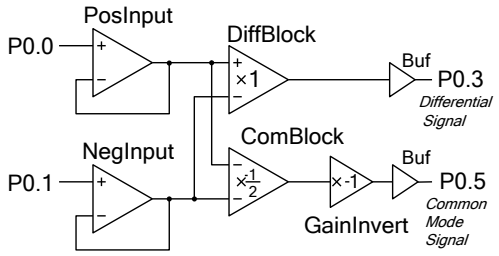
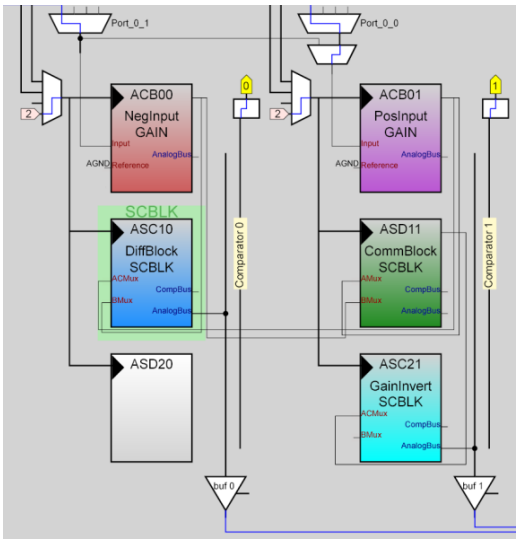



Figure 26. PSoC Block Placement of Differential Amplifier with Common Mode Output




The two input buffers are programmable gain amplifier (PGA) User Modules with matched gains. The three switched cap blocks are populated with generic SC Block user modules.

The difference output is defined by Equation 17.

$$V_{difference} = PosInput - NegInput \qquad \text{Equation 17}$$

The amplifier is an A-B amplifier with a gain of one. Its parameters are shown in Figure 27.

Figure 27. Parameters for DiffBlock SCBLOCK

DiffBlock

| User Module Parameters | Value |
|---|---|
| FCap | 16 |
| ClockPhase | Norm |
| ASign | Pos |
| ACap | 16 |
| ACMux | ACB01 |
| BCap | 16 |
| AnalogBus | AnalogOutBus_0 |
| CompBus | Disable |
| AutoZero | On |
| CCap | 0 |
| ARefMux | AGND |
| FSW1 | On |
| FSW0 | On |
| BMux | ACB00 |
| Power | High |

For a difference amplifier with a gain of one, the values of **FCap**, **ACap**, and **BCap** must be the same. **CCap** is not used so its value is set to zero. The continuous time blocks source both input signals, and thus **ClockPhase** can remain set to “Norm.” The **ACMux** is set to connect its input to “ACB01.” **ARefMux** is set to “AGND” so both input references have the same potential. **BMux** is set to connect its input into “ACB00.” **ASign** is set to “Pos”. To be an amplifier, **FSW1**, **FSW0**, and **AutoZero** must be set “On.” The comparator is not used so **CompBus** is set to “Disable.” **AnalogBus** is set to “AnalogOutBus0” so that the output can be brought to the analog buffer on P0[3]. **Power** is set “High.”

The common mode output is defined by the Equation 18.

$$V_{common} = \frac{PosInput + NegInput}{2} \qquad \text{Equation 18}$$

A stage that can implement an A+B amplifier is required. Unfortunately, the architecture limits the B input to negative gains. The solution is to build a -A-B amplifier and follow it with a gain stage of -1.

The parameters for a -A-B amplifier with a gain of one half are shown in Figure 28 :

Figure 28. Parameters for the ComBlock SCBLOCK

ComBlock

| User Module Parameters | Value |
|---|---|
| FCap | 32 |
| ClockPhase | Norm |
| ASign | Neg |
| ACap | 16 |
| AMux | ACB01 |
| BCap | 16 |
| AnalogBus | Disable |
| CompBus | Disable |
| AutoZero | On |
| CCap | 0 |
| ARefMux | AGND |
| FSW1 | On |
| FSW0 | On |
| BSW | On |
| BMux | ACB00 |
| Power | High |

For a gain of one half on both inputs, **FCap** is set to '32' and both **ACap** and **BCap** are set to '16'. **CCap** is not used so its value is set to zero. The continuous time blocks source both input signals, and thus **ClockPhase** can remain set to "Norm." The **AMux** is set to connect its input to "ACB01." **ARefMux** is set to "AGND" so both inputs references have the same potential. **BMux** is set to connect its input into "ACB00." **BCap** is required to be a switched capacitor so **BSW** is set "On." **ASign** is set to "Neg." To be an amplifier, **FSW1**, **FSW0**, and **AutoZero** must be set "On." The comparator is not used so **CompBus** is set to "Disable." **AnalogBus** is also not used so it is set to "Disable." **Power** is set to "High."

This block is to be followed by a gain inversion stage. The parameters for a -1 gain stage are shown in Figure 29.

Figure 29. Parameters for the GainInvert SCBLOCK

GainInvert

| User Module Parameters | Value |
|---|---|
| FCap | 16 |
| ClockPhase | Norm |
| ASign | Neg |
| ACap | 16 |
| ACMux | ASD11 |
| BCap | 0 |
| AnalogBus | AnalogOutBus_1 |
| CompBus | Disable |
| AutoZero | On |
| CCap | 0 |
| ARefMux | AGND |
| FSW1 | On |
| FSW0 | On |
| BMux | ? |
| Power | High |

For a gain of -1, the values of **Fcap** and **ACap** must be the same. **BCap** and **CCap** are not used so their values are set to zero. **ASign** is set to "Neg." Its input is sampled on the same phase as a valid Com Block output signal so **ClockPhase** can remain set to "Norm." The **ACMux** is set to connect its input to "ASD11." **ARefMux** is set to "AGND." **BMux** is not needed so it is not set. Again **FSW1**, **FSW0**, and **AutoZero** must be set to "On." The comparator is not used so **CompBus** is set to "Disable." **AnalogBus** is set to "AnalogOutBus1" so that the output can be brought to the analog buffer on P0[5]. **Power** for this example is set to "High." The actual setting for other applications is determined by signal bandwidth.

These five blocks implement the circuit shown in Figure 25. The column **clocks** are set to **1 MHz**. This sets the sample rate to 250 Ksps. It is recommended that when used as amplifiers, the SC Blocks should not be sampled faster than 350 Ksps.

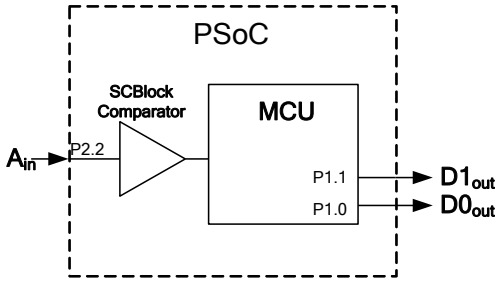
**Example Code:** Example 1 only requires the PGA user modules to be started. The code in C language follows.

```
//-------------------------------------------
-// C main line
//-------------------------------------------
-
#include <m8c.h>          // part specific
constants and macros
#include  "PSoCAPI.h"        //  PSoC  API
definitions for all User Modules

void main(void)
{
    NegInput_Start(NegInput_HIGHPOWER);
    PosInput_Start(PosInput_HIGHPOWER);
    //No code necessary to start SC Blocks
    while(1);
}
```

### Example 2: A 2-Bit ADC

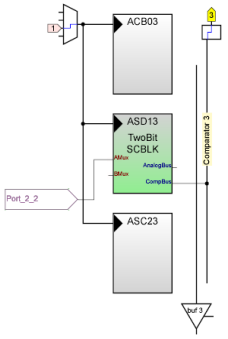
In Figure 19, a four state ADC was shown using a SCBlock as a comparator and using the reference mux to test different ranges. Figure 30 shows the block level representation.

Figure 30. Two Bit ADC Example




The PSoC 1 implementation is shown in Figure 31. Note that the PSoC 1 SC block is capable of implementing a 6-bit SAR ADC using single SC block. It is available in the form of a user module in PSoC Designer.

Figure 31. PSoC 1 SC Block Placement of TwoBit ADC




The input is brought in from P2[2] to an SCBlock (Instance name: "**TwoBit**"). It is configured as a comparator. Software manipulates the **ARefMux** field in Control register **TwoBit_cr3** to select the reference as Agnd, $V_{ref+}$, or $V_{ref-}$.

**Bit 7** of the Analog Comparator Control Register (**CMP_CR**) allows the software to determine the state of the column 3 comparator. This allows the software to determine if the input is:

- Greater than $V_{ref+}$
- Less than $V_{ref+}$ but greater than analog ground
- Less than analog ground but greater than $V_{ref-}$
- Less than $V_{ref-}$

The parameters for a comparator with a configurable reference are shown in Figure 32:

Figure 32. Parameters for the TwoBit SCBLOCK

TwoBit

| User Module Parameters | Value |
|---|---|
| FCap | 16 |
| ClockPhase | Norm |
| ASign | Pos |
| ACap | 31 |
| AMux | Port_2_2 |
| BCap | 0 |
| AnalogBus | Disable |
| CompBus | ComparatorBus_3 |
| AutoZero | On |
| CCap | 0 |
| ARefMux | AGND |
| FSW1 | Off |
| FSW0 | Off |
| BSW | Off |
| BMux | ? |
| Power | High |

For a comparator, the **FCap** is not connected so its value is not important. **ACap** must be a non-zero value. **BCap** and **CCap** are not used so their values are set to zero. The input is from a continuous input signal so there is no phase sampling problem and **ClockPhase** can remain set to "Norm." The **AMux** is set to connect its input to "Port_2_2." **ARefMux** must be controlled by software but is set to a default value of "AGND." **BMux** is not needed so it is not set. **ASign** is set to "Pos." To be a comparator, **FSW1** and **FSW0** must be set to "Off," but **AutoZero** must be set "On." This disconnects the feedback capacitor. Setting **CompBus** to "ComparatorBus_3" allows the CPU access to the state of the comparator. **AnalogBus** is set to "Disable." **BSW** is not used and is set to "Off." **Power** is set "High." The column **clock** is set to **8 MHz**. This sets the sample rate to 2 Msps. It is recommended that when used as a comparator, the SC Blocks should not be sampled faster than 2 Msps.

**Example Code:** In Example 2, the ARefMux reference is controlled using software. This requires substantial code in the main loop, shown in Appendix F.

**Example 3: Isolated Analog Driver**

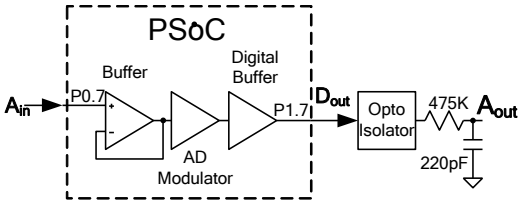
It is sometimes necessary to get an analog signal across an isolated barrier. For a higher frequency signal with no DC component, this is easily done with capacitor or transformer coupling. For lower frequencies, the transformers and capacitors become increasing larger. The expense and size of these components for lower frequency and DC coupled signals makes this solution prohibitively expensive.

A cheaper solution requires using a SC Block as an analog-to-digital (AD) modulator. Figure 20 shows the architecture for an AD modulator that converts an input signal to a series of pulses where:

- A one represents $V_{ref+}$
- A zero represents $V_{ref-}$
- The average is equal to the input signal

Figure 33 shows how it is assembled to pass the signal across an isolation barrier.

Figure 33. PSoC 1 Isolated Analog Driver




The input signal ($A_{in}$) is buffered and passed to the AD modulator where the signal is converted to a series of digital pulses. These pulses are brought out of the chip through the digital buffer. The pulses ($D_{out}$) pass through an opto-isolator. Now isolated, these pulses are averaged to reconstruct an analog signal ($A_{out}$).

The low-pass filter is set to 1.5 kHz to knock out the harmonics generated by the pulses.

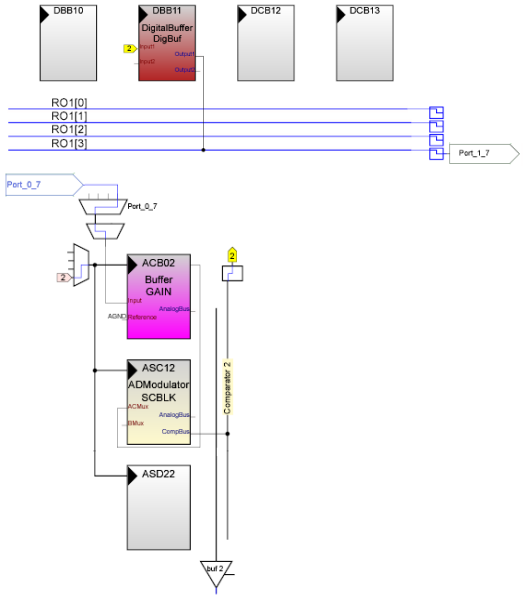
The PSoC 1 implementation is shown in Figure 34.

**Example Code:** Example 3 does not require any main code, but does require a start call to start the PGA. The switched capacitor blocks do not require any calls to start.

The C code follows.

```
void main(void)
{
    //Start user modules
    DigBuf_Start();
    PGA_Start(PGA_HIGHPOWER);

    //SC block starts itself

    while(1);//Execution     requires     no
    further firmware interaction
}
```

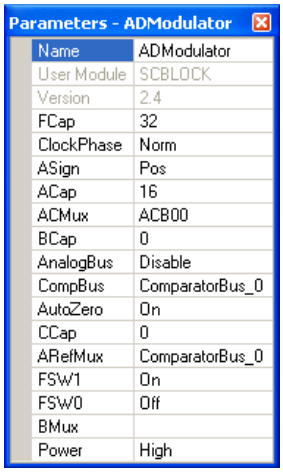
Figure 34. PSoC 1 Analog Isolator Driver Block Placement




The input buffer is a PGA User Module. Its parameter selection is left as an exercise for the reader.

The ADModulator is an integrator with a comparator controlled input reference. Its parameters are shown in Figure 35.

Figure 35. Parameters for ADModulator SCBLOCK




In theory, the ratio of **ACap/FCap** is unimportant. Practical considerations of loop gain and comparator offset dictate that **FCap** must be set to '32' while **ACap** is set to '16'. **BCap** and **CCap** are not used so their values are set to zero. The continuous time blocks source the input signal, and thus **ClockPhase** can remain set to "Norm." The **ACMux** is set to connect its input to "ACB00." **ARefMux** is set to "ComparatorBus_0", allowing the output comparator to control the reference selection. **BMux** is not required so it need not be set. **ASign** must be set to "Pos." To be an integrator, **FSW1** and **AutoZero** must be set "On" while **FSW0** must be set "Off." The comparator needs to connect to the digital blocks so **CompBus** is set to "ComparatorBus_0". **AnalogBus** is set to "Disable." **Power** is set "High."

The DigitalBuffer is a User Module that allows the comparator bus to be output on P1[7]. This output is connected to an external opto-isolator followed by an RC filter.

## Summary

Switched capacitor circuitry allows building of integrated circuitry with capacitors instead of expensive resistors. Changing a circuit's function can be as easy as changing the sequence in which its switches are closed. With eight SC Blocks offers good integration options. This makes PSoC 1 a true programmable system on a chip.

## Related Application Notes

- AN2223: PSoC® 1 Approximating an Opamp with a Switched Capacitor Integrator

  This application note explains how to use a switched capacitor block in integrator mode as a simple Opamp.

- AN2168: PSoC® 1 Understanding Switched Capacitor Filters

  This application note presents the theory behind switched capactor filters – Low pass, High pass, Bandpass and notch filters and provides guidelines and examples for implementing these filters in PSoC®1 devices.

- AN64475: PSoC® 1 Optimizing Cascaded Switched Capacitor filters

  AN64475 demonstrates how PSoC® 1 switched capacitor band pass filters (BPF2, BPF4) and elliptical low pass filters (ELPF2 and ELPF4) can be combined to provide excellent near out-of-band rejection for communications applications.

- AN2219: PSoC® 1 Selecting Analog Ground and Reference

  This application note explains PSoC®1 internal analog ground and reference voltage structure.

- AN32200: PSoC® Clocks and Global Resources

  This application note describes the clock resources of PSoC® 1.

- AN2108: PSoC® 1 Implementing Hysteresis Comparator

  This application note explains multiple implementations of a hysteresis comparator.

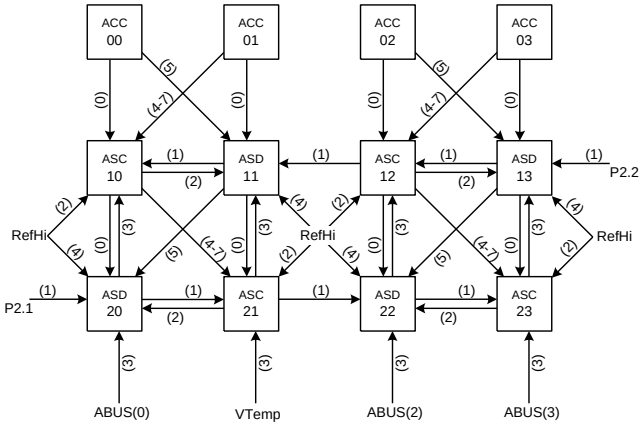
# Appendix A: Control Registers for a Type C Switched Capacitor Block

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| CR0 | **FCap**<br>16, 32 | **ClockPhase**<br>Norm, Swap | **ASign**<br>Pos, Neg | **ACap**<br>[0..31] | | | | |
| CR1 | **ACMux**<br>`C: North => A: North, E1W2, REFHI, South;`<br>`C: Diag  => A: Diag,  Diag, Diag,  Diag` | | | **BCap**<br>[0..31] | | | | |
| CR2 | **AnalogBus**<br>Disable, Enable | **CompBus**<br>Disable, Enable | **AutoZero**<br>Off, On | **CCap**<br>[0..31] | | | | |
| CR3 | **ARefMux**<br>AGND, REFHI, REFLO, CMP | | **FSW1**<br>Off, On | **FSW0**<br>Off, On | **BMuxSCC**<br>North, E1W2, E2W1, South | | **Power**<br>Off, Low, Med, High | |

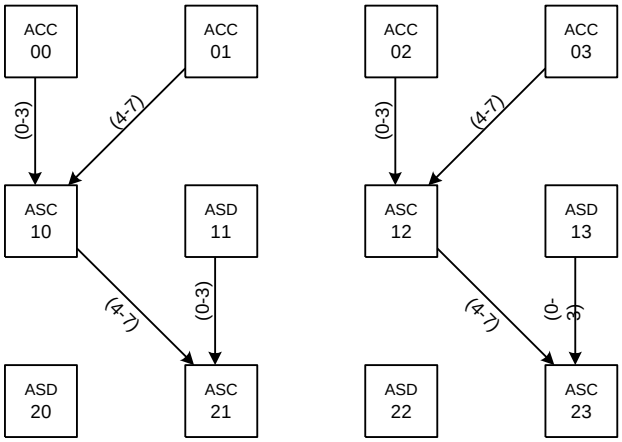
# Appendix B: Control Registers for a Type D Switched Capacitor Block

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| CR0 | **FCap**<br>16. 32 | **ClockPhase**<br>Norm, Swap | **ASign**<br>Pos, Neg | **ACap**<br>[0..31] | | | | |
| CR1 | **AMux**<br>North, E1W2, E2W1, South, REFHI, Diag, NC, Hold | | | **BCap**<br>[0..31] | | | | |
| CR2 | **AnalogBus**<br>Disable, Enable | **CompBus**<br>Disable, Enable | **AutoZero**<br>Off, On | **CCap**<br>[0..31] | | | | |
| CR3 | **ARefMux**<br>AGND, REFHI, REFLO, CMP | | **FSW1**<br>Off, On | **FSW0**<br>Off, On | **BSW**<br>Off, On | **BMuxSCD**<br>Diag, North | **Power**<br>Off, Low, Med, High | |

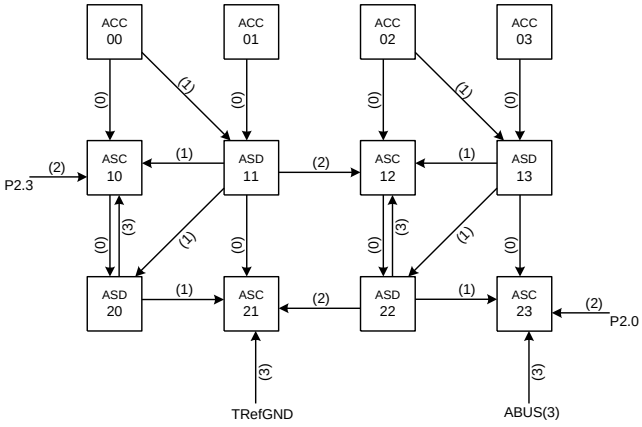
# Appendix C: A Input Multiplexer Connections



## Appendix D: C Input Multiplexer Connections




## Appendix E: B Input Multiplexer Connections



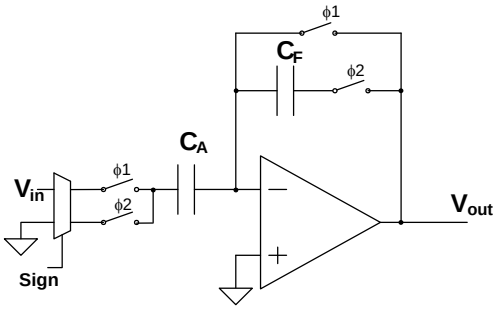
## Appendix F: C Code: 2-Bit ADC Example Project

```
//-------------------------------------------------------------------------
// C main line - This code runs in a loop where the input
// input is continuously sampled and compared with the
// selectable references to determine one of four different
// levels. Dout1 and Dout0 are set accordingly.
// Inline assembly "nop" no-ops are used to stabilize the
// comparator readings.
//-------------------------------------------------------------------------

#include <m8c.h>        // part specific constants and macros
#include "PSoCAPI.h"    // PSoC API definitions for all User Modules


void main()
{
    //TwoBit_SCBLOCKcr3 register bits 6 and 7 are the reference bits
    //00b Analog ground is selected.
    //01b RefHi input selected. (This is usually the high reference.)
    //10b RefLo input selected. (This is usually the low reference.)
    while(1){
        TwoBit_cr3 &= 0x3F;      //Initialize to analog ground reference
        //TEST Comparator Bus
        asm("nop");
        asm("nop");
        asm("nop");
        asm("nop");
        asm("nop");
        asm("nop");
        if(CMP_CR0 && 0x80){      //If it is greater then select RefHi reference
            //Reference set to RefHi
            TwoBit_cr3 &= 0x7F;
            TwoBit_cr3 |= 0x40;
            asm("nop");
            asm("nop");
            asm("nop");
            asm("nop");
            asm("nop");
            asm("nop");
            if(CMP_CR0 && 0x80){  //Value is above RefHi D = 11
                PRT1DR |= 0x03;
            }
            else{                 //Value is between AGND and RefHI D = 10
                PRT1DR &= 0xFE;
                PRT1DR |= 0x02;
            }
        }
        else{                     //Else select RefLo reference
            //Reference set to RefLo
            TwoBit_cr3 &= 0xBF;
            TwoBit_cr3 |= 0x80;
            asm("nop");
            asm("nop");
            asm("nop");
            asm("nop");
            asm("nop");
            asm("nop");
            if(CMP_CR0 && 0x80){  //Value is between AGND and RefLo D = 01
                PRT1DR &= 0xFD;
```

```
                PRT1DR |= 0x01;
            }
            else{                   //Value is below RefLo D = 00
                PRT1DR &= 0xFC;
            }
        }
    }
}
```

# Appendix G: SC-Block Applications Cook Book

### Integrator



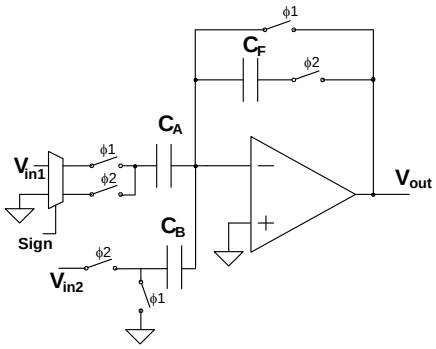

$$Gain = \frac{V_{out}}{V_{in}} = \frac{C_A}{C_F}\frac{1}{(1-z^{-1})} \cong \frac{1}{s}\left(f_s \frac{C_A}{C_F}\right)$$

Both Type C and Type D SC block can be used to build an integrator.

| SCBlock | | | |
|---|---|---|---|
| **Parameter** | **Type C / D** | **Value** | **Comments** |
| FCap | Both | 16 / 32 | Select FCap based on integrator time constant requirement |
| ClockPhase | Both | Norm | Options – Norm, Swap |
| ASign | Both | Pos | Options:<br>Pos – Non-inverting configuration<br>Neg – Inverting configuration |
| ACap | Both | 1 – 31 | Select ACap ($C_A$) value based on required Integrator time constant |
| ACMux | Type C only | source | Select the source for integrator input signal (input $V_{in}$) |
| BCap | Both | 0 | Disconnect 'B' input |
| AnalogBus | Both | AnalogOutBus_0 | SC block output is routed to Analog output bus (which is then routed to pin) |
| CompBus | Both | Disable | Not used |
| Autozero | Both | On | Autozero (input offset voltage correction) enabled |
| CCap | Type C only | 0 | Not used |
| ARefMux | Both | AGND | SC block reference is analog ground. The integrator output ramps up or down depending on whether input voltage is greater than or less than AGND. |
| FSW1 | Both | On | FSW1 is enabled |
| FSW0 | Both | Off | FSW0 is disabled |
| BMux | Both | x | Not used |
| Power | Both | High | SC block is operated in high power mode |
| AMux | Type D only | Source | Select the source for integrator input signal (input $V_{in}$) |
| BSW (SD) | Type D only | x | Not used |

### Integrator: Dual input

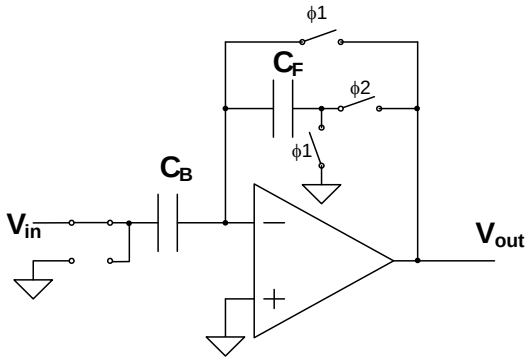
This is slight variant of the application given above. This architecture uses two inputs $V_{in1}$ and $V_{in2}$. In this implementation, outputs ramps high or low depending on the difference between two input voltages. This can be implemented in both Type C and D blocks.




$$V_{out} = \frac{f_s}{s} \times \left(\frac{C_A}{C_F} V_{in1} - \frac{C_B}{C_F} V_{in2}\right)$$

| SCBlock | | | |
|---|---|---|---|
| **Parameter** | **Type C / D** | **Value** | **Comments** |
| FCap | Both | 16 / 32 | Select FCap based on integrator time constant requirement |
| ClockPhase | Both | Norm | Options – Norm, Swap |
| ASign | Both | Pos | Options:<br>Pos – Non-inverting configuration<br>Neg – Inverting configuration |
| ACap | Both | 1 – 31 | Select ACap ($C_A$) value based on required Integrator time constant |
| ACMux | Type C only | Source 1 | Select the source for integrator input signal ($V_{in1}$) |
| BCap | Both | 1 – 31 | Select BCap ($C_B$) value based on required Integrator time constant |
| AnalogBus | Both | AnalogOutBus_0 | SC block output is routed to Analog output bus (which is then routed to pin) |
| CompBus | Both | Disable | Not used |
| Autozero | Both | On | Autozero (input offset voltage correction) enabled |
| CCap | Type C only | 0 | Not used |
| ARefMux | Both | AGND | SC block reference is analog ground. The integrator output ramps up or down depending on whether input voltage is greater than or less than AGND respectively. |
| FSW1 | Both | On | FSW1 is enabled |
| FSW0 | Both | Off | FSW0 is disabled |
| BMux | Both | Source 2 | Select the source for integrator input signal ($V_{in2}$) |
| Power | Both | High | SC block is operated in high power mode |
| AMux | Type D only | Source 1 | Select the source for integrator input signal ($V_{in1}$) |
| BSW (SD) | Type D only | ON | Switching enabled for B input |

### Differentiator



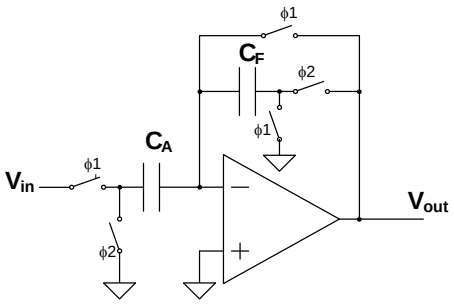

$$Gain = \frac{V_{out}}{V_{in}} = -\left(1 - z^{-1}\right)\frac{C_B}{C_F} \cong -s\left(\frac{1}{f_s}\frac{C_B}{C_F}\right)$$

**Note** Differentiator can be implemented only in Type-D SC block because of presence of BSW switch.

| SCBlock | | |
|---|---|---|
| **Parameter** | **Value** | **Comments** |
| FCap | 16/32 | Select FCap based on differentiator gain requirement |
| ClockPhase | Norm | Options: Norm, Swap |
| ASign | Pos | Options:<br>Pos – Non-inverting configuration<br>Neg – Inverting Configuration |
| ACap | 0 | Disconnect 'A' input |
| AMux | x | Not used |
| BCap | 1 - 31 | Select BCap ($C_B$) value based on differentiator gain requirement |
| AnalogBus | AnalogOutBus_1 | Output routed to analog output bus |
| CompBus | Disable | Not used |
| Autozero | On | Autozero enabled |
| CCap | 0 | Not used |
| ARefMux | AGND | Reference of SC-Block set to AGND |
| FSW1 | On | FSW1 is enabled |
| FSW0 | On | FSW0 is enabled |
| BSW | Off | BSW switch is disabled |
| BMux | source | Select $V_{in}$ |
| Power | High | High power mode |

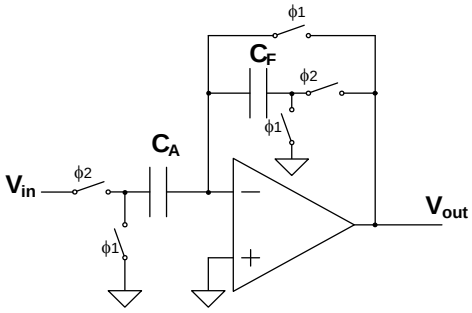
### Non-Inverting and Inverting Amplifier

Figure 36. Non-Inverting Amplifier




$$V_{out} = \frac{C_A}{C_F} V_{in}$$

Figure 37. Inverting Amplifier

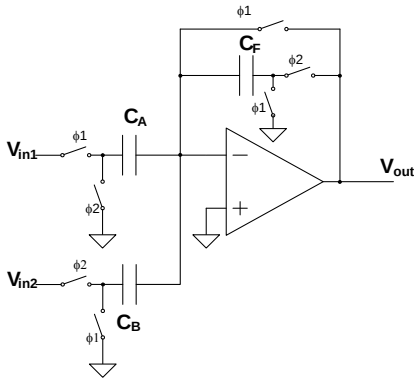



$$V_{out} = -\frac{C_A}{C_F} V_{in}$$

| SCBlock | | | |
|---|---|---|---|
| **Parameter** | **Type C / D** | **Value** | **Comments** |
| FCap | Both | 16 / 32 | Select FCap ($C_F$) based on amplifier gain requirement |
| ClockPhase | Both | Norm | Options – Norm, Swap |
| ASign | Both | Pos / Neg | Pos - Non-Inverting amplifier configuration<br>Neg – Inverting amplifier configuration |
| ACap | Both | 1 – 31 | Select ACap ($C_A$) value based on amplifier gain requirement |
| ACMux | Type C only | Source 1 | Select the source for amplifier input signal ($V_{in}$) |
| BCap | Both | 0 | Disconnects B input |
| AnalogBus | Both | AnalogOutBus_0 | SC block output is routed to Analog output bus (which is then routed to pin) |
| CompBus | Both | Disable | Not used |
| Autozero | Both | On | Autozero (input offset voltage correction) enabled |
| CCap | Type C only | 0 | Not used |
| ARefMux | Both | AGND | SC block reference is analog ground. |

| SCBlock | | | |
|---|---|---|---|
| **Parameter** | **Type C / D** | **Value** | **Comments** |
| FSW1 | Both | On | FSW1 is enabled |
| FSW0 | Both | On | FSW0 is enabled |
| BMux | Both | X | Not used |
| Power | Both | High | High power mode |
| AMux | Type D only | Source 1 | Select the source for amplifier input signal ($V_{in}$) |
| BSW (SD) | Type D only | X | Not used |

### Differential Amplifier

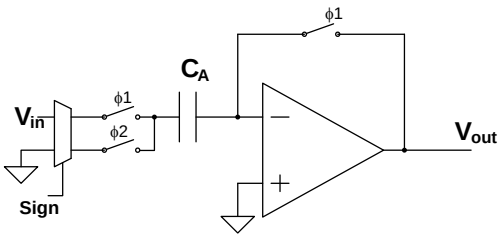



$$V_{out} = \frac{C_A}{C_F} V_{in1} - \frac{C_B}{C_F} V_{in2}$$

| SCBlock | | | |
|---|---|---|---|
| **Parameter** | **Type C / D** | **Value** | **Comments** |
| FCap | Both | 16 / 32 | Select FCap ($C_F$) based on amplifier gain requirement |
| ClockPhase | Both | Norm | Options – Norm, Swap |
| ASign | Both | Pos | Non-Inverting configuration for input $V_{in1}$ |
| ACap | Both | 1 – 31 | Select ACap ($C_A$) value based on amplifier gain requirement |
| ACMux | Type C only | Source 1 | Select the source for amplifier input signal ($V_{in1}$) |
| BCap | Both | 1 – 31 | Select BCap ($C_B$) value based on amplifier gain requirement |
| AnalogBus | Both | AnalogOutBus_0 | SC block output is routed to Analog output bus (which is then routed to pin) |
| CompBus | Both | Disable | Not used |
| Autozero | Both | On | Autozero (input offset voltage correction) enabled |
| CCap | Type C only | 0 | Not used |
| ARefMux | Both | AGND | SC block reference is analog ground |
| FSW1 | Both | On | FSW1 is enabled |
| FSW0 | Both | On | FSW0 is enabled |
| BMux | Both | Source 2 | Select the source for amplifier input signal ($V_{in2}$) |

| SCBlock | | | |
|---|---|---|---|
| **Parameter** | **Type C / D** | **Value** | **Comments** |
| Power | Both | High | High power mode |
| AMux | Type D only | Source 1 | Select the source for amplifier input signal ($V_{in1}$) |
| BSW (SD) | Type D only | On | Enable switching for input B |

### Comparator




$$V_{out} = HIGH\ when\ V_{in} > AGND$$

$$V_{out} = LOW\ when\ V_{in} < AGND$$

| | SCBlock | | |
|---|---|---|---|
| **Parameter** | **Type C / D** | **Value** | **Comments** |
| FCap | Both | X | Not used |
| ClockPhase | Both | Norm | Φ1 – charge acquisition<br>Φ2 – charge transfer |
| ASign | Both | Pos | Non-Inverting configuration |
| ACap | Both | >0 | Select value greater than 0 |
| ACMux | Type C only | source | Select the source for integrator input signal (input $V_{in}$) |
| BCap | Both | 0 | Disconnects ‘B’ input |
| AnalogBus | Both | Disable | Not used |
| CompBus | Both | Enable | Routes the comparator output to bus |
| Autozero | Both | On | Autozero enabled, but no effect on the offset correction |
| CCap | Type C only | 0 | Not used |
| ARefMux | Both | AGND | SC block reference is analog ground. |
| FSW1 | Both | Off | FSW1 is disabled |
| FSW0 | Both | Off | FSW0 is disabled |
| BMux | Both | x | Not used |
| Power | Both | High | High power mode |
| AMux | Type D only | Source | Select the source for comparator input signal (input $V_{in}$) |
| BSW (SD) | Type D only | x | Not used |

## Document History

Document Title: AN2041 - Understanding PSoC® 1 Switched Capacitor Analog Blocks

Document Number: 001-40440

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | 1532004 | DWV | 10/02/2007 | New application note |
| *A | 1793485 | DWV | 12/03/2007 | Added Appendix E: Input Multiplexer Connections |
| *B | 2344389 | CFW | 04/11/2008 | Appendix A and Appendix B - figures transposed<br>Corrected a couple of typos |
| *C | 3210347 | MAXK | 03/30/2011 | Updated projects to PD 5.1 SP1<br>Added Isolated Analog Driver project (was missing from previous versions)<br>General formatting updates<br>Added document history table<br>Updated figures<br>Updated Title and Abstract |
| *D | 3244236 | MAXK | 04/29/2011 | Corrected symbol fonts in various figures. |
| *E | 3671850 | RJVB | 07/10/2012 | Updated template.<br>Added detailed explanation for inverting amplifier, non-inverting amplifier, comparator, differentiator and integrator.<br>Updated figures.<br>Added Appendix G: SC-Block Applications Cook Book. |
| *F | 4393365 | RJVB | 05/29/2014 | Sunset Review. |
| *G | 5705924 | AESATMP9 | 04/21/2017 | Updated logo and copyright. |

## Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

## Products

| | |
|---|---|
| ARM® Cortex® Microcontrollers | cypress.com/arm |
| Automotive | cypress.com/automotive |
| Clocks & Buffers | cypress.com/clocks |
| Interface | cypress.com/interface |
| Internet of Things | cypress.com/iot |
| Memory | cypress.com/memory |
| Microcontrollers | cypress.com/mcu |
| PSoC | cypress.com/psoc |
| Power Management ICs | cypress.com/pmic |
| Touch Sensing | cypress.com/touch |
| USB Controllers | cypress.com/usb |
| Wireless Connectivity | cypress.com/wireless |

## PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

## Cypress Developer Community

Forums | WICED IOT Forums | Projects | Videos | Blogs | Training | Components

## Technical Support

cypress.com/support



Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709