AN202720

Connecting Cypress Flash Memory to a System Address Bus

AN202720 discusses how flash memories may be connected to a system address bus and how software should issue device commands to the flash devices.

1 Introduction

How Flash memories may be connected to a system address bus and how software should issue device commands to the Flash devices.

2 Organization Modes

Most Cypress Flash devices have either a byte-wide internal organization or can be used in “byte mode”, a mode that presents an 8-bit wide organization to the system. Many Cypress Flash devices can also present a 16-bit wide organization to the system referred to as “word mode”. Cypress also offers 32-bit wide Flash in both standalone Flash, for the Automotive Industry (S29CD family), and Multi Chip Products for general use.

3 Flash Address Pin Labels

The address pins for byte-wide-only Flash devices are labeled A0 to AN, where AN is the highest order address bit. A0 is the lowest order address bit.

The address pins for x8/x16 Flash devices are labeled in terms of Byte/Word selection.

In word mode, the pins are labeled as A0 through AN, where AN is the highest order address bit. A0 is the lowest order address bit. In word mode there is no means to individually select a byte within a word.

In byte mode, the pins are labeled as DQ15/ A-1 through AN. In Byte mode the DQ15/ A-1 pin functions as the lowest order address bit, and is referred to as A-1 (read “A minus 1”, to indicate that the bit is one order lower than A0).

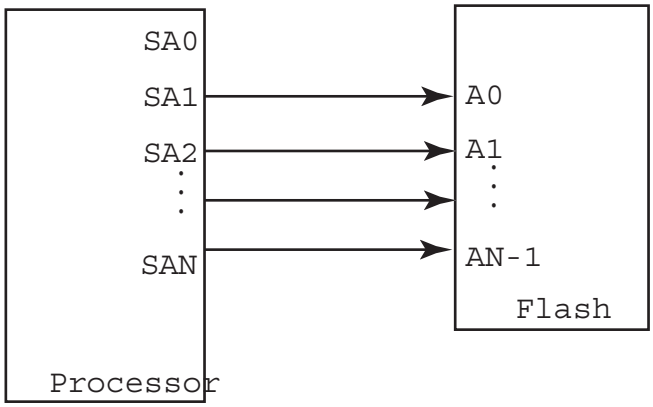
4 Word Mode Address Interface

A common situation is a byte-addressed processor (see note), which is connected to a 16-bit flash device.

In a byte-addressed processor system, when consecutive 16-bit word locations are read, the address from one location to the next is increased by two. Take a processor with 4-bit address bus and 16-bit data bus as an example, the consecutive word addresses will look like this: 0000, 0010, 0100, 0110, etc. If the processor address bits are connected to the same order Flash address bits (SA0 -> A0, SA1 -> A1, and so on), odd locations of the Flash memory will not be read. In order to avoid this situation, the processor address bit SA1 should be connected to the Flash address bit A0, SA2 should be connected to A1 and so on (As shown in Figure 1). Processor address bit SA0 is not connected to the Flash device. The addresses (in above example) seen by the Flash device with this connection will be consecutive and look like this: 000, 001, 010, 011.

Note: *A byte-addressed Processor is a Processor with an address bus whose basic unit of address is byte. For example the 8051 and 68HC11.*

Figure 1. Byte Address Processor Connected to Word Mode Flash



Another common situation is a byte-addressed processor connected to either a x8/x16 Flash device operated in byte mode (Figure 2), or a x8 Flash device (Figure 3.). In this case, each consecutive byte access from the processor needs to select a specific byte in the Flash memory array. The processor address bit SA0 is connected to the Least Significant Bit (LSB) of the Flash address (which is labeled A0 in x8-only devices, and DQ15/A-1 in x8/x16 devices).

Figure 2. Byte Address Processor Connected to Byte Mode x8/x16 Flash

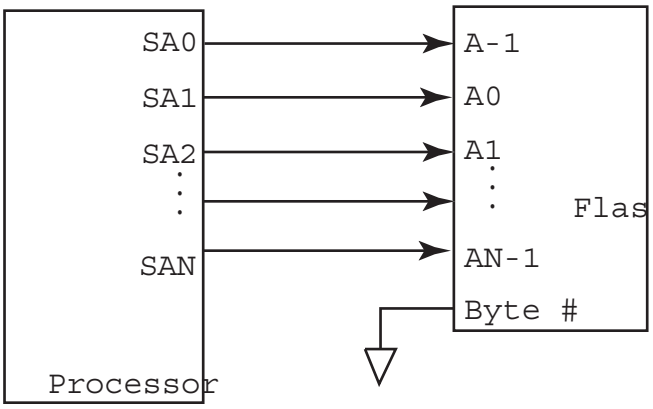
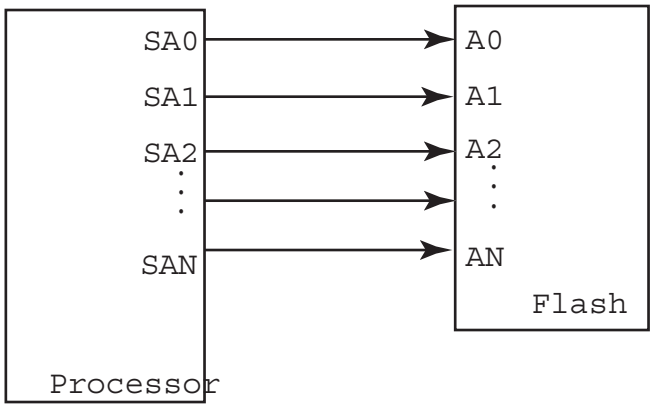


Figure 3. Byte Address Processor Connected to x8-only Flash



Cypress Flash devices can also be used in parallel, such as might be the case when using two x8-only devices in parallel to form a 16-bit data bus (Figure 4.). This situation is extensible to 32-bit processor buses when combined with four byte-wide devices in parallel (Figure 5), or two word-wide devices in parallel (Figure 6). In these cases, the Flash devices are being treated as portions of a wider memory. Higher order processor address lines are

connected to lower order Flash address lines for the same reason discussed in "Word Mode Address Interface" section.

Note: *The DQ15/A-1 signal only appears in x8/x16 devices. When operating in x8 (or byte) mode, the DQ15/A-1 signal is the LSB bit of the Flash address bus. In x16 (or word) mode, the DQ15/A-1 signal is the MSB bit of the Flash data bus and A0 is the LSB of the Flash address bus.*

Figure 4. Byte Address Processor Connected to Two x8-only Flash on a 16-Bit-Wide Data Bus

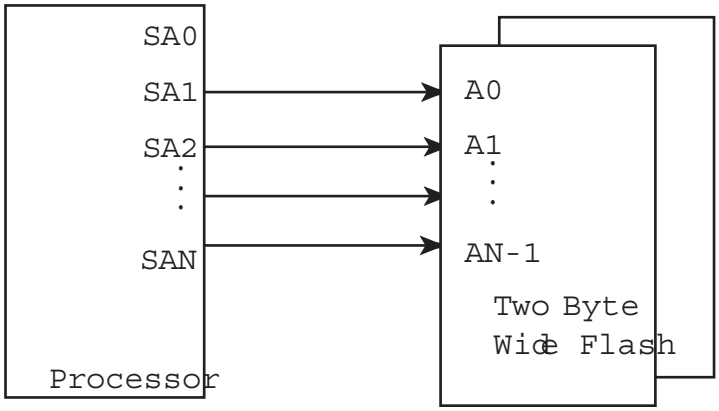


Figure 5. Byte Address Processor Connected to Four x8-Only Flash on a 32-Bit-Wide Data Bus

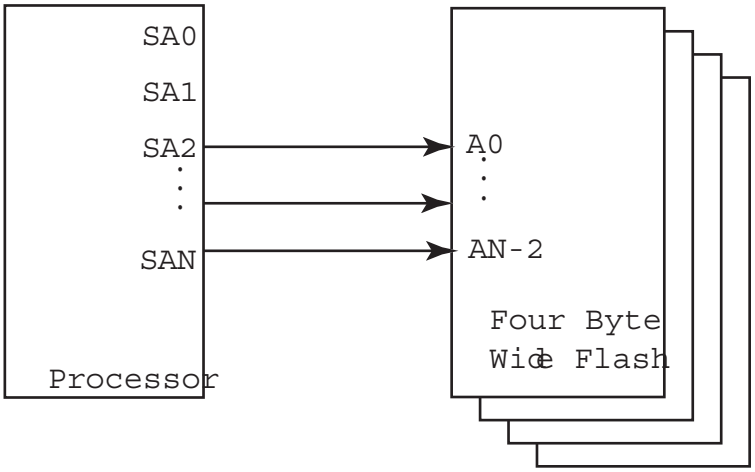
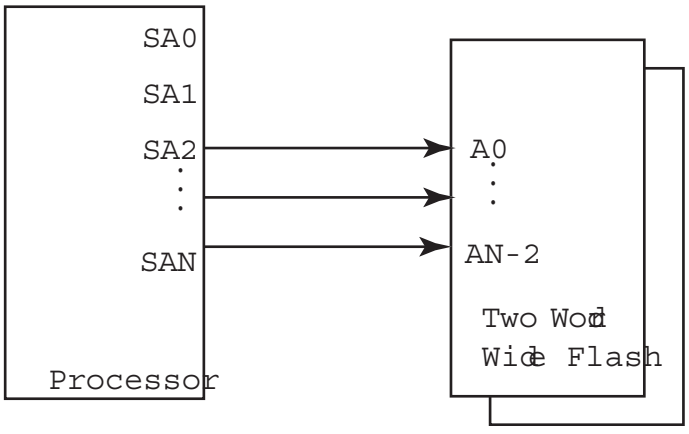


Figure 6. Byte Address Processor Connected to Two x16 Flash on a 32-Bit-Wide Data Bus



What is important from the above system examples is to note that the mapping between processor address lines and Flash address lines changes depending on the Flash device mode (x8/x16 mode) in use, the data bus width of the system and how the processor address bus is connected to the Flash address bus.

The Flash device monitors and expects certain pattern values on address bits A10 - A0, data bits DQ7 -DQ0 when commands are written to it. System designers must therefore supply the expected address patterns and values from the Flash device point of view.

4.1 Address Command Patterns on X8/x16 Flash devices

For each command listed in Table 3, there is an associated set of address/data patterns that must be written in a particular sequence in order to instruct the Flash device to perform specific functions.

It can also be seen that the address patterns, 555, 2AA required for each command sequence are different for Byte mode and Word mode. Table 1 and Table 2 help visualize the address pins and address values.

The device internal control logic is monitoring the address bits A10-A0, and data bits DQ7-DQ0 for the correct command patterns. The rest of the address bits and data bits are "Don't Care".

Table 1. Command Patterns in Word Mode and Byte Mode

First Unlock cycle/ Address Pattern												
x8/x16 Flash Address	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	A-1
Word Mode	1	0	1	0	1	0	1	0	1	0	1	
(Hex)	5			5				5				
Byte Mode	1	0	1	0	1	0	1	0	1	0	1	0
(Hex)	A			A				A				

Table 2. Command Patterns in Word Mode and Byte Mode (continued)

Second Unlock cycle/ Address Pattern												
x8/x16 Flash Address	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	A-1
Word Mode	0	1	0	1	0	1	0	1	0	1	0	
(Hex)	2			A				A				
Byte Mode	0	1	0	1	0	1	0	1	0	1	0	1
(Hex)	5			5				5				

Table 3. x8/x16 Flash Basic Command Definitions

Command Sequence			Cycles	Bus Cycles											
				First		Second		Third		Fourth		Fifth		Sixth	
				Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read			1	RA	RD										
Reset			1	XXX	F0										
Autoselect	Manufacturer ID	Word	4	555	AA	2AA	55	555	90	X00	01				
		Byte		AAA		555		AAA							
	Device ID, Top Boot Block	Word	4	555	AA	2AA	55	555	90	X01	22DA				
		Byte		AAA		555		AAA		X02	DA				
	Device ID, Bottom Boot Block	Word	4	555	AA	2AA	55	555	90	X01	225B				
		Byte		AAA		555		AAA		X02	5B				
	Sector Protect Verify	Word	4	555	AA	2AA	55	555	90	(SA) X02	XX00				
											XX01				
		Byte		AAA		555		AAA		(SA) X04	00				
											01				
Program		Word	4	555	AA	2AA	55	555	A0	PA	PD				
		Byte		AAA		555		AAA							
Unlock Bypass		Word	3	555	AA	2AA	55	555	20						
		Byte		AAA		555		AAA							
Unlock Bypass Program			2	XXX	A0	PA	PD								
Unlock Bypass Reset			2	XXX	90	XXX	00								
Chip Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
		Byte		AAA		555		AAA		AAA		555		AAA	
Sector Erase		Word	6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
		Byte		AAA		555		AAA		AAA		555			
Erase Suspend			1	XXX	B0										
Erase Resume			1	XXX	30										

The command definition tables, provided in all Cypress Flash data sheets, are structured to represent what the Flash is required to “see” on its address lines and data lines for a particular operation to execute. Since the Flash address may be connected in different ways (as illustrated earlier), the address values in the tables may need to be “shifted” accordingly when writing software driver code, to reflect the processor and Flash address bus relationship, in order for the Flash device to recognize the proper bit patterns.

Developers therefore should be aware that the Command Definition Tables in Cypress Flash data sheets are from the Flash point of view, but that the code has to be constructed from the Processor point of view.

4.2 Address Command Patterns on 16-Bit and higher Data Bus Width Systems

The same is true when more than one Flash device is used in parallel to serve a wider data bus. The relative positions of processor and Flash address lines will shift more as shown in Figure 4., Figure 5, and Figure 6. The expected patterns shown in the Command Definition Table must be shifted up in the Processor code viewpoint so the required patterns remain on the desired Flash address pins. Table 4, Table 5, Table 6, and Table 7 help visualize the relationships in a 16-bit and 32-bit data bus system.

Table 4 and Table 5 show the address patterns 555h, 2AAh from the Flash and Processor (software) point of view in a 16-bit system. Note that the address connections between the Flash and Processor are shifted by one bit for the reason discussed in Word Mode Address Interface.

Table 6 and Table 7 show the address patterns 555h, 2AAh from the Flash and Processor (software) point of view in a 32-bit system. Note that the address connections between the Flash and Processor are shifted by two bits for similar reasons discussed in Word Mode Address Interface.

Table 4. Address Pattern 555h in a 16-bit System

	Address Bits and Values											
Processor Address	SA11	SA10	SA9	SA8	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
Flash Address	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
Address Pattern Required By Flash (555h)	1	0	1	0	1	0	1	0	1	0	1	
Address Pattern from Software Point of view (AAAh)	1	0	1	0	1	0	1	0	1	0	1	0

Table 5. Address Pattern 2AAh in a 16-bit System

Description	Address Bits and Values											
Processor Address	SA11	SA10	SA9	SA8	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
Flash Address	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	
Address Pattern Required By Flash (2AAh)	0	1	0	1	0	1	0	1	0	1	0	
Address Pattern from Software Point of view (554h)	0	1	0	1	0	1	0	1	0	1	0	0

Table 6. Address Pattern 555h in a 32-bit System

Description	Address Bits and Values												
Processor Address	A12	SA11	SA10	SA9	SA8	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
Flash Address	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		
Address Pattern Required By Flash (555h)	1	0	1	0	1	0	1	0	1	0	1		
Address Pattern from Software Point of view (1554h)	1	0	1	0	1	0	1	0	1	0	1	0	0

Table 7. Address Pattern 2AAh in a 32-bit System

Description	Address Bits and Values												
Processor Address	A12	SA11	SA10	SA9	SA8	SA7	SA6	SA5	SA4	SA3	SA2	SA1	SA0
Flash Address	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		
Address Pattern Required By Flash (2AAh)	0	1	0	1	0	1	0	1	0	1	0		
Address Pattern from Software Point of view (0AA8h)	0	1	0	1	0	1	0	1	0	1	0	0	0

4.3 Some Address Lines are Don't Care

Not all address bits are checked for the address patterns by the Flash memory. The upper address bits, AN-A11, are “don't care” from the viewpoint of any Cypress Flash device. For some AMD legacy 5-volt Flash devices, AN - A14 bits are “Don't Care”. Always check the notes below the Command Definition table in the datasheet to determine which address bits are the “Don't Care” bits.

4.4 Handling Bank, Sector, and Programming Offsets

In certain commands, a bank, sector, or programming offset address must be given in order for the command to correctly begin. Flash address bits AN-A12 are used for these purposes.

Bank addresses (listed as “BA” in Cypress data sheets) are used in Simultaneous Read-Write devices to uniquely identify one of the device's specific banks. For example, the S29JL064H data sheet specifies that address bits A21-A19 uniquely select a specific bank.

Sector Addresses (SA in Cypress data sheets) are used for sector specific Flash operations (such as Sector Erase and Sector Protect Verify). For devices with 64K bytes sectors address bits AN-A12 are used to uniquely specify a sector. Refer to individual data sheet for the exact sector addresses.

The Program Address Offset (PA in Cypress data sheets) is simply an offset from the beginning of the device into the Flash Array. It is simply the desired byte offset into the array in which data will be programmed. The offset address can span the entire address range (AN-A0). None of the address bits are considered “don't cares."

Flash sector and bank sizes are always quoted in terms of bytes/words in the datasheets. In the most common system implementation using a single byte or word mode Flash, the system byte address of the processor matches with the quoted sector address boundaries since both are in terms of bytes. There is no special adjustment needed for the system address in these common system implementations. However, where parallel Flash devices are used on a wider data bus, the bank, sector, and programming offset addresses will have to be shifted up to match the Flash device viewpoint.

5 Conclusion

The Flash memory command definition tables found in all Cypress Flash datasheets always show addresses from the viewpoint of the Flash address lines in use for the particular mode (byte or word). These tables also assume a system where the Flash memory is in an organization mode that matches the width of the data bus. Those who write software drivers for Flash devices must consider the system implementation of a single device versus two or more Flash devices in parallel when determining the degree to which addresses shown in the command tables may need to be shifted up in order for Flash devices to properly recognize the Flash commands.

For the most common system configurations, software drivers have already been written for Cypress Flash memories. These are available as C source code via the Cypress website (http://www.cypress.com).

Document History Page

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**	–	–	01/30/2006	Initial version
*A	5005436	MSWI	11/06/2015	Updated in Cypress template
*B	5866759	AESATMP8	08/29/2017	Updated logo and Copyright.

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