AN202493

Migrating from SPI nvSRAM to SPI F-RAM™

Author: Shivendra Singh

Associated Part Family: SPI nvSRAM, SPI F-RAM

Associated Code Examples: None

Related Application Notes: AN304, AN89659

AN202493 provides guidelines for migrating from SPI nvSRAM to SPI F-RAM™. It recommends equivalent SPI F-RAM devices, describes package and feature differences, and discusses the hardware and firmware modifications that need to be made for a successful migration.

Contents

1 Introduction

F-RAM (ferroelectric random-access memory) is a nonvolatile memory that uses a ferroelectric capacitor to store data. The data written in F-RAM is nonvolatile instantaneously. Unlike EEPROM and flash, F-RAM writes data to nonvolatile memory at bus speed.

nvSRAM is a SRAM memory with a nonvolatile element embedded in each memory cell. The embedded nonvolatile elements incorporate Silicon-Oxide-Nitride-Oxide-Silicon (SONOS) Quantum Trap technology. The SRAM provides infinite read and write cycles, while the Quantum Trap cells offer highly reliable nonvolatile storage of data. Data transfers from the SRAM to the nonvolatile elements (STORE operation) take place automatically at power down. On power up, data is restored to the SRAM from the nonvolatile memory (RECALL operation).

Cypress has been supporting a few SPI nvSRAM parts with the status NRND (not recommended for new designs) and is offering replacement options for these devices with its SPI F-RAM products. This application note provides details on migrating from SPI nvSRAM to SPI F-RAM. It discusses the differences in packaging, features, and timing and the modifications required in hardware and firmware to make the migration successful. Table 1 lists the suggested SPI F-RAM replacement parts for the SPI nvSRAM.

Refer to the application notes AN304 – SPI Guide for F-RAM™ and AN89659 – Interfacing SPI F-RAM with PSoC® 4 for SPI F-RAM design guidelines and a firmware example.

This application note uses the generic part numbers CY14xxxxQ1x and CY14xxxxQ2x to represent the SPI nvSRAM part options in the 8-pin DFN package built using the first SPI nvSRAM silicon (Rev **). Similarly, the CY14xxxxQ1xA and CY14xxxxQ2xA part numbers are used to represent the SPI nvSRAM part options in the 8-pin SOIC package built using the new SPI nvSRAM silicon (Rev A).

Table 1. SPI nvSRAM to SPI F-RAM Migration Options

Density	Package	nvSRAM Parts				Suggested F-RAM (Replacement) Parts			
		Part No.	SPI Freq.	Voltage	Temp.	Part No.	SPI Freq.	Voltage	Temp.
64 Kb	8-pin SOIC	CY14MB064Q2B	40 MHz	2.7 V to 3.6 V	– 40 ˚C to + 85 ˚C	FM25CL64B	20 MHz	2.7 V to 3.65 V	– 40 ˚C to + 85 ˚C
	8-pin SOIC	CY14MB064Q2A	40 MHz	2.7 V to 3.6 V	– 40 ˚C to + 105 ˚C	FM25CL64B	16 MHz	3.0 V to 3.6 V	– 40 ˚C to + 125 ˚C
	8-pin SOIC	CY14ME064Q2A	40 MHz	4.5 V to 5.5 V	– 40 ˚C to + 105 ˚C	FM25640B	4 MHz	4.5 V to 5.5 V	- 40 ˚C to + 125 ˚C
256 Kb	8-pin DFN	CY14B256Q2	40 MHz	2.7 V to 3.6 V	– 40 ˚C to + 85 ˚C	FM25V02A	40 MHz	2.0 V to 3.6 V	– 40 ˚C to + 85 ˚C
	8-pin SOIC	CY14B256Q2A	40 MHz	2.7 V to 3.6 V	– 40 ˚C to + 85 ˚C	FM25V02A	40 MHz	2.0 V to 3.6 V	– 40 ˚C to +85 ˚C
	8-pin SOIC	CY14E256Q5A	40 MHz	4.5 V to 5.5 V	– 40 ˚C to + 105 ˚C	No suggested replacement part			
512 Kb	8-pin SOIC	CY14B512Q2A	40 MHz	2.7 V to 3.6 V	– 40 ˚C to + 85 ˚C	FM25V05	40 MHz	2.0 V to 3.6 V	– 40 ˚C to +85 ˚C
1024 Kb	8-pin DFN	CY14B101Q2	40 MHz	2.7 V to 3.6 V	– 40 ˚C to + 85 ˚C	FM25V20A	40 MHz	2.0 V to 3.6 V	– 40 ˚C to +85 ˚C
	8-pin SOIC	CY14B101Q2A	40 MHz	2.7 V to 3.6 V	– 40 ˚C to + 85 ˚C	FM25VN10 FM25V10	40 MHz	2.0 V to 3.6 V	– 40 ˚C to +85 ˚C
	16-pin SOIC	CY14V101Q3	40 MHz	V_{CC} = 2.7 V to 3.6 V V_{CCQ} = 1.65 V to 1.95 V	– 40 ˚C to + 85 ˚C	No suggested replacement part			

The suggested SPI F-RAM parts are similar to the SPI nvSRAM parts in their features and access protocols, operating conditions, density, and package type, but they are not identical and pin-for-pin drop-in replacements. Therefore, you need to be aware of the differences when replacing an SPI nvSRAM with an SPI F-RAM. This application note discusses the similarities and differences between the two to assist you during the migration.

2 SPI nvSRAM and SPI F-RAM Compatibility

This section discusses the similarities and differences between SPI nvSRAMs and SPI F-RAMs with respect to attributes such as pin and package, commands (opcode), features and specifications, hardware, and firmware. Review these attributes and make the necessary changes in your design.

2.1 Pin Compatibility

All I/O pins except Pin 3 match between SPI nvSRAM and SPI F-RAM, as described in Table 2. Pin 3 is the write protect ($\overline{WP}$) pin in SPI F-RAM, while it is the V_{CAP} pin in SPI nvSRAM in the CY14xxxxQ2x/CY14xxxxQ2xA packages. The SPI nvSRAM pinout in the CY14xxxxQ1x/CY14xxxxQ1xA packages is identical to that in the SPI F-RAM 8-pin package.

Table 2. Pin Comparison

Pin No	nvSRAM Pin (CY14xxxxQ1x/ CY14xxxxQ1xA)	nvSRAM Pin (CY14xxxxQ2x/ CY14xxxxQ2xA)	F-RAM Pin (FM25xxxx)	Pin Description
1	$\overline{CS}$	$\overline{CS}$	$\overline{CS}$	Chip Select: Activates the device when pulled LOW. Driving this pin HIGH puts the device in low-power standby mode.
2	SO	SO	SO	Serial Output: Pin for output of data through SPI.
3	$\overline{WP}$	V_{CAP}	$\overline{WP}$	Write Protect: Implements hardware write protection in SPI.
				AutoStore Capacitor: Supplies power to the nvSRAM during power loss to STORE data from the SRAM to nonvolatile elements. If AutoStore is not needed, the V_{CAP} pin must be left as NC (no connect). It must never be connected to ground.
4	V_{SS}	V_{SS}	V_{SS}	Ground
5	SI	SI	SI	Serial Input: Pin for input of all SPI instructions and data.
6	SCK	SCK	SCK	Serial Clock: Runs at speeds up to a maximum of the SPI clock frequency (f_{SCK}). Serial input is latched at the rising edge of the clock. Serial output is driven at the falling edge of the clock.
7	$\overline{HOLD}$	$\overline{HOLD}$	$\overline{HOLD}$	HOLD Pin: Suspends serial operation.
8	V_{CC}	V_{CC}	V_{DD}	Power supply

2.2 Package Compatibility

This section describes the SPI nvSRAM and SPI F-RAM package compatibility for migration. Table 3 lists the packages, package dimensions, and applicability to SPI nvSRAMs and SPI F-RAMs.

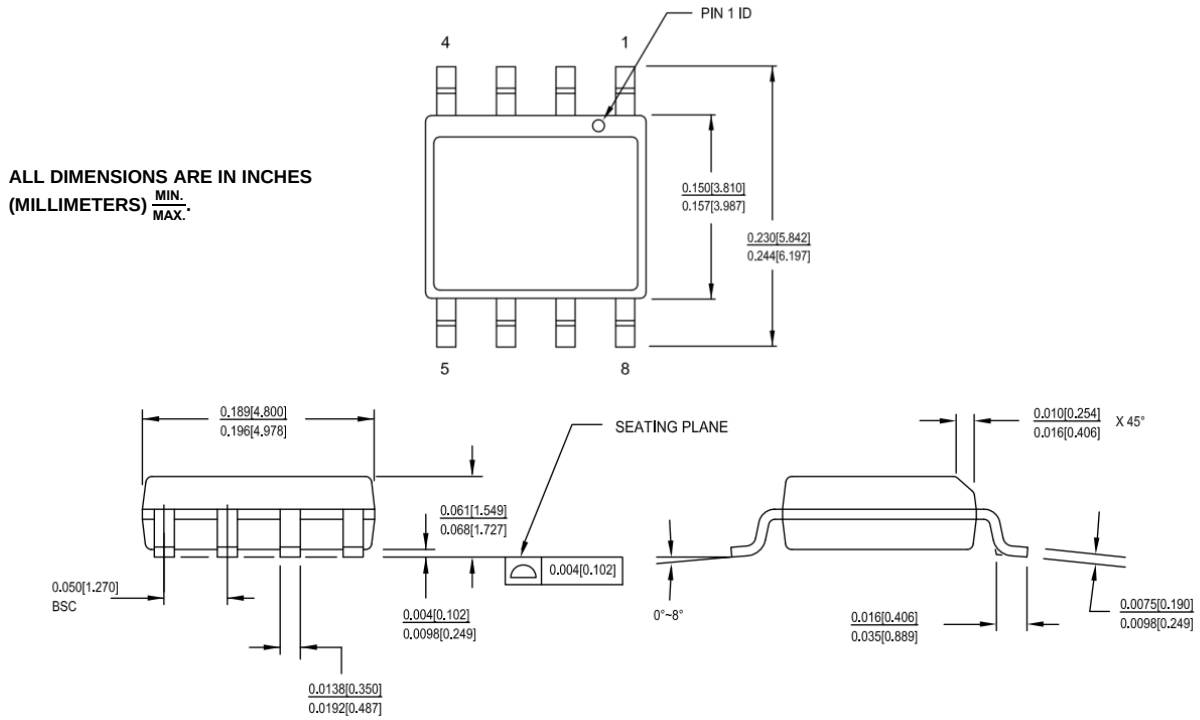
Table 3. Package Comparison

Package, Spec No.	Length (mm)	Width (mm)	Height (mm)	Pitch (mm)	Exposed Pad (mm)	SPI nvSRAM	SPI F-RAM
8-pin SOIC, 51-85066	4.89 ± 0.09	6.02 ± 0.18	1.64 ± 0.09	1.27	NA	√	√
8-pin DFN, 001-85260	4.5 ± 0.10	4.0 ± 0.10	0.75 ± 0.05	0.95	L = 3.6 ± 0.10 W = 2.6 ± 0.10	NA	√
8-pin DFN, 001-85579	5.0 ± 0.10	6.0 ± 0.10	0.75 ± 0.05	1.27	L = 4.0 ± 0.10 W = 2.3 ± 0.10	NA	√
8-pin DFN, 001-50671	5.0 ± 0.10	6.0 ± 0.10	0.75 ± 0.05	1.27	L = 4.0 ± 0.10 W = 3.0 ± 0.10	√	NA

2.2.1 8-Pin SOIC Package

All SPI nvSRAM 8-pin SOIC package dimensions (see Figure 1) are identical to those of the SPI F-RAM 8-pin package. Therefore, migrating from SPI nvSRAM to SPI F-RAM does not require a package footprint update in the PCB layout.

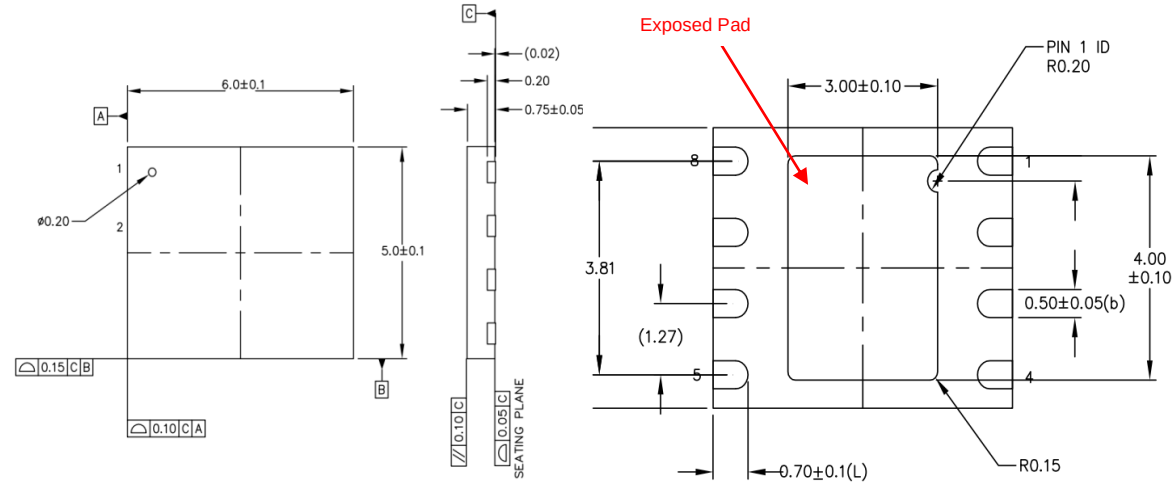
Figure 1. 8-Pin SOIC (150 Mils) Package Outline, 51-85066



2.2.2 8-Pin DFN Package

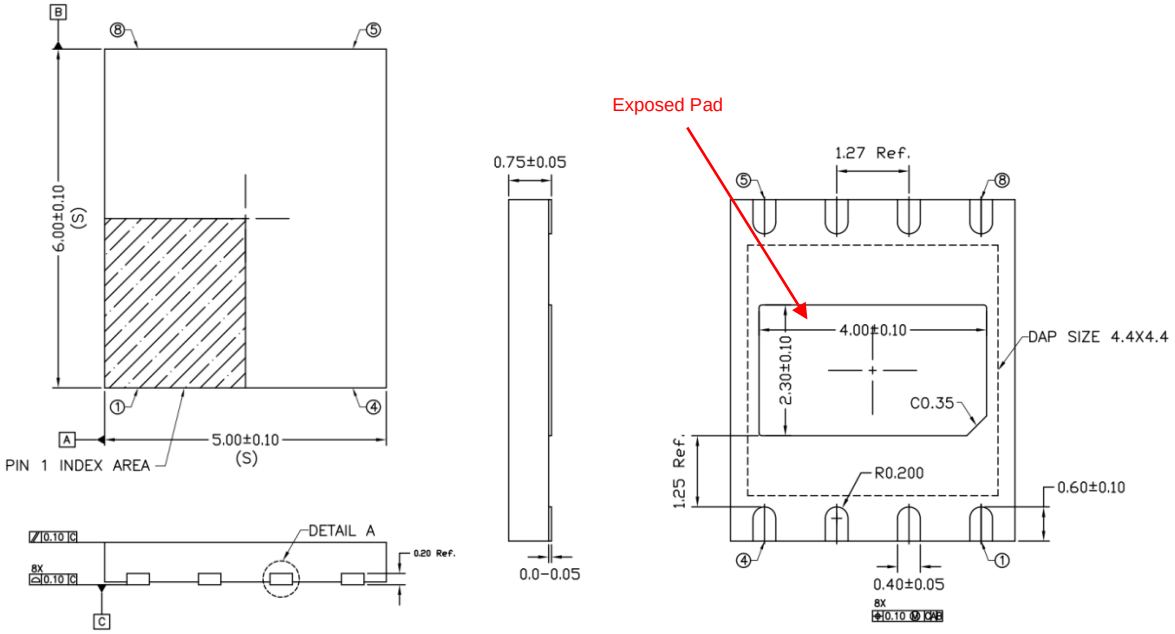
The SPI nvSRAM 8-pin DFN package (see Figure 2) dimensions are not identical to those of the SPI F-RAM 8-pin DFN package (see Figure 3 and Figure 4) for all density options. Therefore, migrating from SPI nvSRAM to SPI F-RAM may require a package footprint change in the PCB layout. Refer to Table 3 for the DFN package footprint differences between SPI nvSRAM and the suggested SPI F-RAM replacement part.

Figure 2. SPI nvSRAM 8-Pin DFN (5 × 6 × 0.85 mm) Package Outline, 001-50671



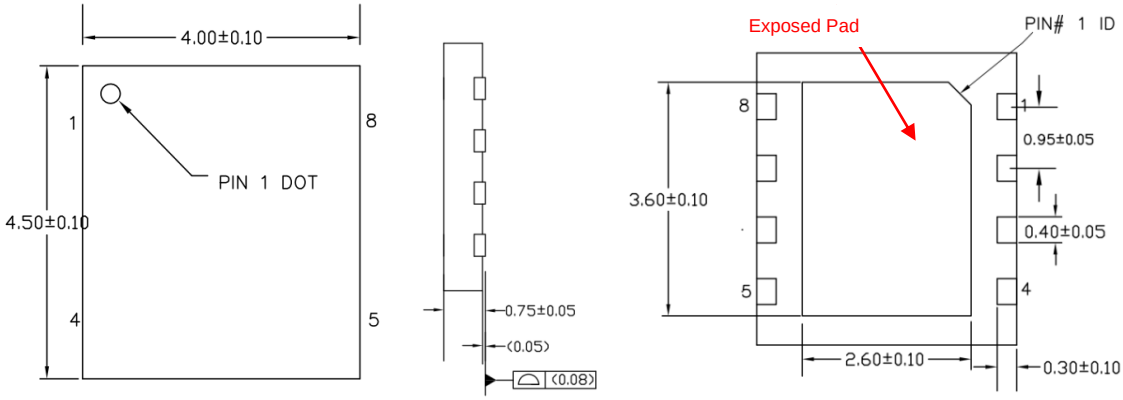
ALL DIMENSIONS ARE IN MILLIMETERS.

Figure 3. SPI F-RAM 8-Pin DFN (5 × 6 × 0.75 mm) Package Outline, 001-85579



ALL DIMENSIONS ARE IN MILLIMETERS.

Figure 4. F-RAM 8-Pin DFN (4.0 × 4.5 × 0.8 mm) Package Outline, 001-85260



ALL DIMENSIONS ARE IN MILLIMETERS.

Note: The SPI F-RAM exposed pad is not connected to the die and hence should be left floating. Ensure that the exposed pad of the SPI F-RAM DFN package is not soldered on the PCB when migrating. Soldering it will cause the SPI F-RAM die to be exposed to excessive heat, which can result in bit failures and margin loss.

2.3 Command (Opcode) Compatibility

Table 4 compares the SPI nvSRAM and SPI F-RAM opcodes.

Table 4. Command (Opcode) Comparison

Command	Opcode (Hex)	Command Description	SPI nvSRAM	SPI F-RAM	Comments
WREN	06h	Set write enable latch	√	√	Identical features between SPI nvSRAM and SPI F-RAM.
WRDI	04h	Reset write enable latch	√	√	
RDSR	05h	Read Status Register	√	√	
WRSR	01h	Write Status Register	√	√	
READ	03h	Read memory data	√	√	
WRITE	02h	Write memory data	√	√	
FSTRD	0Bh	Fast read memory data	√	√	Supported in all 128-Kb and above F-RAM densities. Supported in revision “A” silicon of SPI nvSRAM CY14xxxxQxA with SPI access above 40 MHz SPI.
SLEEP	B9h	Enter sleep mode	√	√	Supported in all 128-Kb and above F-RAM densities. Supported in revision “A” silicon of SPI nvSRAM CY14xxxxQxA. Refer to the Sleep Mode (SLEEP) Command section for details on the SLEEP command differences between SPI nvSRAM and SPI F-RAM.
RDID	9Fh	Read device ID	√	√	Supported in all 128-Kb and above F-RAM densities. Supported in revision “A” silicon of SPI nvSRAM CY14xxxxQxA. Refer to the Read Device ID (RDID) Command section for details on the RDID command differences between SPI nvSRAM and SPI F-RAM.
RDSN/ SNR	C3h	Read serial number	√	√	Supported only in F-RAM with the unique serial number feature (FM25VN10). Supported in revision “A” silicon of SPI nvSRAM CY14xxxxQxA. Refer to the Read Serial Number (RDSN, SNR) Command section for details on the RDSN command differences between SPI nvSRAM and SPI F-RAM.

Command	Opcode (Hex)	Command Description	SPI nvSRAM	SPI F-RAM	Comments
WRSN	C2h	Write serial number	√	X	Supported in revision “A” silicon of SPI nvSRAM CY14xxxxQxA. Not supported in SPI F-RAM. Applications using the write serial number (WRSN) feature in SPI nvSRAM cannot migrate to SPI F-RAM. You can implement the serial number write by reserving an 8-byte space in the main memory array. However, this reserved space cannot be made “read only,” unlike in SPI nvSRAM, by setting the SNL bit in the Status Register to make the serial number read only.
STORE	3Ch	Software STORE	√	X	These are SPI nvSRAM specific commands. They are undefined opcodes for the SPI F-RAM and will be ignored when executed. Refer to the nvSRAM Special Features section for details on these commands and their use considerations when migrating to SPI F-RAM.
RECALL	60h	Software RECALL	√	X	
ASENB	59h	AutoStore Enable	√	X	
ASDISB	19h	AutoStore Disable	√	X	
FAST_RDSR	09h	Fast Status Register read	√	X	Supported in revision “A” silicon of SPI nvSRAM CY14xxxxQxA with SPI access above 40 MHz SPI. These are undefined opcodes for the SPI F-RAM and will be ignored when executed.
FAST_RDID	99h	Fast read device ID	√	X	
FAST_RDSN	C9h	Fast serial number read	√	X	

2.4 Status Register Compatibility

Status Register access in SPI nvSRAM and SPI F-RAM is identical. However, some “don’t care” bits in the SPI nvSRAM are writeable, while they are read-only bits in SPI F-RAM. Table 5 shows the Status Register bit definitions for the two parts and their compatibility.

Table 5. Status Register Comparison

Status Register	SPI nvSRAM	SPI F-RAM	Comments
Bit0	RDY#	Don’t care	Read-only bit indicates the ready status of the device to perform a memory access. This bit is set to ‘1’ by the device while a STORE or Software RECALL cycle is in progress. This is a don’t care bit in SPI F-RAM.
Bit1	WEN	WEL	Identical behavior in SPI nvSRAM and SPI F-RAM
Bit2	BP0	BP0	
Bit3	BP1	BP1	
Bit4	Don’t care	Don’t care	Identical behavior in SPI nvSRAM (Rev “A” silicon) and SPI F-RAM. These bits are read only and always return ‘0’ upon read.
Bit5	Don’t care	Don’t care	Bits are writeable and volatile in the first revision of SPI nvSRAM (CY14xxxxQx). On power up, bits are written with ‘0’.
Bit6	SNL	Don’t care	Set to '1' to lock the serial number written using the special WRSN command in revision “A” silicon of SPI nvSRAM CY14xxxxQxA. This bit is writeable and is volatile in the first revision of SPI nvSRAM (CY14xxxxQx). On power up, it is written with ‘0’. This bit is the read-only bit in 256-Kb SPI F-RAMs and always returns ‘0’ upon read. SPI F-RAMs of 512 Kb and above return ‘1’ upon read.
Bit7	WPEN	WPEN	Identical behavior in SPI nvSRAM and SPI F-RAM

Note: Bits 4 to 6 are don’t care bits for SPI F-RAM. The default value of these three bits can be ignored when migrating from SPI nvSRAM to SPI F-RAM.

2.5 Device Spec Compatibility

Table 6, Table 7, and Table 8 list all the spec differences between the two parts. A few parameters warrant some system-level analysis before replacing SPI nvSRAM with SPI F-RAM. These include output load, startup time, and power ramp (power up and power down). Figure 5 and Figure 6 depict the power cycle timing of SPI nvSRAM and SPI F-RAM respectively.

Table 6. DC Parameter Comparison

Parameter	Description	SPI nvSRAM	SPI F-RAM	Comments
V_{DD}	Power supply voltage	2.7 V to 3.6 V 4.5 V to 5.5 V	2.0 V to 3.60 V 2.7 V to 3.65 V 4.5 V to 5.5 V	SPI F-RAM operating range is wider than that of SPI nvSRAM. Therefore, migrating from SPI nvSRAM to SPI F-RAM does not require any change in the power supply voltage.
V_{IH}	Input high voltage	2.0 V to V_{CC} + 0.5 V	0.7 x V_{DD} to V_{DD} + 0.3 V	The V_{IH} (min) of SPI F-RAM follows the CMOS logic level and is proportional to the input power supply (V_{DD}). The V_{IH} (min) of SPI nvSRAM is a fixed level at a minimum of 2.0 V. Hence, you must evaluate the V_{IH} (min) compatibility when migrating to SPI F-RAM. The V_{IH} (max) of SPI F-RAM is V_{DD} + 0.3 V, while it is V_{CC} + 0.5 V for SPI nvSRAM. This limits the overshoot voltage at SPI F-RAM input pins and should be adjusted when migrating.
V_{IL}	Input low voltage	–0.5 V to 0.8 V	–0.3 V to 0.3 x V_{DD}	The V_{IL} (max) of SPI F-RAM follows the CMOS logic level and is proportional to the input power supply (V_{DD}). The V_{IL} (max) of SPI nvSRAM is a fixed level at a maximum of 0.8 V. Hence, you must evaluate the V_{IL} (max) compatibility when migrating to SPI F-RAM. The V_{IL} (min) of SPI F-RAM is –0.3 V, while it is –0.5 V for SPI nvSRAM. This limits the undershoot voltage at SPI F-RAM input pins and should be adjusted when migrating.
V_{OH}	Output high voltage	CY14xxxxQ1/ CY14xxxxQ2: 2.0 V (min) I_{OUT} = –2 mA CY14xxxxQ1A/ CY14xxxxQ2A: 2.4 V (min) For V_{CC} = 3 V (typical) I_{OUT} = –2 mA V_{CC} –0.4 V (min) For V_{CC} = 5 V (typical) I_{OUT} = -2 mA	2.4 V (min) I_{OH} = –1 mA V_{DD} – 0.8 V (min) I_{OH} = –2 mA V_{DD} – 0.2 V (min) I_{OH} = –100 µA	No change is required when migrating from SPI nvSRAM to SPI F-RAM in a typical system configuration. However, a heavily loaded system bus must ensure that V_{OH} remains within the logic levels for inputs.

Parameter	Description	SPI nvSRAM	SPI F-RAM	Comments
V_{OL}	Output low voltage	0.4 V (max) I_{OUT} = 4.0 mA	0.4 V (max) I_{OL} = +2 mA 0.2 V (max) I_{OL} = +150 µA	No change is required when migrating from SPI nvSRAM to SPI F-RAM in a typical system configuration. However, a heavily loaded system bus must ensure that V_{OL} remains within the logic levels for inputs.
V_{VCAP}	Storage capacitor	42 µF to 180 µF	NA	This is an nvSRAM specific pin for the AutoStore operation. This pin/function and associated parameters are not applicable to SPI F-RAM.
V_{VCAP}	Maximum voltage driven on V_{CAP} pin by the device	V_{CC} (max) for 3 V (typical) V_{CC} – 0.5 V (max) for 5 V (typical)	NA	

Note: All other DC parameters (except current parameters) not listed in Table 6 are equivalent. Since F-RAM is an energy-efficient nonvolatile memory technology, all DC current specifications for SPI F-RAM are better than those for SPI nvSRAM.

Table 7. AC Parameter Comparison

Parameter Description	SPI nvSRAM			SPI F-RAM			Units	Comments
	Parameter	Min	Max	Parameter	Min	Max		
Clock frequency, SCK	f_{SCK}		40	f_{SCK}		40	MHz	Identical
Clock HIGH time	t_{CH}	11		t_{CH}	11		ns	
Clock LOW time	t_{CL}	11		t_{CL}	11		ns	
Chip select setup	t_{CSS}	10		t_{CSU}	10		ns	
Chip select hold	t_{CSH}	10		t_{CH}	10		ns	
Output disable time	t_{HZCS}		20	t_{OD}		12	ns	SPI F-RAM output disables faster than that of SPI nvSRAM. There is no impact when migrating to SPI F-RAM.
Output data valid time	t_{CO}		9	t_{ODV}		9	ns	Identical
Output hold time	t_{OH}	0		t_{OH}	0		ns	Identical
$\overline{CS}$ HIGH time	t_{CS}	20		t_{D}	40		ns	This timing is higher for SPI F-RAM. You should evaluate and adjust this parameter accordingly when migrating to SPI F-RAM.
Data in rise time	Not specified			t_{R}		50	ns	Not specified in SPI nvSRAM. You should evaluate and adjust this parameter accordingly when migrating to SPI F-RAM.
Data in fall time				t_{F}		50	ns	
Data setup time	t_{SD}	5		t_{SU}	5		ns	Identical
Data hold time	t_{HD}	5		t_{H}	5		ns	Identical

Parameter Description	SPI nvSRAM			SPI F-RAM			Units	Comments
	Parameter	Min	Max	Parameter	Min	Max		
$\overline{HOLD}$ setup time	t_{SH}	5		t_{HS}	10		ns	This timing is higher for SPI F-RAM. You should evaluate and adjust this parameter accordingly when migrating to SPI F-RAM.
$\overline{HOLD}$ time	t_{HH}	5		t_{HH}	10		ns	
$\overline{HOLD}$ LOW to HI-Z	t_{HHZ}		15	t_{HZ}		20	ns	
$\overline{HOLD}$ HIGH to data active	t_{HLZ}		15	t_{LZ}		20	ns	

Table 8. Power Parameter Comparison

Parameter Description	SPI nvSRAM			SPI F-RAM			Units	Comments
	Parameter	Min	Max	Parameter	Min	Max		
Power-up RECALL duration	t_{FA}		20	t_{PU}		1	ms	No impact when migrating to SPI F-RAM. System can optimize firmware to improve system performance.
STORE cycle duration	t_{STORE}		8				ms	These are nvSRAM specific parameters and are not applicable to SPI F-RAM.
Time allowed to complete SRAM write cycle	t_{DELAY}		25				ms	
Low-voltage trigger level	V_{SWITCH} (3 V)		2.65				V	No impact when migrating to SPI F-RAM. System can optimize firmware to improve system performance.
	V_{SWITCH} (5 V)		4.4				V	
V_{CC} rise time	$t_{VCCRISE}$	150		Not specified			µs	This spec is indirectly associated with the SPI F-RAM t_{VR} spec.
V_{DD} power-up ramp rate	Not specified			t_{VR}		50	µs/V	SPI nvSRAM does not impose any restriction on the V_{CC} ramp rate.
V_{DD} power-down ramp rate				t_{VF}		100	µs/V	When migrating to SPI F-RAM, you must ensure that the SPI F-RAM V_{DD} power ramp rate is within its specified limit.
Last access ($\overline{CS}$ HIGH) to power down V_{DD} (min)				t_{PD}		0	µs/V	No impact when migrating to SPI F-RAM
Time for nvSRAM to wake up from sleep mode	t_{WAKE}		20	t_{REC} (t_{RDP})		0.45	ms	No impact when migrating to SPI F-RAM. System can optimize firmware to improve system performance.
Time to enter sleep mode after issuing SLEEP instruction	t_{SLEEP}		8	NA			ms	SPI F-RAM enters sleep as soon as $\overline{CS}$ toggles LOW to HIGH after the SLEEP command is entered.
Time to enter standby mode after $\overline{CS}$ going HIGH	t_{SB}		100	Not specified			µs	No impact when migrating to SPI F-RAM

Figure 5. SPI nvSRAM Power Cycle Timing

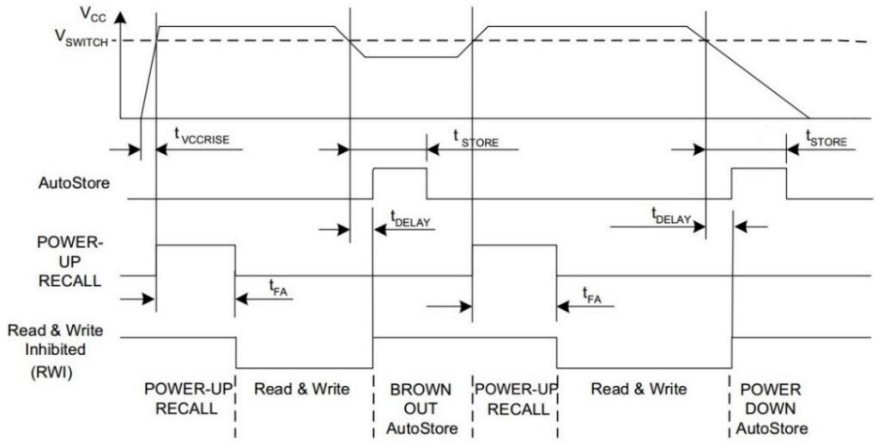
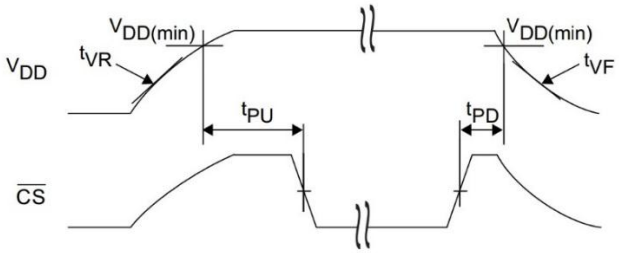


Figure 6. SPI F-RAM Power Cycle Timing



3 Hardware Compatibility

SPI nvSRAMs support two pin configurations for the 8-pin SOIC and 8-pin DFN packages, as shown in Figure 7 and Figure 8 .

3.1 SPI nvSRAM with $\overline{WP}$ (CY14xxxxQ1 and CY14xxxxQ1A) Pin Layout

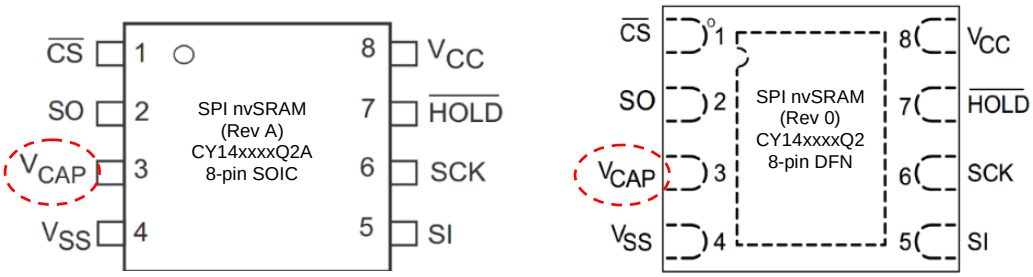
The two SPI nvSRAM package pin layouts shown in Figure 7 are identical to the SPI F-RAM pin layout. The SPI F-RAM pin layout shown in Figure 9 is a pin-for-pin drop-in replacement when migrating from SPI nvSRAM to SPI F-RAM.

Figure 7. SPI nvSRAM with $\overline{WP}$ (CY14xxxxQ1 and CY14xxxxQ1A)

3.2 SPI nvSRAM with V_{CAP} (AutoStore) (CY14xxxxQ2 and CY14xxxxQ2A) Pin Layout

The two SPI nvSRAM package pin layouts shown in Figure 8 are identical to the SPI F-RAM pin layout (except for the V_{CAP} pin). The SPI F-RAM pin layout is shown in Figure 9.

Figure 8. SPI nvSRAM with AutoStore (CY14xxxxQ1 and CY14xxxxQ1A)



It will be a pin-for-pin drop-in replacement (except for the V_{CAP} pin) when migrating from SPI nvSRAM to SPI F-RAM. The V_{CAP} pin on the SPI nvSRAM package is the hardware write protect ($\overline{WP}$) pin for SPI F-RAM. The $\overline{WP}$ pin is an input pin and is not biased internally; therefore, this pin remains floating when not connected on the PCB. When migrating to SPI F-RAM on the same footprint, you must ensure that the $\overline{WP}$ pin is properly biased for a successful operation. When the $\overline{WP}$ is biased at logic HIGH, it enables the Status Register write. When the $\overline{WP}$ pin is biased at logic LOW, it disables the Status Register write (write protect) when the WPEN bit in the Status Register is also set to '1'.

3.3 SPI F-RAM Pin Layout

The SPI F-RAM provides only one pin layout option for both the 8-pin SOIC and 8-pin DFN packages, as shown in Figure 9.

Figure 9. SPI F-RAM Pin Layout

The 8-pin SOIC package footprint for SPI F-RAM is identical to that of SPI nvSRAM. Therefore, migrating to SPI F-RAM does not require the package PCB footprint to change.

The 8-pin DFN package dimension for the SPI F-RAM can vary from that of the SPI nvSRAM 8-pin DFN as discussed in the Package Compatibility section. Therefore, migrating from the SPI nvSRAM 8-pin DFN to the SPI F-RAM 8-pin DFN is not always a drop-in replacement and will require the PCB layout to change if the package dimensions are different.

Note: Replacing SPI nvSRAM with the V_{CAP} option will require the hardware schematic and layout to be updated to either connect the controller I/O to control the $\overline{WP}$ pin of SPI F-RAM or connect an external pull-up on $\overline{WP}$ to keep the pin HIGH to disable the write protect if not used.

4 Firmware Compatibility

The SPI host controller firmware for SPI nvSRAM access will work as is for SPI F-RAM except for the nvSRAM special features. The nvSRAM special features such as AutoStore, AutoStore Enable, AutoStore Disable, software STORE, and software RECALL are not applicable to SPI F-RAM. In nvSRAM, data is first written to SRAM and then transferred to nonvolatile cells during AutoStore or software STORE. In F-RAM, data is nonvolatile instantaneously; hence, these features are not relevant.

4.1 Sleep Mode (SLEEP) Command

On the lower density SPI F-RAMs (64 Kb and below), the standby current is equivalent or lower than the sleep mode current (sleep mode current (I_{ZZ}) of SPI) of SPI nvSRAM. Hence, the sleep mode is not provided in the lower density SPI F-RAM devices. The sleep mode is offered in the 128-Kb and above density SPI F-RAMs, and the sleep mode (SLEEP) command execution is similar to that of the SPI nvSRAM SLEEP command. However, the sleep mode entry timing and wake timing differ between the two, as shown in Figure 10 and Figure 11.

Figure 10. SPI nvSRAM SLEEP Command

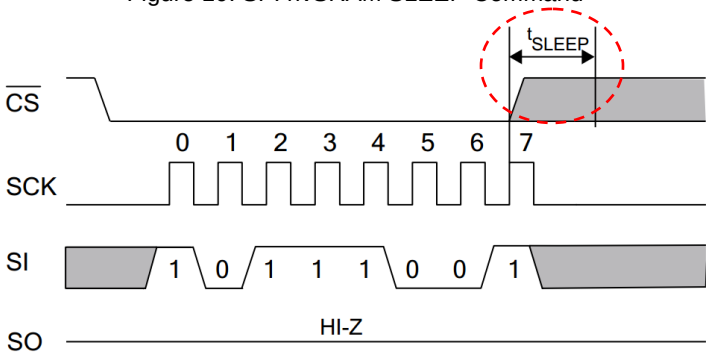
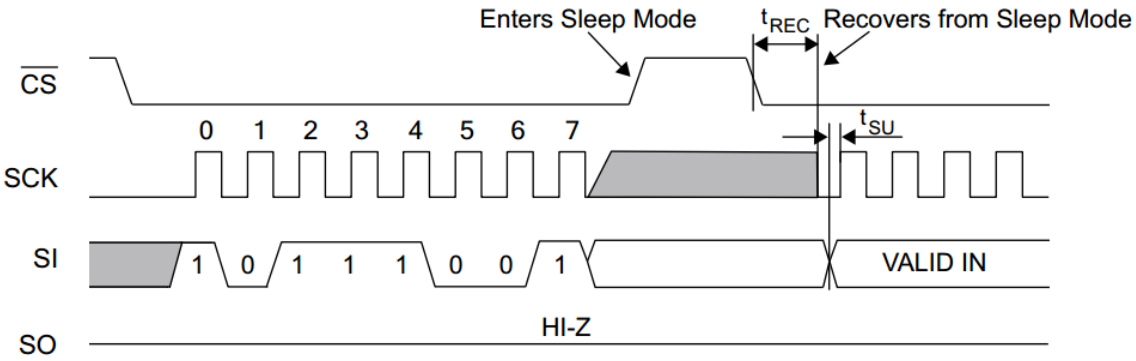


Figure 11. SPI F-RAM SLEEP Command



Notes:

- SPI nvSRAM takes about 8 ms (t_{SLEEP}, max) after the SLEEP command is registered to enter sleep. SPI F-RAM enters sleep at the $\overline{CS}$ rising edge. The 8-ms t_{SLEEP} wait time is not required in SPI F-RAM. This can be an improvement when migrating from SPI nvSRAM to SPI F-RAM.
- SPI nvSRAM takes about 20 ms (t_{WAKE}, max) to wake up from sleep after $\overline{CS}$ is toggled LOW. SPI F-RAM takes about 450 µs (t_{REC}, max) to wake up from sleep after $\overline{CS}$ is toggled LOW. The SPI F-RAM wakeup performance is superior to that of SPI nvSRAM, and this can be an improvement when migrating from SPI nvSRAM to SPI F-RAM.

4.2 Read Device ID (RDID) Command

The read Device ID feature is not available in all SPI F-RAMs with 64 Kb and lower densities. These devices will ignore the read device ID (RDID) command like any other unsupported SPI commands. All SPI F-RAMs with 128 Kb and above densities support the read Device ID command similar to the SPI nvSRAM. However, the RDID output differs between the two devices. The SPI nvSRAM returns a 4-byte ID, while SPI F-RAM returns a 9-byte ID. When migrating from SPI nvSRAM to SPI F-RAM, the firmware needs to be updated to read the 9-byte ID from SPI F-RAM. Refer to Figure 12 and Figure 13 for details.

Figure 12. Read Device ID in SPI nvSRAM

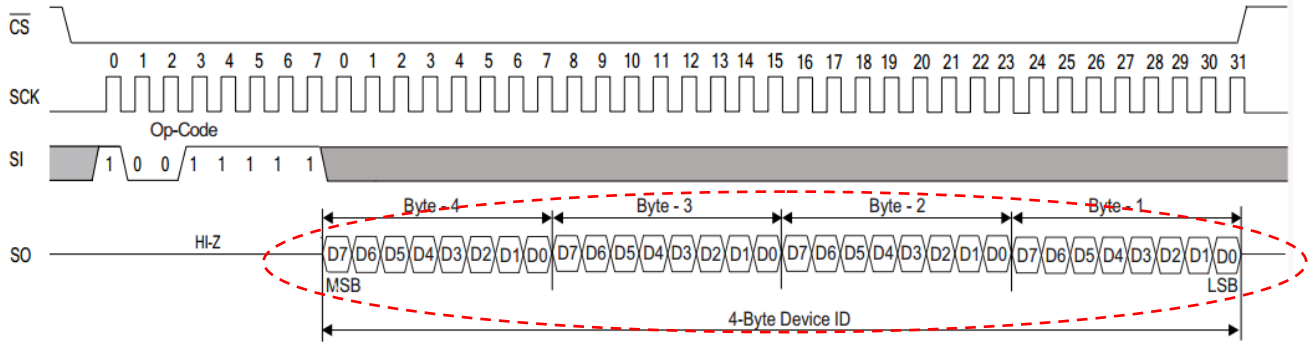
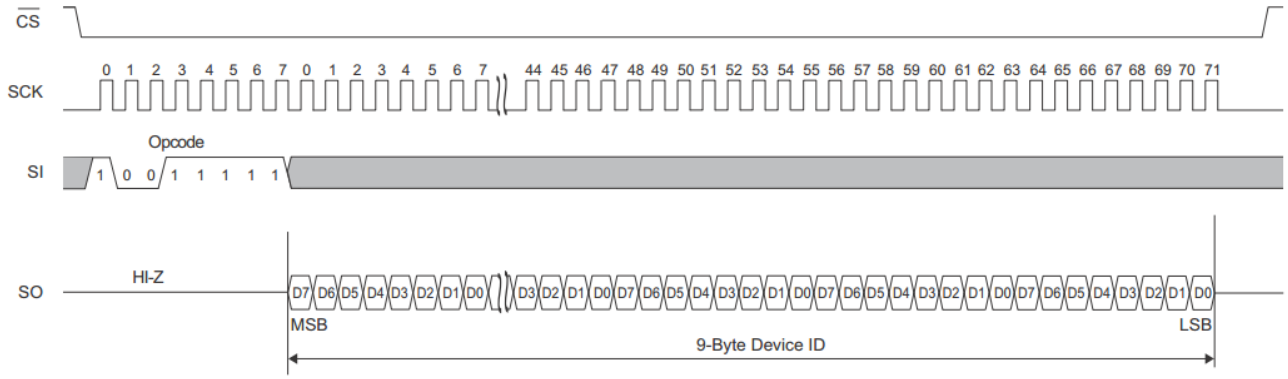


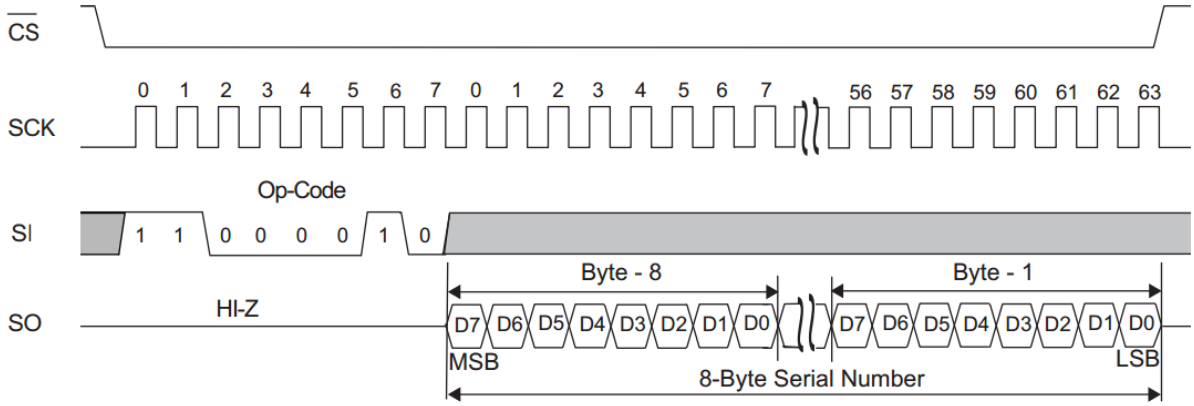
Figure 13. Read Device ID in SPI F-RAM



4.3 Read Serial Number (RDSN, SNR) Command

The read serial number (SNR) feature is available only in the 1-Mb, 3-V SPI F-RAM (FM25VN10). The other F-RAMs will ignore the read SNR command like any other unsupported SPI commands. The serial number in nvSRAM is user writeable with the write serial number (WRSN) command, but in SPI F-RAM, it is a factory-programmed read-only number. The instruction to read the serial number is identical between the two, as shown in Figure 14. Migrating from SPI nvSRAM to SPI F-RAM does not require any firmware change.

Figure 14. Read Serial Number (SPI nvSRAM and SPI F-RAM)



4.4 nvSRAM Special Features

The firmware for SPI nvSRAM may contain extra logic due to nvSRAM-specific features such as AutoStore, software STORE, software RECALL, AutoStore Enable, and AutoStore Disable. This extra logic can be removed when migrating to SPI F-RAM.

4.4.1 AutoStore

AutoStore is a unique feature of nvSRAM that automatically stores SRAM data to SONOS cells during power down. This STORE uses an external capacitor (V_{CAP}) and enables the device to safely STORE the data in the nonvolatile memory when power goes down. When migrating to SPI F-RAM, the capacitor on the V_{CAP} pin is replaced by the $\overline{WP}$ pin of the SPI F-RAM. No firmware update is required when migrating to SPI F-RAM.

4.4.2 Software STORE

Software STORE is a unique feature of nvSRAM to trigger a STORE operation through a special SPI instruction. The nonvolatile STORE operation is initiated by executing a STORE instruction. This feature is used when nvSRAM AutoStore is disabled through a special ASDISB command and the system uses the Software STORE command to save SRAM data to nonvolatile memory on demand. The system using this nvSRAM special feature cannot migrate to SPI F-RAM. However, a majority of applications use the nvSRAM AutoStore feature for data logging.

4.4.3 Software RECALL

Software RECALL is a unique feature of nvSRAM that allows you to initiate a RECALL operation to restore the content of nonvolatile memory to the SRAM. This is done by issuing a RECALL instruction. This feature is used in applications in which the possibility of soft errors is high, and systems use RECALL to overwrite the affected SRAM content with good data. Since SPI F-RAM soft error rate (SER) performance is superior to that of SPI nvSRAM, migrating to SPI F-RAM can achieve the same SER performance without requiring any firmware change. SPI F-RAM will ignore the software RECALL command.

4.4.4 AutoStore Enable and AutoStore Disable

AutoStore Enable (ASENB) and AutoStore Disable (ASDISB) are SPI commands to enable and disable the AutoStore operation in SPI nvSRAM. Since SPI F-RAM does not support the AutoStore feature, these two commands are don't care commands for the SPI F-RAM and will be ignored. Migrating from SPI nvSRAM to SPI F-RAM does not require any firmware change for these two features.

5 Summary

This application note discussed the options for migrating from SPI nvSRAM to SPI F-RAM devices. A few differences between the two devices in terms of package parameters, features, opcodes, and electrical parameters need to be considered when migrating. The majority of designs that use the specified SPI nvSRAM devices, however, can migrate to SPI F-RAM with a few hardware and software changes.

Document History

Document Title: AN202493 - Migrating from SPI nvSRAM to SPI F-RAM™

Document Number: 002-02493

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5054662	ZSK	12/18/2015	New application note.
*A	5850792	HARA	08/17/2017	Updated logo and copyright.

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Videos | Blogs | Training | Components

Technical Support

cypress.com/support

PSoC is a registered trademark and F-RAM is a trademark of Cypress Semiconductor Corporation.

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709