Migration from GL-P and GL-S to GL-T Flash

About this document

Scope and purpose

This application note outlines the differences and potential issues when migrating from the Infineon GL-P and GL-S to the GL-T flash family. It discusses affected device features, timing parameters as well as packages.

Intended audience

This is intended for users who plan to use GL-T flash family as a repleacement for the GL-P and GL-S flash.

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1 Introduction

Infineon continues to extend the MirrorBit™ GL family of 3V NOR flash with the introduction of the GL-T parallel NOR family based on 45 nm process technology. Infineon developed the GL-T flash family with migration in mind and most existing applications developed for GL-P and GL-S flash can also use GL-T flash. This document outlines the product differences that require attention in order to migrate to GL-T flash.

2 GL-P, GL-S, and GL-T Flash Feature Comparison

Table 1 provides an overview of the features of the GL-P, GL-S, and GL-T flash families. The 45 nm MirrorBit GL-T flash supports several features that were available with older flash families such as the GL-P but have been dropped with GL-S flash. In addition, GL-T flash maintains basic hardware and software compatibility to allow use on existing designs which use GL-P and/or GL-S flash. The feature differences are discussed in more detail in 3 Feature Difference Discussion on page 5.

The differences in Power-On-Reset (POR) timing are discussed in 4 Power On and Warm Reset Timing on page 13.

The differences in DC and AC specifications are detailed in 5 DC and AC Parameter Differences on page 15.

The differences in footprint and packaging are discussed in 6 Packaging on page 17.

Table 1 GL Family Feature Comparison

Family	S29GL-P 90 nm	S29GL-S 65 nm	S29GL-T 45 nm	Migration Issues
Density				
128 Mbit	√	√	–	Yes
256 Mbit	√	√	–	Yes
512 Mbit	√	√	√	No
1024 Mbit	√	√	√	No
2048 Mbit	√ (multi-die)	√ (multi-die)	√ (multi-die)	No
Sector Architecture				
Uniform 128 kB	√	√	√	No
Access				
x16 Data Bus Width	√	√	√	No
x8 Data Bus Width	√	–	√	No
Asynchronous	√	√	√	No
Read Page Mode	√	√	√	No
Read Page Size	16 Byte	32 Byte	32 Byte	No
Write Buffer Size	64 Byte	512 Byte	512 Byte	No
Security				
Individual Sector Write Protection	√	√	√	No
Secure Silicon OTP Area	256 Byte	2 x 512 Byte	4 x 512 Byte	Maybe
Other				
12V Accelerated Programming	√	–	√	No
Unlock Bypass Command	√	–	√	No
Multi-Sector Erase	√	–	√	No
Blank Check	–	√	√	No
Continuity Check	–	–	√	No
High Voltage Autoselect Access	√	–	–	Maybe
CFI Version	1.3	1.5	1.3 / 1.5	No
Status via Data Polling	√	√	√	No

GL-P, GL-S, and GL-T Flash Feature Comparison

Family	S29GL-P 90 nm	S29GL-S 65 nm	S29GL-T 45 nm	Migration Issues
Status via Status Register	–	√	√	No
Packaging and Ordering Options				
56-pin TSOP	√	√	√	No
64-ball BGA 10 x 13 mm (FAA064)	√	–	–	Yes
64-ball BGA 11 x 13 mm (LAA064)	√	√	√	No
64-ball BGA 9 x 9 mm (LAE064)	–	√	√	No
56-ball BGA 9 x 7 mm (VBU056)	–	–	√	No
SnPb Solder Option (RoHS 5/6)	√	√	–	Maybe

3 Feature Difference Discussion

3.1 Density

The S29GL-T flash is available in monolithic 512 and 1024 Mbit densities only. In addition, the multi-die S70GL-T flash is available in 2048 Mbit density. Only these densities can be migrated.

3.2 Sector Architecture

The GL-T flash has a 128 kB uniform sector architecture, identical to that in the GL-P and GL-S flash.

3.3 Data Bus Width

The GL-T flash supports both a x16 and a x8 Data Bus Width, i.e. it is compatible with all previous generations, including the GL-S flash that only supports x16 mode. The BYTE# input signal, pin 53 on 56-TSOP and ball F7 on 64-BGA, determines which mode is being used. GL-T flash has an internal pull-up so it is also compatible with GL-S applications that do not drive the BYTE# signal.

3.4 Read Page Buffer Size

Like GL-S flash, GL-T includes a 32 byte (16 word) read page buffer which is double the size of the GL-P flash to facilitate larger processor cache line fill operations. No software modifications are required to operate with 16 byte maximum read page transfers supported by the GL-P flash.

Software can be modified to take advantage of the larger GL-T read page buffer by querying the CFI page mode register at CFI word offset 4Ch and configuring software to perform additional page mode read cycles.

3.5 Write Buffer Size

The GL-T flash has a 512 byte (256 word) write buffer, same as GL-S flash and eight times the size of the GL-P flash. The larger write buffer facilitates higher programming throughput and better data alignment with most file systems. No software modifications are required to operate with a 64 byte maximum write buffer fill supported by the GL-P flash.

Software can be modified to take advantage of the larger GL-T write buffer by querying the CFI programming buffer size register at CFI word offset 2Ah and configuring software to perform large write buffer fills. It is recommended that GL-T buffer writes be performed on multiples of 32-byte pages to maximize data integrity. For the Industrial Plus version (-40°C to +105°C) of GL-T flash this is mandatory. For example, load the write buffer with one to sixteen 32-byte pages of data that will be programmed into the array in a single operation.

3.6 High Voltage Accelerated Programming

The GL-T flash does support accelerated programming, same as the GL-P flash, when V_{HH} (nominally 12V) is applied to the WP#/ACC input. No modifications are needed for existing designs based on GL-S flash which does not support this feature.

3.7 Autoselect Register Access

The Autoselect Register provides manufacturer and device identification through special identifier codes.

GL-T and GL-S flash only support Autoselect Register access via the Autoselect command (now called the ID Entry command), unlike the GL-P flash, which supports Autoselect Register access via the Autoselect command

as well as a high voltage method which requires VID (nominally 12V) applied to Address input A9. If an existing design is enabled to support Autoselect Register access via the high voltage method, it must be modified.

In the GL-P flash, the Autoselect Register is overlaid onto Sector Address zero (SA00). In the GL-S and GL-T flash, the Autoselect Register is overlaid onto whichever sector is selected with the Autoselect Entry command. SW modification is not required to access the GL-T flash Autoselect Register in existing GL-P and GL-S designs.

Sector Lock Status can be determined by accessing Autoselect Register word offset 02h within the desired sector. In GL-P flash, the lock protection status of multiple sectors can be determined after entering Autoselect mode at the flash base address. On GL-T and GL-S flash, only the protection status of the sector selected in the Autoselect entry command can be determined. To determine the lock protection status of a different sector, Autoselect mode has to be exited and reentered using the desired sector in the Autoselect Entry command.

3.8 Device ID

The monolithic 512 Mbit and 1024 Mbit GL-T flash devices have the same Device ID register values as the corresponding GL-P and GL-S parts. The S70GL02GT flash has the same Device ID as the S70GL02GP and S70GL02GS parts.

Table 2 GL Flash Device IDs

Description	Address	Read Data
Device ID word 1	(SA) + 0001h	227Eh
Device ID word 2	(SA) + 000Eh	2248h = 2 Gbit 2228h = 1 Gbit 2223h = 512 Mbit
Device ID word 3	(SA) + 000Fh	2201h

Existing software which supports the GL-P or GL-S flash and uses Device IDs to set up software command support does not require modification to enable compatibility with the GL-T flash. Use of specific CFI Register queries should be employed to take advantage of new GL-T features. The CFI Process Generation bits at CFI word offset 45h provide for in-system determination of the unique GL family, e.g. GL-P: 0014h, GL-S: 001Ch, GL-T: 0024h.

Device ID can only be accessed via software Autoselect Register commands on the GL-T flash and not via the optional high voltage method supported on the GL-P flash. See Autoselect Register Access on page 4.

3.9 Unlock Bypass

Unlock Bypass mode programming is a legacy feature used to decrease the command cycle overhead by 50% when performing programming with the single byte/word Program command. Applications using high density GL devices rely on multi-word write buffer programming to maximize programming throughput. Write buffer programming has an inherently low effective command overhead and supports single byte/word programming as well.

The GL-T flash supports Unlock Bypass mode programming, like the GL-P flash. No modifications are needed for existing designs based on GL-S flash which does not support this feature.

3.10 Multi-Sector Erase

Multi-sector erase is a legacy feature that allows queueing of multiple sector erase operations within one command string to minimize command overhead.

Feature Difference Discussion

The GL-T flash supports multi-sector erase operations, like the GL-P flash. No modifications are needed for existing designs based on GL-S flash which does not support this feature.

3.11 Secure Silicon OTP Area

S29GL-T flash devices have 2048 bytes of one time programmable (OTP) memory. This Secure Silicon Region (SSR) is divided into four areas, the lower 512B region, SSR0, is Factory modifiable and the upper three 512B regions, SSR1 - SSR3, are Customer modifiable. SSR0 can be ordered Factory pre-programmed. SSR0 is Factory locked and cannot be Customer modified. The Secure Silicon Region can only be accessed after writing the Secure Silicon Entry command and is mapped into the lower 1 kB of the sector selected during the entry command. SSR0 is overlaid onto word offset 0x0000 to 0x00FF of the selected sector. SSR1 is overlaid onto word offset 0x0100 to 0x01FF of the selected sector, SSR2 onto word offset 0x0200 to 0x02FF and SSR3 onto word offset 0x0300 to 0x03FF. Memory outside of the 2 kB Secure Silicon Region has undefined data when in Secure Silicon access mode.

Similarly, S29GL-S flash devices have 1024 bytes of one time programmable (OTP) memory. This memory is divided into two 512B regions, SSR0 and SSR1 with same functionality as GL-T flash.

The GL-P flash has 256B of OTP in the Secure Silicon Sector region. This region can be ordered Factory preprogrammed and locked, or it can be programmed and locked by the user. The region can only be accessed in Secure Silicon Access mode and is overlaid onto word 0x0000 to 0x007F of SA0. Also the Secure Silicon Lock Register bit usage is different from GL-T and GL-S. The GL-T Lock Register bit 0 is Factory programmed to 0 to indicate SSR Region 0 was Factory locked. The GL-T Lock Register bits 6, 9 and 10 are Factory preset to 1 to indicate SSR1-SSR3 are unlocked and that they can be programmed to 0 by the Customer to lock the SSRs. The GL-P Lock Register bit 0 is by default preset to 1 to indicate the Secure Silicon Region is unlocked. It can be Factory set to 0 if Factory preprogramming is ordered or can be programmed to 0 by the Customer to lock the Secure Silicon Region.

The S70GL02GT flash effectively has two 2 kB OTP areas, one in each GL01GT die. Access to the upper region requires flash input A26 = 1 during the Secure Silicon Register Access command cycles.

3.12 Individual Sector Write Protection

The GL-T flash supports the Advanced Sector Protection (ASP) feature that provides software enabled program and erase protection on a sector basis utilizing a user configurable 8-byte password as well as non-volatile and volatile control, consistent with the GL-S and GL-P flash.

3.13 Data Polling

GL-T flash supports legacy data polling to determine the status of embedded programming and erase operations. The implementation is consistent with the GL-S and GL-P flash and no software modification is required to continue using data polling routines when migrating to the GL-T flash.

If a DQ5 time out event occurs on GL-T flash, a software reset command is required to clear DQ5 and to return the flash to a ready state. It can take 100 ns for the GL-T flash to stop communicating that it is busy following this reset command. For GL-S flash this parameter was 2 µs.

Note that data polling may not be supported on future smaller process MirrorBit GL flash families. Status Register reads will be required to determine the status of embedded program and erase operations if data polling is not supported.

3.14 Status Register

The GL-T flash supports Status Register reads as an alternative method to Data Polling for determination of embedded operation status. The Status Register feature is supported on the GL-S flash as well but not on the GL-P flash.

The 16-bit Status Register is accessed via a two cycle sequence consisting of a Read Status Register Command write cycle followed immediately by a read cycle to the same targeted sector address. Using the Status Register is advantageous because, unlike legacy data polling, software does not need to track active address regions or compare sequential polling read values to determine embedded algorithm status; one Status Register access provides all the information necessary to determine the flash state. A Clear Status Register command is available to reset the last completed embedded operation portion of the Status Register.

Status Register usage is optional and existing designs utilizing GL-P flash do not have to accommodate this feature. If desired, software can be modified to take advantage of this feature by querying the Lower Software Bits at offset 000Ch in Autoselect mode. If bit 0 is set, Status Register functionality is supported.

Full details of the Status Register implementation are provided in the GL-T flash datasheet. The Status Register bit definitions are provided in **Table 3**.

Table 3 Status Register Bit Definition

Status Register Bit	Description	Name	Reset Value	Busy Status	Ready Status
15:8	Reserved		x	Invalid	x
7	Device Ready Bit	DRB	1	0	1
6	Erase Suspend Status Bit	ESSB	0	Invalid	0: No Erase In Suspension 1: Erase In Suspension
5	Erase Status Bit	ESB	0	Invalid	0: Erase Successful 1: Erase Failed
4	Program Status Bit	PSB	0	Invalid	0: Program Successful 1: Program Failed
3	Write Buffer Abort Status Bit	WBASB	0	Invalid	0: Program Not Aborted 1: Program Aborted During Write Buffer Command
2	Program Suspend Status Bit	PSSB	0	Invalid	0: No Program In Suspension 1: Program In Suspension
1	Sector Lock Status Bit	SLSB	0	Invalid	0: Sector Not Locked During Operation 1: Sector Locked Error Operation
0	Continuity Check	CC	0	Invalid	0: Continuity Check Pattern not detected 1: Continuity Check Pattern detected

Note:

1. *Bits 15 thru 8 are reserved for future use and may display as 0 or 1. These bits should be ignored (masked) when checking status.*
2. *Bit 7 is 1 when there is no Embedded Algorithm in progress in the device.*
3. *Bits 6 thru 0 are valid only if bit 7 is 1.*
4. *All bits are put in their reset status by cold reset or warm reset.*
5. *Bits 5, 4, 3, and 1 are cleared to 0 by the Clear Status Register command or Reset command.*
6. *Upon issuing the Erase Suspend Command, the user must continue to read status until DRB becomes 1.*
7. *ESSB is cleared to 0 by the Erase Resume Command.*
8. *ESB reflects success or failure of the most recent erase operation.*
9. *PSB reflects success or failure of the most recent program operation.*
10. *During erase suspend, programming to the suspended sector will cause program failure and set the Program status bit to 1.*
11. *Upon issuing the Program Suspend Command, the user must continue to read status until DRB becomes 1.*
12. *PSSB is cleared to 0 by the Program Resume Command.*
13. *SLSB indicates that a program or erase operation failed because the sector was locked.*
14. *SLSB reflects the status of the most recent program or erase operation.*

3.15 Blank Check

The GL-T flash supports a sector Blank Check feature that enables system software to minimize latency associated with erasures prior to code updates, like the GL-S flash. Use of this feature is optional and is not supported on GL-P flash. The new Blank Check feature has no effect on existing designs. Please refer to the GL-T data sheet for Blank Check feature implementation details.

3.16 Continuity Check

The Continuity Check feature is introduced with the GL-T flash. It provides a basic test of connectivity from package connectors to each die pad and to each individual die in a multi-die package. Use of this feature is optional and is not supported on GL-S and GL-P flash. It has no effect on existing designs. See the GL-T data sheet for implementation details.

3.17 CFI Register

Table 4 provides a listing of all the Common Flash Interface (CFI) register values that are different for the GL-T, GL-S, and GL-P flash families. Software can access the CFI register to determine device specific features such as array size, command set, page size and programming time and use these values to self-configure for optimal performance.

GL-S flash supports the CFI version 1.5, which is an extended address range revision of the legacy CFI version 1.3 supported by the GL-P flash. GL-T flash has an order option to support either the CFI version 1.3 or CFI version 1.5 for maximum backward compatibility. The only difference is the Minor Version Number value at offset 44h as well as the values at and above offset 51h which are invalid for CFI version 1.3.

Migrations from GL-P Flash should order GL-T parts with CFI 1.5 if possible; order GL-T parts with CFI 1.3 if required for use with old drivers (for example, Linux 2.6) which are unable to be patched and rebuilt.

Feature Difference Discussion

Table 4 CFI Register Differences

CFI Register	Word Offset	GL-P	GL-S	GL-T
Typical timeout for single word write = 2^N µs	1Fh	0006h	0008h	0008h
Typical timeout for individual block erase = 2^N ms	21h	0009h	0008h	000Ah
Typical timeout for full chip erase = 2^N ms 0000h = Not Supported	22h	0013h (1 Gb) 0012h (512 Mb) 0011h (256 Mb) 0010h (128 Mb)	0012h (1 Gb) 0011h (512 Mb) 0010h (256 Mb) 000Fh (128 Mb)	0014h (1 Gb) 0013h (512 Mb)
Maximum timeout for single word = 2^N times typical	23h	0003h	0001h	0002h (85°C) 0003h (105°C)
Maximum timeout for maximum multi-byte program = 2^N times typical	24h	0005h	0002h	0001h (85°C) 0002 (105°C)
Maximum timeout for individual block erase = 2^N times typical	25h	0003h	0003h	0002h
Maximum timeout for full chip erase = 2^N times typical 0000h = Not Supported	26h	0002h	0003h	0002h
Flash Device Interface Description 0000h = x8-only, 0001h = x16-only, 0002h = x8/x16-capable	28h	0002h	0001h	0002h
Maximum number of bytes in multi-byte write = 2^N	2Ah	0006h	0009h	0009h
Minor version number, ASCII	44h	0033h	0035h	0033h / 0035h
Process Technology (Bits 5-2): 0101b = 90 nm MirrorBit, 0111b = 65 nm MirrorBit Eclipse, 1001b = 45 nm MirrorBit, Address Sensitive Unlock (Bits 1-0): 00b = Required, 01b = Not Required	45h	0014h	001Ch	0024h
Page Mode Type 0002h = 8-word Page, 0003h = 16-word Page	4Ch	0002h	0003h	0003h
ACC (Acceleration) Supply Minimum 0000h = Not Supported, D[7:4] = V, D[3:0] = 100 mV	4Dh	00B5h	0000h	00B5h
ACC (Acceleration) Supply Maximum 0000h = Not Supported, D[7:4] = V, D[3:0] = 100 mV	4Eh	00C5h	0000h	00C5h
Unlock Bypass 0000h = Not Supported, 0001h = Supported	51h	–	0000h	- / 0001h

Feature Difference Discussion

CFI Register	Word Offset	GL-P	GL-S	GL-T
Secure Silicon Sector (Customer OTP Area) Size = 2^N bytes	52h	–	0009h	- / 0009h
Software Features	53h	–	008Fh	- / 008Fh
Read Page Size = 2^N bytes	54h	–	0005h	- / 0005h
Erase Suspend Timeout Maximum < 2^N µs	55h	–	0006h	- / 0006h
Program Suspend Timeout Maximum < 2^N µs	56h	–	0006h	- / 0006h
Embedded Hardware Reset Timeout Maximum < 2^N µs	78h	–	0006h	- / 0006h
Non-embedded Hardware Reset Timeout Maximum < 2^N µs	79h	–	0009h	- / 0009h

3.18 Lock Register Differences

There are some changes to the Lock Register for GL-T flash, see **Table 5**.

- The DQ11..DQ9 Lock Bits are new on GL-T flash. They are 'Reserved' and factory preset to 1 on GL-S and GL-P flash.
- The DQ8 'Reserved' bit is factory set to 0 on both GL-T and GL-S flash. It is factory preset to 1 on GL-P flash. The DQ7 'Reserved' bit is factory set to either 0 or 1 on GL-S flash. This bit is factory preset to 1 on GL-T and GL-P flash.
- The DQ6 (SSR1 Lock Bit) is factory set to 1 and can be customer set to 0 to permanently write protect the 512 byte SSR1 region, on GL-T and GL-S flash. This bit is 'Reserved' and factory preset to 1 on GL-P flash.
- The DQ0 (SSR0 [Factory] Lock Bit) is preset at the factory to 0 to permanently write protect the 512 byte SSR0 region, on GL-T and GL-S flash. On GL-P flash, this bit enables locking of the Secure Silicon Region by either the Factory or Customer. If the Secure Silicon Region is Factory preprogrammed, this bit is 0, which indicates the Secure Silicon Region is locked, otherwise it is Factory preset to 1 and can be set to 0 by the Customer to lock the Secure Silicon Region.

Note: The Customer is not required to program all bits at the same time. This allows the Customer to lock the SSRs before or after the device protection scheme has been selected. When programming the Lock Register, all 'Reserved' bits should be written as 1 (masked).

Table 5 Lock Register Differences

Lock Register	GL-P Flash		GL-S Flash		GL-T Flash	
Bit	**Definition**	**Default**	**Definition**	**Default**	**Definition**	**Default**
DQ[15:12]	Reserved	1111b	Reserved	1111b	Reserved	1111b
DQ11	Reserved	1b	Reserved	1b	SSR3 Password Mode Lock Bit	1b
DQ10	Reserved	1b	Reserved	1b	SSR3 Lock Bit	1b
DQ9	Reserved	1b	Reserved	1b	SSR2 Lock Bit	1b
DQ8	Reserved	1b	Reserved	0b	Reserved	0b

Feature Difference Discussion

Lock Register	GL-P Flash		GL-S Flash		GL-T Flash	
Bit	**Definition**	**Default**	**Definition**	**Default**	**Definition**	**Default**
DQ7	Reserved	1b	Reserved	0b/1b	Reserved	1b
DQ6	Reserved	1b	SSR1 Lock Bit	1b	SSR1 Lock Bit	1b
DQ[5:3]	Reserved	111b	Reserved	111b	Reserved	111b
DQ2	Password Protection Mode Lock Bit	1b	Password Protection Mode Lock Bit	1b	Password Protection Mode Lock Bit	1b
DQ1	Persistent Protection Mode Lock Bit	1b	Persistent Protection Mode Lock Bit	1b	Persistent Protection Mode Lock Bit	1b
DQ0	Secure Silicon Sector Protection Bit	1b	SSR0 (Factory) Lock Bit	0b	SSR0 (Factory) Lock Bit	0b

4 Power On and Warm Reset Timing

At power on, the flash needs more time in the reset state to initialize than it does during a warm reset. **Table 6** and **Figure 1** and **Figure 2** detail the power on and warm reset timing requirements for the GL-T, GL-S, and GL-P flash.

Table 6 Power On and Warm Reset Timing Requirements

Parameter	Description	Type	GL-P	GL-S	GL-T
Power on Reset					
t_{VCS}	V_{CC} Setup Time to first access	min	35 µs	300 µs	300 µs
t_{VIOS}	V_{IO} Setup Time to first access	min	35 µs	300 µs	300 µs
t_{RPH}	RESET# Low to CE# Low	min	35 µs	35 µs	35 µs
t_{RP}	RESET# Low to RESET# High	min	35 µs	200 ns (2)	200 ns (2)
t_{RH}	RESET# High to CE# Low	min	200 ns	50 ns (2)	50 ns (2)
t_{CEH}	CE# High to CE# Low	min	N/A	20 ns	20 ns
Warm Reset					
t_{RPH}	RESET# Low to CE# Low	min	35 µs	35 µs	35 µs
t_{RP}	RESET# Low to RESET# High	min	35 µs	200 ns (2)	200 ns (2)
t_{RH}	RESET# High to CE# Low	min	200 ns	50 ns (2)	50 ns (2)
t_{CEH}	CE# High to CE# Low	min	N/A	20 ns	20 ns

Note:

1. *N/A = Not Applicable.*
2. *For GL-S and GL-T, t_{RP} + t_{RH} must not be less than t_{RPH}.*

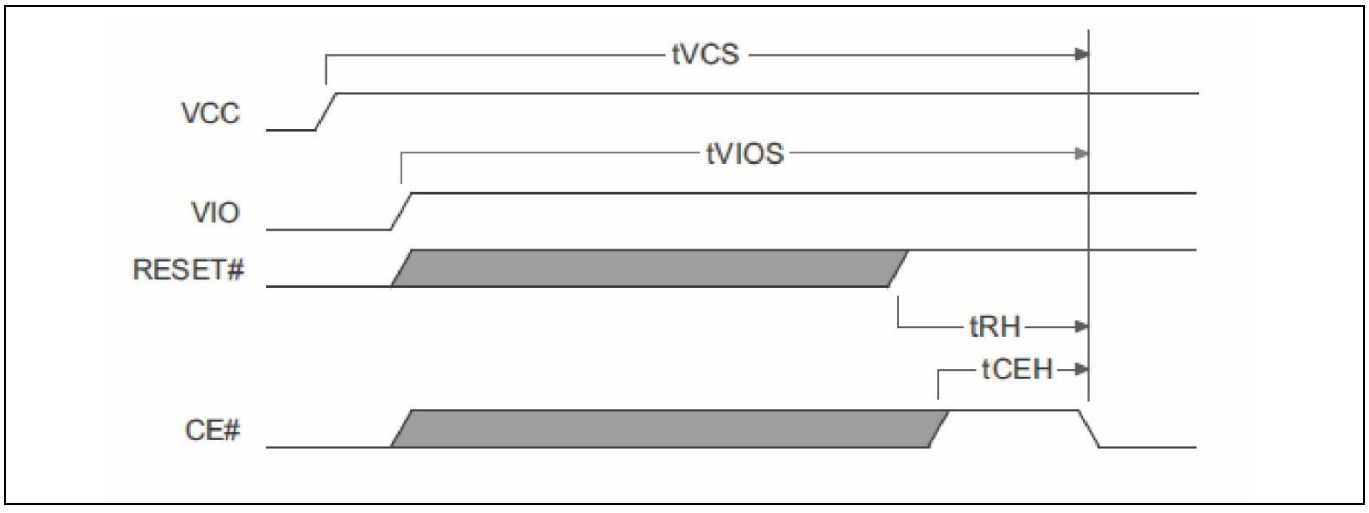

Figure 1 Power-Up Reset Timing

Note: The sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.

Power On and Warm Reset Timing

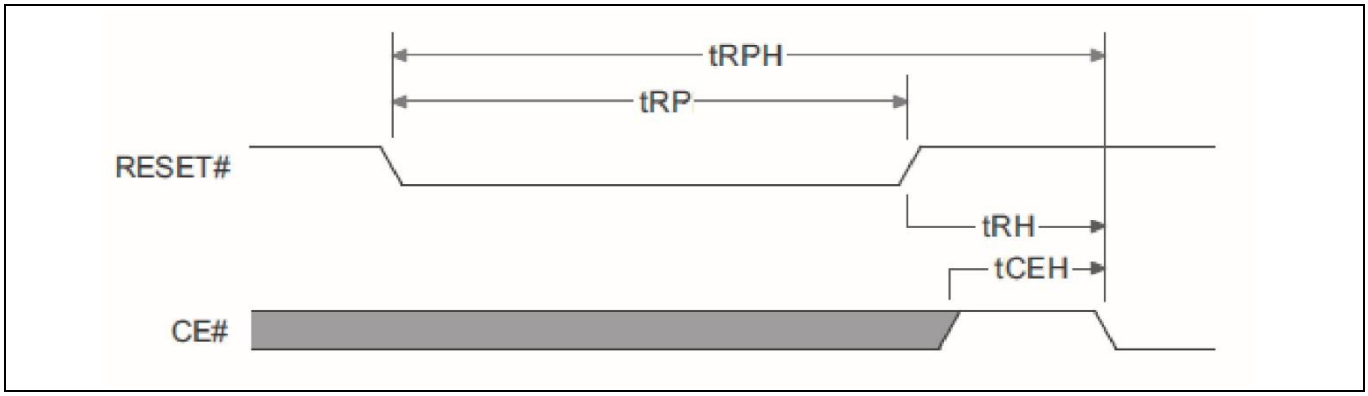

Figure 2 Warm Reset Timing

Note: The sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.

The differences in power-on timing should not present a migration challenge for most applications where the flash interfaces directly with a Host that requires oscillator and PLL lock prior to initiating the first boot read access to the flash. In applications which may access the flash within 300 µs of power application, some circuit modification is required to accommodate migration to GL-T flash.

To initiate the first read or write cycle after power on, GL-T and GL-S require CE# to transition from High to Low no sooner than tVCS after VCC exceeds VCC_min and VIO exceeds VIO_min. CE# must be High at least tCEH = 20 ns prior to CE# falling edge which initiates the first access. These were not requirements for GL-P so designs that have CE# fixed low cannot migrate to GL-T without modification to enable active CE# control.

CE# is ignored during Warm Reset; however, to initiate the first read or write cycle after warm reset, GL-T and GL-S require CE# to transition from High to Low no sooner than tRH after RESET# transitions from Low to High. CE# must be high at least tCEH = 20 ns prior to CE# falling edge, which initiates first access. These were not requirements for GL-P so designs that have CE# fixed low cannot migrate to GL-T without modification to enable active CE# control.

The GL-T flash allows VIO to ramp concurrently with or after VCC with no restriction on time or voltage differential. During power ramp no input is allowed to exceed VIO. The GL-T and GL-S data sheets provide enhanced direction on power management and control to design a robust and reliable system. In general, this additional guidance in the GL-T data sheet also applies to GL-P flash.

5 DC and AC Parameter Differences

Table 7 provides a side by side reference of DC specification differences. The differences do not impact logic transition points or timing parameter specifications and should not cause migration issues.

Table 7 DC Specification Differences (-40°C to +85°C)

Parameter	Description	Type	S29GL-P	S29GL-S	S29GL-T
Input Levels					
V_{IO}	All I/O other than A9 and ACC	max	4.0V	4.0V	4.0V
V_{IO}	A9 and ACC	max	12.5V	4.0V	12.5V
Logic Levels					
V_{IL}	Input Low Voltage	max	0.3 * V_{IO}	0.2 * V_{IO}	0.3 * V_{IO}
V_{IH}	Input High Voltage	max	V_{IO} + 0.3V	V_{IO} + 0.4V	V_{IO} + 0.4V
Power Usage					
I_{CC1}	Active V_{CC} + V_{IO} Read (5 MHz)	max	55 mA	60 mA	60 mA
I_{CC2}	Active V_{CC} Intra-Page Read (33 MHz)	max	20 mA	25 mA	25 mA
I_{CC3}	Active Program or Erase	max	90 mA	100 mA	100 mA
I_{CC4}	Standby Current	max	5 µA	100 µA	100 µA
I_{CC5}	Reset Current	max	500 µA	20 mA	20 mA
I_{CC6}	Automatic Sleep Current	max	5 µA	150 µA	150 µA

Table 8 provides side by side comparisons of AC parameter specification differences between the GL families (minus reset timing parameter differences documented in Table 6). All parameters should be reviewed against actual application implementations to ensure a successful migration. For applications that use the erase suspend and/or program suspend features, it is important to review the system software ramifications of the GL-T having longer latency than the GL-P between issuance of the suspend and resume commands and the flash updating status and completing the transition between modes.

Table 8 AC Specification Differences

Parameter	Description	Type	GL-P (1)	GL-S (1)	GL-T (1)
Async Read					
t_{ACC} / t_{CE} / t_{RC}	Read Cycle Time	min	100 ns	100 ns	100 ns
t_{PACC}	Intra-Page Access Time	min	25 ns	15 ns	15 ns
t_{DF}	Control negate to data High-Z	min	20 ns	15 ns	15 ns
Async Write					
t_{WC}	Write Cycle Time	min	100 ns	60 ns	60 ns
t_{WP}	WE# Enable to Disable	min	35 ns	25 ns	25 ns
t_{WPH}	WE# Disable to Enable	min	30 ns	20 ns	20 ns
t_{DS}	Data Setup to WE# Disable	min	30 ns	30 ns	30 ns
t_{BUSY}	Erase/Program Valid to RY/BY# Delay	max	90 ns	80 ns	80 ns
Suspend Resume					
t_{ESL}	Erase Suspend / Erase Resume	max	20 µs	40 µs	40 µs
t_{PSL}	Program Suspend / Program Resume	max	15 µs	40 µs	40 µs

DC and AC Parameter Differences

Parameter	Description	Type	GL-P (1)	GL-S (1)	GL-T (1)
Array Update					
	Full Buffer Write Program Time (2)	typ	480 µs	340 µs	451 µs
	Effective per Word Write Buffer Program Time	typ	15 µs	1.33 µs	1.76 µs
	Single Word Program Time	typ	60 µs	125 µs	160 µs
	128 kB Sector Erase Time	typ	500 ms (4)	275 ms	535 ms
	Sector Erase Timeout	max	50 µs	0 s	50 µs
Throughput					
	x16 Async Read	max	20 MB/s	20 MB/s	20 MB/s
	x16 Page Mode Read (3)	max	58 MB/s	98 MB/s	98 MB/s
	Programming	typ	133 kB/s	1.5 MB/s	1.14 MB/s
	Erase	typ	262 kB/s (4)	477 kB/s	245 kB/s

Note:

1. *All table specifications apply to I-temp rated 512 Mbit density devices with VCC = VIO = 2.7-3.6V (-40°C to +85°C). Refer to individual data sheets for performance specifications for other densities and operating conditions.*
2. *Maximum Write Buffer Size varies: GL-P = 64B, GL-S = GL-T = 512B.*
3. *Page mode read throughput based on 8 word page accesses for GL-P and 16 word page accesses for GL-S and GL-T.*
4. *Excluding pre-programming to 0x00 prior to erasure*

6 Packaging

Standard S29GL-T flash is available in one 56-lead leadframe package (TSO056), two 64-ball BGA packages (LAA064, LAE064) and one 56-ball BGA package (VBU056), Pb-free only. The electrical contact dimensions and footprints are compatible with the GL-P and GL-S flash.

The outer dimensions of the LAE064 package are 9 x 9 mm, forty three percent smaller than the 11 x 13 mm LAA064 package. Printed Circuit Board (PCB) layout changes are not required to utilize the LAE064 package on existing LAA064 designs; however, surface mount placement programs require modification for proper part placement. The VBU056 package is a new option that is not available for GL-P and GL-S flash.

The S70GL02GT flash is available in the same 64-ball LAA064 ball grid array package as the S70GL02GP and S70GL02GS flash.

Some connection definitions have changed, see **Table 9**.

Table 9 Pin Out Differences

Pin or Ball	GL-P	GL-S	GL-T	Migration Issue
TSOP Package				
16	WP#/ACC	WP#	WP#/ACC	No
27	NC	RFU	RFU	No
28	NC	DNU	RFU	No
30	NC	RFU	RFU	No
51	DQ15/A-1	DQ15	DQ15/A-1	No
53	BYTE#	RFU	BYTE#	No
55	NC/A25 (1)	NC/A25 (1)	NC/A25 (1)	No
LAA/LAE Package				
B1	NC/A26 (2)	NC/A26 (2)	NC/A26 (2)	No
B4	WP#/ACC	WP#	WP#/ACC	No
E1	NC	DNU	RFU	No
F7	BYTE#	RFU	BYTE#	No
G1	NC	RFU	RFU	No
G7	DQ15/A-1	DQ15	DQ15/A-1	No
G8	NC/A25 (1)	NC/A25 (1)	NC/A25 (1)	No

Legend:

NC = Not Connected internally (okay to use pad for routing).

RFU = Reserved for Future Use (not connected internally on current product).

DNU = Do Not Use (must be left floating, not okay to use pad for routing).

Note:

1. *A25 only for S29GL01G and S70GL02G versions.*
2. *A26 only for S70GL02G.*

Packaging

The WP#/ACC connection on GL-T and GL-P flash is the WP# input on GL-S flash. The ACC feature is not supported on GL-S. This input difference does not cause migration issues.

Similarly, the DQ15/A-1 connection on GL-T and GL-P flash is the DQ15 input/output on GL-S flash (which only supports x8 Data Bus Width). The BYTE# input on GL-T and GL-P flash is electrically isolated and labeled RFU on GL-S flash. This input difference does not cause migration issues.

7 Appendix A: Patch for Older Linux Kernels

This patch fixes a situation with older 2.6.x Linux kernels where flash devices with CFI version 1.5 do not get detected.

```
diff -rupN linux-2.6.12/drivers/mtd/chips/cfi_util.c linux-2.6.12-
cfi15/drivers/mtd/chips/cfi_util.c
--- linux-2.6.12/drivers/mtd/chips/cfi_util.c     2005-06-17 21:48:29.000000000 +0200
+++ linux-2.6.12-cfi15/drivers/mtd/chips/cfi_util.c      2012-01-10
10:54:09.618387020 +0100
@@ -71,7 +71,7 @@ __xipram cfi_read_pri(struct map_info *m
 #endif

        if (extp->MajorVersion != '1' ||
-           (extp->MinorVersion < '0' || extp->MinorVersion > '3')) {
+           (extp->MinorVersion < '0' || extp->MinorVersion > '5')) {
              printk(KERN_WARNING "  Unknown %s Extended Query "
                     "version %c.%c.\n",  name, extp->MajorVersion,
                     extp->MinorVersion);
```

Revision history

Document version	Date of release	Description of changes
**	2015-09-15	Initial release
*A	2017-05-02	Updated **Table 1** and **Table 4** Updated **3.17 CFI Register** Updated template
*B	2017-08-09	Updated **3.17 CFI Register** Added **Appendix A: Patch for Older Linux Kernels** Updated template
*C	2021-04-28	Updated to Infineon template

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