# CoolSiC™ 1200 V SiC MOSFET Application Note

## About this document

### Scope and purpose

The benefits of wide-bandgap silicon carbide (SiC) semiconductors arise from their higher breakthrough electric field, larger thermal conductivity, higher electron-saturation velocity and lower intrinsic carrier concentration compared to silicon (Si). Based on these SiC material advantages, SiC MOSFETs are becoming an attractive switching transistor for high-power applications, such as solar inverters and off-board electric vehicles (EV) chargers. This application note introduces the CoolSiC™ trench MOSFET, describing the SiC MOSFET's products, characteristics, gate-oxide reliability and application designs. This application note describes the CoolSiC™ MOSFET's general features and applications, which can help in designing power systems effectively using the novel transistor.

### Intended audience

This application note is intended for people who would like to get an introduction to CoolSiC™ 1200 V SiC MOSFET.

## Table of contents

# 1 Infineon 1200 V SiC Trench CoolSiC™ MOSFET

Silicon carbide (SiC) as a compound semiconductor material is formed by silicon (Si) and carbon (C). Currently, 4H–SiC is preferred for power devices primarily because of its high carrier mobility, particularly in the vertical c-axis direction.

Table 1 summarizes the physical property differences between Si and SiC [1]. As a rule of thumb, SiC has ten times the electric breakthrough field, allowing for thinner epitaxial layers to support the high blocking voltage in power devices. As an example, a 4500 V power device would require only a 40 µm–50 µm drift layer, as opposed to almost 500 µm in the case of silicon. The thinner and more highly doped drift layer leads to much lower drift resistance, hence, to low forward voltage and low conduction loss, while maintaining high blocking voltage. Secondly, SiC thermal conductivity amounts to 3.7 W/cm/K allowing for efficient thermal management. With a high electric breakthrough field, SiC can be used especially for high-voltage unipolar devices such as MOSFETs and Schottky diodes, achieving low switching loss.

In today's power transistors, with the push to high power and high voltage, ordinary Si-based MOSFETs as a unipolar device are becoming less favorable due to increases in on-state losses. Consequently, the Si IGBT as a bipolar device was typically the preferred choice for voltages exceeding approximately 1000 V. Moreover, the Si IGBT as a bipolar device has lower on-state losses than high voltage Si MOSFET. However, a major drawback is that high-speed operation is not possible due to the restricted dynamics of injected holes, resulting in significant switching loss by tail currents, for example. Alternatively, the larger critical electric field for breakdown of SiC allows a greatly reduced drift region resistance for the same breakdown voltage compared to the silicon-based part. Furthermore, SiC MOSFETs have the benefit of being unipolar devices, and thus enable faster switching than a Si IGBT, and better controllability of switching behavior. This makes the SiC MOSFET a very attractive device.

Infineon developed a truly "normally-off" SiC MOSFET using trench technology with the trade mark name CoolSiC™ MOSFET. The following chapters introduce this CoolSiC™ MOSFET describing its basic performance, benefits and application design guidelines.

**Table 1 Physical properties' comparison of basic semiconductor material** [1]

| Physical properties | 4H-SiC | Si |
|---|---|---|
| Band gap [eV] | 3.23 | 1.124 |
| Breakthrough field [MV/cm] | 2.5 | 0.25 |
| Thermal conductivity [W/cm/K] | 3.7 | 1.5 |
| Ideal bulk mobility [cm²/Vs] | 1000 | 1420 |
| Electron saturation vel. [cm/s] | $2x10^7$ | $1.05x10^7$ |

# 2 Characteristics of CoolSiC™ MOSFET

This chapter introduces the static and dynamic characteristic results of the CoolSiC™ MOSFET. The data in this chapter was acquired using the discrete 1200 V 45 mΩ device, and is valid for the part numbers IMW120R045M1 (TO-247 3pin) and IMZ120R045M1 (TO-247 4pin). The general behavior can be transferred to other packages or chips using the CoolSiC™ MOSFET technology. Some of the CoolSiC™ MOSFET products from chips, discrete units to modules are shown in Figure 1.Currently released power modules use the 45 mOhm chip as well, mostly by paralleling.


**Figure 1 Solutions using 1200 V CoolSiC™ MOSFET**

## 2.1 Static characterization

Static characterization includes blocking capability; output characteristics; $R_{ds(on)}$ vs. $T_j$; threshold voltage $V_{GS(th)}$; transfer characteristics; junction capacitance and body diode I-V characteristics.

### 2.1.1 Blocking capability

The leakage current $I_{DSS}$ of the CoolSiC™ MOSFET is measured with increasing temperature at a blocking voltage of 1200 V. This was done by shorting the gate and source terminals ($V_{GS}$=0 V), and thus the device is off. At a blocking voltage of 1200 V, the device's leakage current $I_{DSS}$ is typically at 2 µA at 25°C and 4 µA at 175°C.

### 2.1.2 Output characteristics

The I-V curves, or output characteristics, of each MOSFET are measured in pulse mode for different junction temperatures of 25°C and 175°C, respectively. Figure 2 (left) shows the drain current as a function of drain-source voltage $V_{DS}$ with different gate-source voltages $V_{GS}$. The solid black curves are typical results at 25°C and the red-dashed curves are those at the maximum junction temperature of 175°C. The device is designed for an on-state gate voltage of +15 V, which is common for Si IGBT. The typical on-resistance of the device is determined at $V_{GS}$=+15 V, and a rated current of $I_{DS}$=20 A. It amounts to $R_{DS(on)}$ =45 mΩ at $T_j$=25°C.

As the SiC MOSFET is a voltage-controlled device, it turns on step by step with increasing gate-source voltage. The higher gate voltage is above threshold level, the higher drain current is at specified drain voltage. The curves of Figure 2 are almost linear up to drain currents of about 30 A, if the gate source voltage is above 13 V. For higher drain currents or lower gate-source voltages, there is a significant curve steadily lowering the current slope with increasing $V_{DS}$. This behavior is a consequence of the built-in junction field effect transistor (JFET), which is formed by the deep p+ wells. As the p+ wells are linked to source, the junction channel of the JFET is controlled by a drain-source voltage drop. Hence, the JFET channel is narrowed down with increasing $V_{DS}$. This feature improves the short-circuit ruggedness by limiting the saturation current for very high drain voltages $V_{DS}$.

The temperature behavior of the I-V characteristic also depends on temperature. Exceeding 13 V of gate voltage, the drain current decreases with temperature, resulting in better paralleling performance of multiple devices . Below 13 V gate voltage, the drain current increases with temperature.It is not recommended to have $V_{GS}$ below +13 V for on-state. In general, the device could be driven with higher gate-source voltages than 15 V, which

further improves the on-state behavior. However, the lifetime of the gate oxide will be reduced, since gate-oxide stress is higher, thus accelerating the aging of the device. Consequently the failure rate is increased by using a higher gate-source voltage than 15 V. For on-state operating, Infineon recommends $V_{GS}$=+15 V of its CoolSiC™ MOSFET. The trade-off between long lifetime and low forward voltage $V_{DS}$ is well-balanced for this on-state operation voltage. For deviating operating conditions, please check with Infineon about the impact on the FIT rates.

### 2.1.3 On-state resistance $R_{DS(on)}$ vs. junction temperature $T_j$

The on-state resistance $R_{DS(on)}$ is shown in the below Figure 2 (right) as a function of junction temperature $T_j$ with drain-to-source current $I_{DS}$ as a parameter. At 20 A and 25°C, the typical value of $R_{DS(on)}$ is 45 mΩ with $V_{GS}$=+15 V.

The $R_{DS(on)}$ of CoolSiC™ MOSFET is mainly determined by the following factors: MOSFET's channel, the intrinsic JFET and the drift region in the device, which all depend on temperature. The MOSFET's channel has a negative temperature characteristic due to the behavior of the interface states, while the drift region and intrinsic JFET have positive temperature characteristics. Because of the advantageous channel orientation along the preferred crystal plane with a low density of interface defects, the total $R_{DS(on)}$ of CoolSiC™ MOSFET is not dominated by the MOSFET's channel resistance so that the total $R_{DS(on)}$ exhibits a positive temperature coeeficient in the complete temperature range . This behavior is beneficial for balancing the current distribution of parallel devices.

Moreover, with high temperature, the $R_{DS(on)}$ is increased to limit the highest saturation current, thus improving the short-circuit ruggedness of the device as well.

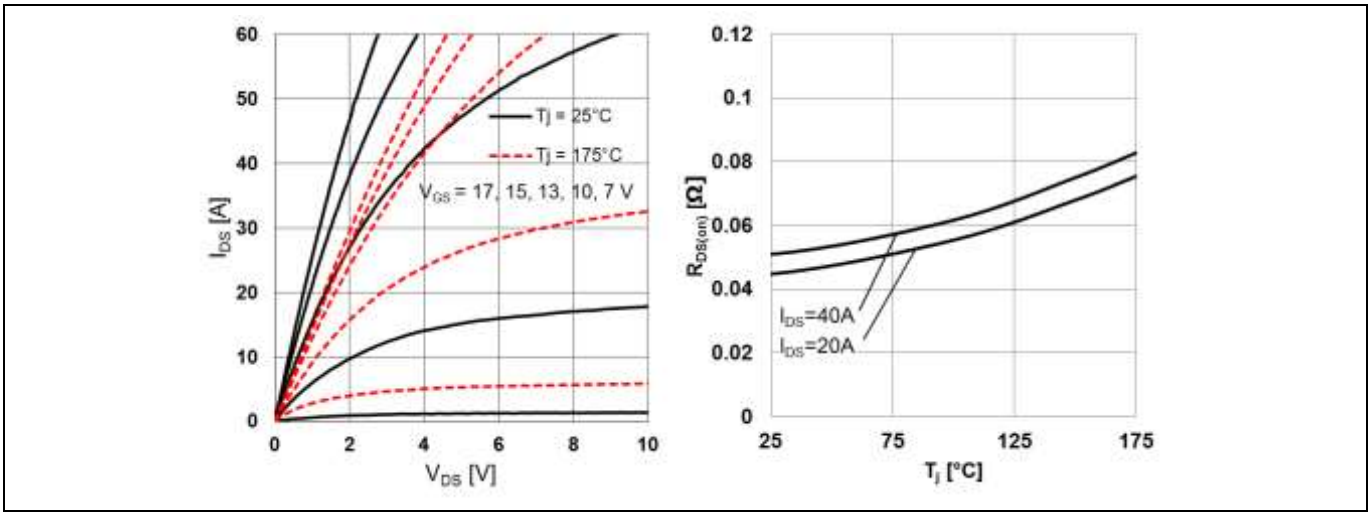



**Figure 2** **(Left) Typical output characteristics, $V_{GS}$ as parameter, with $T_j$=25°C and $T_j$=175°C; ( Right) Typical on-resistance vs. junction temperature, $I_{DS}$ as parameter ($V_{GS}$=15 V)**

### 2.1.4 Threshold voltage

The threshold voltage $V_{GS(th)}$ is the gate-source voltage needed for current to start flowing through the channel of the device at a specific drain to source current. The left side of Figure 3 shows the threshold voltage versus temperature at $I_{DS}$=10 mA. This threshold voltage $V_{GS(th)}$ is measured by first applying one 1 ms pulse-gate voltage at a $V_{GS}$=+20 V as a precondition [10], then the threshold-voltage value of $V_{GS(th)}$ is read at $V_{GS}$=$V_{DS}$ by forcing current $I_{DS}$=10 mA . From the results, the typical threshold voltage $V_{GS(th)}$ equals 4.5 V at 25°C and $I_{DS}$=10 mA, which provides good noise immunity against parasitic turn-on, meaning ease of use for the device.

Typically SiC MOSFETs have a short-channel effect resulting in a reduction of threshold voltage at higher drain voltages. The effect is called DIBL (drain-induced barrier lowering), already known from low-voltage Si power MOSFETs. For the CoolSiC™ MOSFET, the $V_{GS(th)}$ is reduced when blocking $V_{DS}$ voltage increases as shown on

the right side of Figure 3 with drain current $I_{DS}$ =10 mA. With DC voltage at normal maximum operating voltage of 1000 V, the $V_{GS(th)}$ of CoolSiC™ MOSFET is typically above 2 V at maximum junction temperature of 175°C.

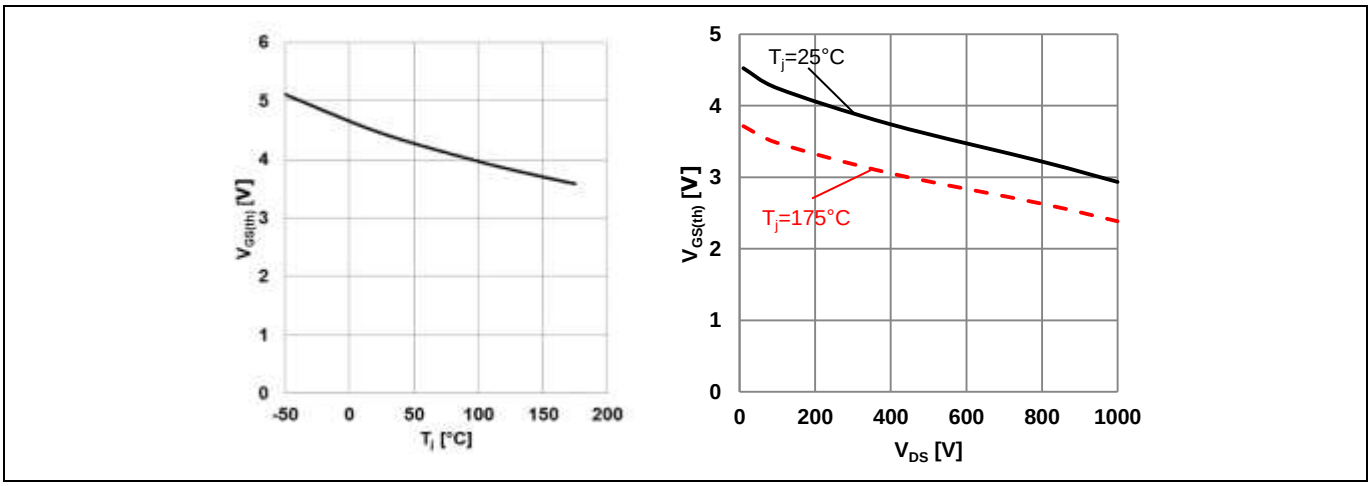



**Figure 3** **(left) Typical gate-source threshold voltage as a function of junction temperature ($I_{DS}$=10 mA, $V_{GS}$=$V_{DS}$); (right) Typical gate-source threshold voltage as a function of drain-source voltage ($I_{DS}$=10 mA)**

## 2.1.5 Transfer characteristics and small signal capacitance

The transfer characteristics of the CoolSiC™ MOSFET are obtained by measuring the drain current as the gate-source voltage was increased from 0V to $V_{gsmax}$ for a fixed drain-source voltage ($V_{DS}$=20 V), which is shown on the left side of Figure 4. The slope of the transfer curve is known as the transconductance $g_{fs}$ of the MOSFET. It indicates that there is a crossing point at $V_{GS}$=15 V. The temperature dependence decreases with increasing gate-source voltage, and above 15 V, the current decreases with temperature, which is beneficial in limiting the saturation current in the event of a short circuit.

The low signal capacitance of CoolSiC™ MOSFET is measured under increasing drain-source voltage to 1000 V at room temperature as showed on the right side of Figure 4. The device design is optimized to a favorably small ratio of the Miller capacitor $C_{rss}$ related to the gate-source capacitor $C_{gs.}$ This has been done to avoid to avoid the isssues related to bridge topology and parasitic turn-on from the Miller capacitor. Here, the capacitor $C_{iss}$ is the input capacitance with $C_{gs}$+$C_{gd}$, output capacitor $C_{oss}$ is equal to $C_{gd}$+$C_{ds}$, and $C_{rss}$ is the Miller capacitance, called reverse capacitance.

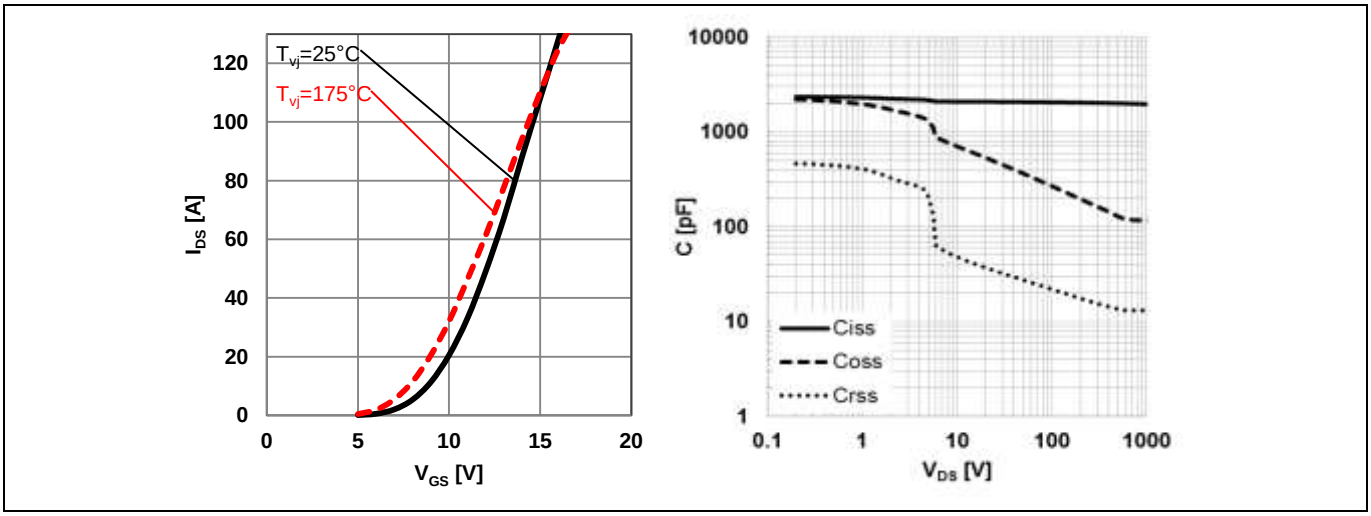



**Figure 4** **(left) Typical transfer characteristics ($V_{DS}$=20 V) ; (right)Typical capacitance as a function of drain-source voltage**

### 2.1.6 Third quadrant operating mode

Like other MOSFETs, the CoolSiC™ MOSFET also integrates an intrinsic body diode with p-n junction behavior. As shown in Figure 5, the intrinsic bipolar body diode has a relatively high forward voltage $V_{SD}$ (about4.1 V at 20 A) compared to silicon parts, if the gate voltage is between 0 V and -5 V. This is due to the wide bandgap characteristics of the silicon carbide material. The forward voltage $V_{SD}$ has a negative temperature coefficient as well as the standard Si p-n junction diode. So it is not effective to use the body diode to conduct current for long periods of time. Fortunately, unlike IGBTs, the SiC MOSFETs can conduct reverse current from source to drain through the channel if a positive bias is applied to the gate. This mode of operation is called synchronous rectification (or third quadrant operation) and achieved with a positive voltage of typically +15 V on the gate. As shown in the figure below, this synchronous rectification mode is highly recommended to limit conduction losses. Applying synchronous rectification has the additional benefit that positive temperature coefficient of $R_{dson}$ will support current sharing.

However, the body diode has to operate during dead-time operation when both high-side and low-side MOSFETs are turned off in bridge topologies, for example and to reduce the on-state conduction losses due to the body diode. Therefore it is necessary to design the dead-time period as short as possible (synchronous rectification mode). The value of dead time depends on the topology and the design circuit, for example, hard or soft switching, PCB layout, gate drive IC selection, etc. The time interval can range from one hundred nanoseconds to several hundred nanoseconds.

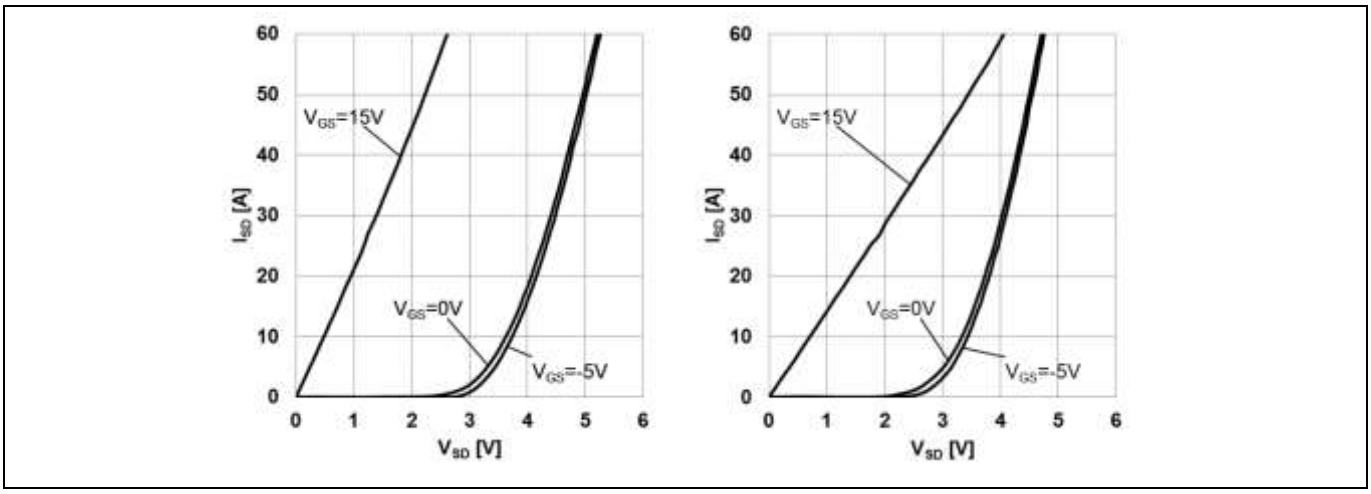



**Figure 5 Reverse current $I_{SD}$ as function of voltage at different gate voltages and temperature: $T_j$ =25°C (left), $T_j$=175°C (right)**

## 2.2 Dynamic characterization

The dynamic characterization includes switching characteristics, body-diode reverse-recovery charges, and short-circuit and gate charges.

### 2.2.1 Switching characteristics

The clamped double-pulse testing circuit is used to measure the switching losses for both TO-247 3pin and TO-247 4pin at 175°C as shown in Figure 6. The 20 A 1200 V G5 SiC Schottky diode with part number IDH20G120C5 is used as a high-side freewheeling diode. The external gate resistor $R_G$ is at 2 Ω and the $V_{GS}$ is at +15 V for turn-on and -5 V for turn-off. Both TO-247 3pin and TO-247 4pin show much lower switching losses compared to their Si counterpart. In addition, due to the ability of the TO-247 4pin package to separate the gate-source pin and power-source pin (Kelvin connection), the TO-247 4pin can also reduce $E_{on}$ by 40% and $E_{off}$ by around 10% at a drain current of 40 A. The higher the current to be switched, the bigger the benefit of the TO-247 4pin package

will be. For the hard-switching topology, it is recommended to use the TO-247 4pin package to reduce switching losses and ringing.

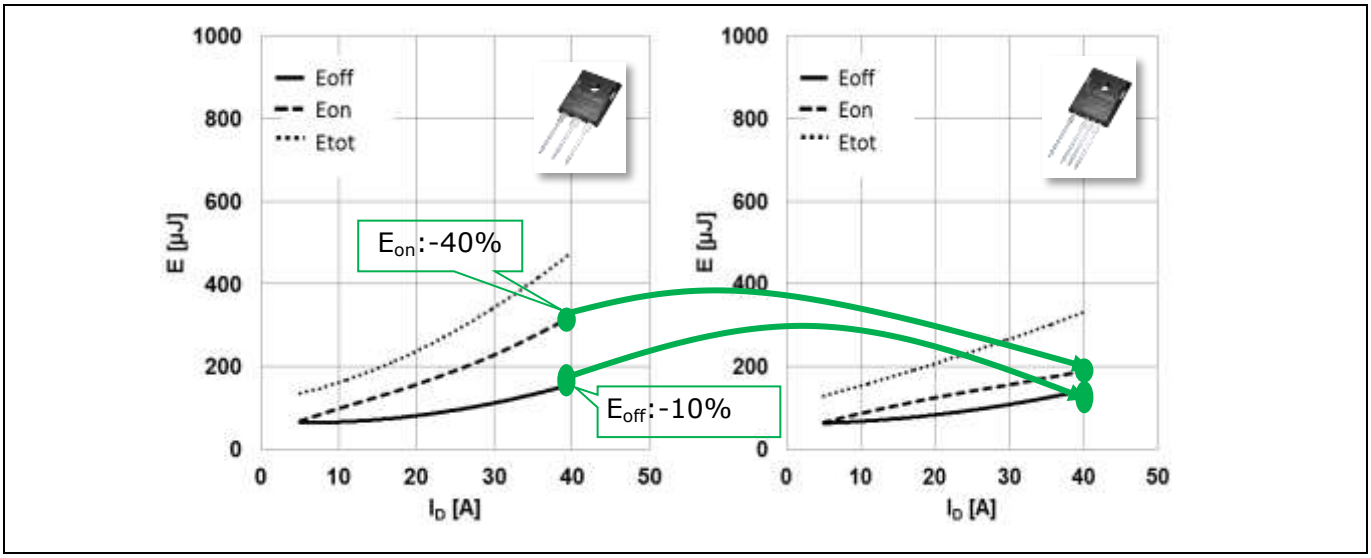



**Figure 6 Typical switching energy losses as a function of drain-source current with $T_j$=175°C; IMW120R045M1 (TO-247 3pin, left) and IMZ120R045M1 (TO-247 4pin, right)**

Figure 7 shows the typical turn-on and turn-off waveforms for the TO-247 3pin CoolSiC™ MOSFET IMW120R045M1 at 800 V DC and 175°C.The test is a double-pulse test using its own body diode as a freewheeling diode. It shows that theis SiC MOSFET has implemented the benefit of tuning the drain-source slew rate dv/dt and di/dt, which helps to mitigate spikes or ringing. It shows that the CoolSiC™ Mosfet provides good control of switching transients by the gate resistor value. With the external gate resistors varied from 4 Ω to 15 Ω, the drain-source slew rate dv/dt is decreased, however at the penalty of increased switching loss. When changing the external gate resistor from 4 Ω to 15 Ω, the ringing voltage on the drain source can be suppressed, and the gate-to-source voltage $V_{GS}$ ringing will be further reduced during turn-on and turn-off transients.

The slew rate dv/dt and switching losses are fully controllable by changing external gate resistor $R_G$,as shown in Figure 8. This proves the device has clear controllability by $R_G$ to trade-off slew rate dv/dt, and switching losses. Thhe higher $R_G$ leads to fewer EMI problems and low $R_G$ can reduce switching losses. Also, the gate-to-source $V_{GS}$ waveform is smooth during turn-on and off with different gate resistors due to a favorable ratio of the Miller capacitance $C_{rss}$ related to the gate-to-source capacitance $C_{gs}$.

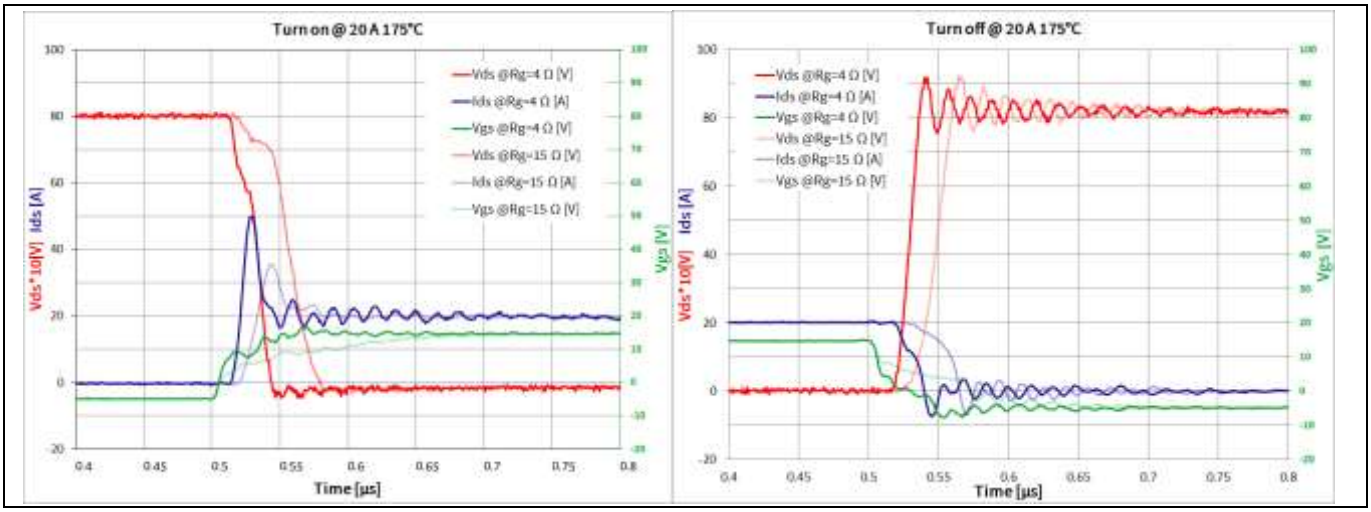



**Figure 7 Typical switching turn-on and turn-off waveforms for IMW120R045M1 (TO-247 3pin)**

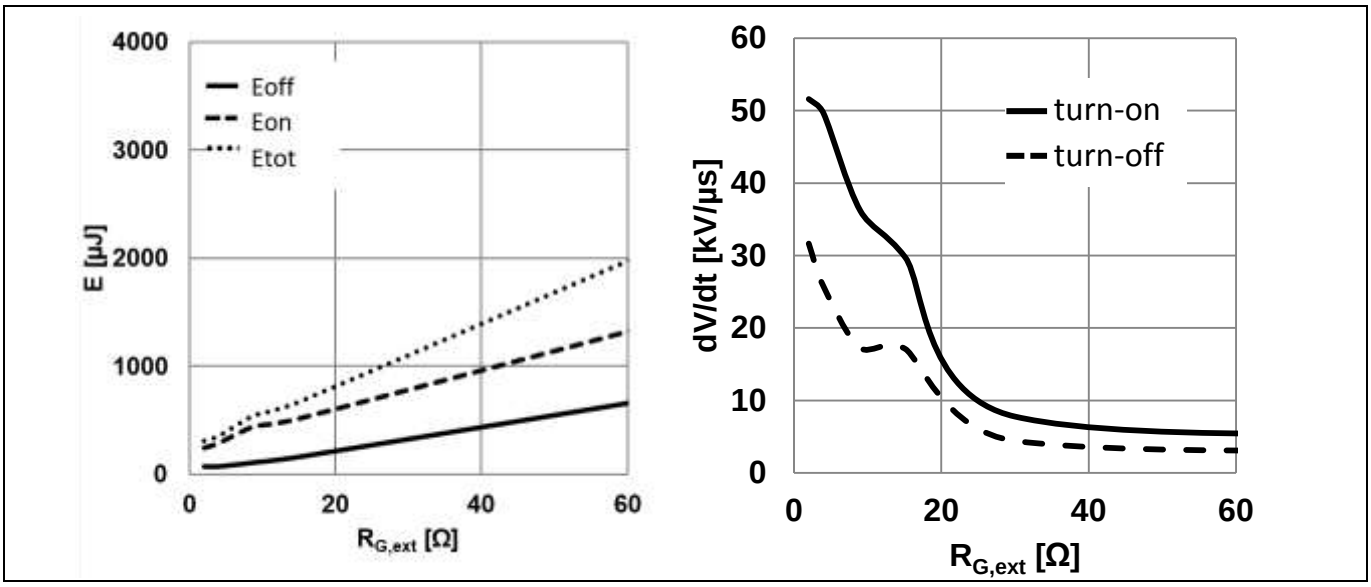



**Figure 8** **Typical switching energy losses (left) and maximum dv/dt values (right ) vs. external gate resistor $R_G$ at $V_{DS}$=800 V, $I_{Ds}$=40 A, $V_{GS}$ =+15/-5 V, 175°C, for IMW120R045M1 in half-bridge configuration**

## 2.2.2 Body-diode reverse recovery

The switching performance of the intrinsic body diode is measured with $Q_{rr}$ and $I_{rrm}$ at $V_{DS}$=800 V, $V_{GS}$=15/-5 V and $I_{DS}$=20 A. As illustrated in Figure 9, the reverse-recovery charge is temperature-dependent, unlike the SiC Schottky diode. The higher the temperature, the higher the reverse-recovery charge. This is an effect evidently caused by minority carriers injected by the forward-biased intrinsic pn-junction, which generates a reverse-recovery charge. Fortunately, the absolute values at the rated current are still fairly low, meaning the CoolSiC™ MOSFET has significantly lower, almost negligible, reverse-recovery losses.

The body diode $Q_{rr}$ is an important parameter for bridge topology with hard commutation. During the dead-time period of bridge topology, the body diode is freewheeling current before the corresponding transistor is turned on. When this transistor is turned on, the body diode reverse-recovery current will go through the corresponding transistor for a short period. With the low $Q_{rr}$ of CoolSiC™ MOSFET, it can minimize switching loss, and enables an increase in switching frequency.

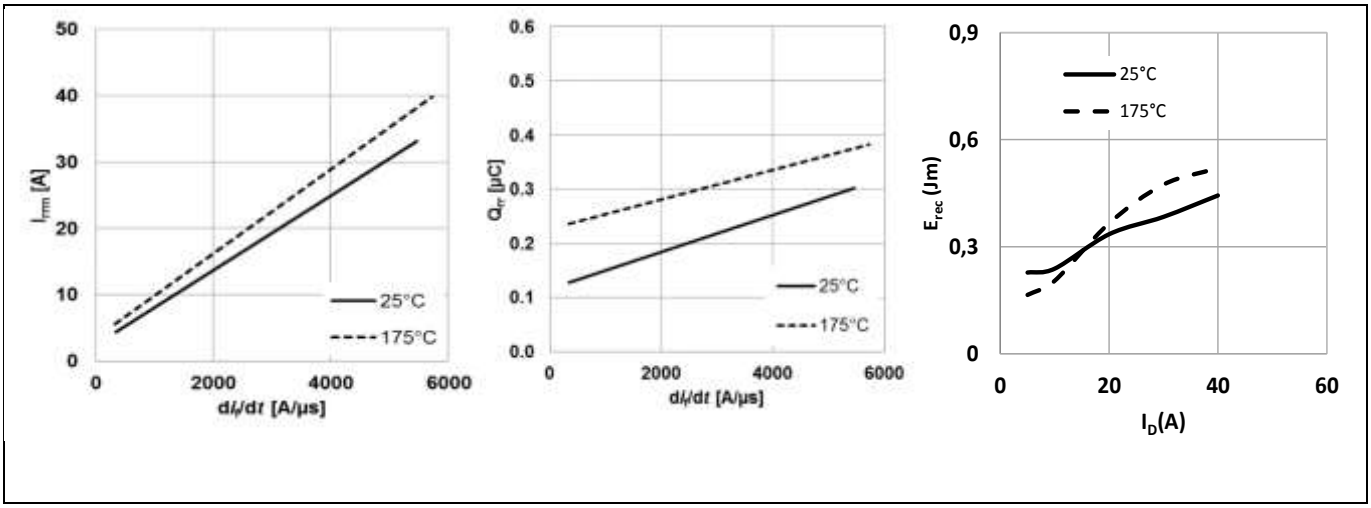



**Figure 9** **Typical reverse-recovery charge (left) and reverse-recovery current (middle and reverse-recovery energy (right) ) as a function of diode current slope for IMW120R045M1**

### 2.2.3 Short-circuit (SC) capability

Figure 10 depicts the short-circuit waveforms for the TO-247 4pin (IMZ120R045M1) and TO-247 3pin (IMW120R045M1) with $V_{GS}$=-5 V/+15 V and DC voltage $V_{DD}$=800 V. Initially, the drain current increases rapidly and reaches the peak current level. Because of fast turn-on with the Kelvin-source design, the TO-247 4pin current rises faster, and has less self-heating at the beginning of the SC event with high peak current exceeding 300 A, while the TO-247 3pin has a smaller peak current. The major reason is a negative feedback induced via the di/dt against the applied $V_{GS}$ in the case of the 3-pin device. Since this effect is eliminated in the solution with Kelvin connection, whichenables faster switching, the current can also rise to higher values for the 4-pin device before the saturation effect takes place.

After peak current, the drain current is significantly decreased, to about 150 A. This is due to the reduction in carrier mobility and JFET effect with temperature increase and self-heating. The test waveform shows clean, robust behavior, which proves the typical 2 µs SC capability (10x) for both packaged TO-247 CoolSiC™ MOSFET and power modules.

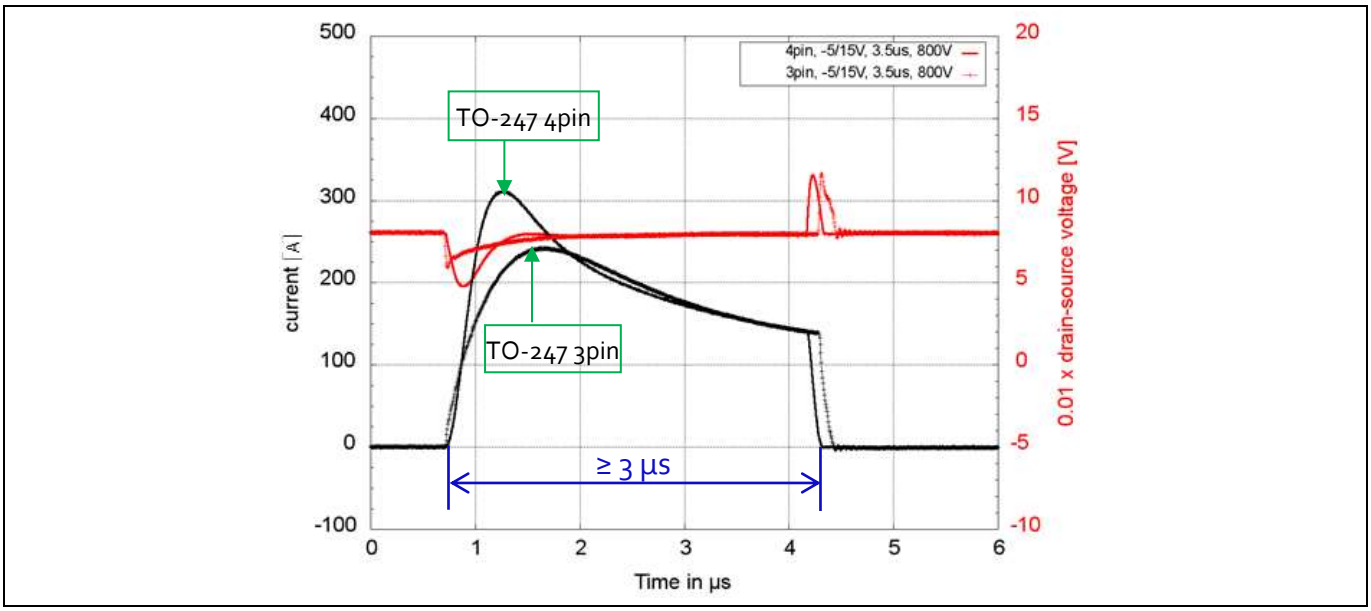



**Figure 10 Typical short circuit as a function of duration time at 25°C**

### 2.2.4 Gate charge

Figure 11 provides the gate-charge waveform at $I_{DS}$=20 A and $V_{DS}$=800 V with the $V_{DS}$ declining as a reference. The CoolSiC™ MOSFET's Miller plateau is a non-flat type with a "Miller ramp", which means the gate-source voltage of the MOSFET changes during the drain-source voltage fall and rise transitions instead of remaining constant. Since there is no a typical flat Miller plateau, the $Q_{GD}$ cannot simply be extracted by using the length of the plateau/ramp phase. During this ramp phase, the $C_{gs}$ is also charged ($V_{GS}$ rises)for the CoolSiC™ MOSFET. Therefore, to estimate a more practical $Q_{GD}$, the $V_{DS}$ waveform is overlayed to the $Q_G$ waveform, and $Q_{GD}$ is extracted between $V_{DS}$=97% to $V_{DS}$=10%. This also fits nicely to the integral of $C_{rss}$. Hence, the typical value of $Q_{GD}$ is 13 nC according to the above definition. The $Q_{GS,pl}$ is defined as the charge from the origin ($V_{GS}$=-5 V) to the start of the ramp, here the typical value of $Q_{GS,pl}$=23 nC, and the total gate charge $Q_G$ is still defined as the charge from the origin ($V_{GS}$=-5 V) to the point on the curve at which the driving voltage equals the actual gate to source voltage of the device ($V_{GS}$=15 V); here the typical value of $Q_G$=62 nC.

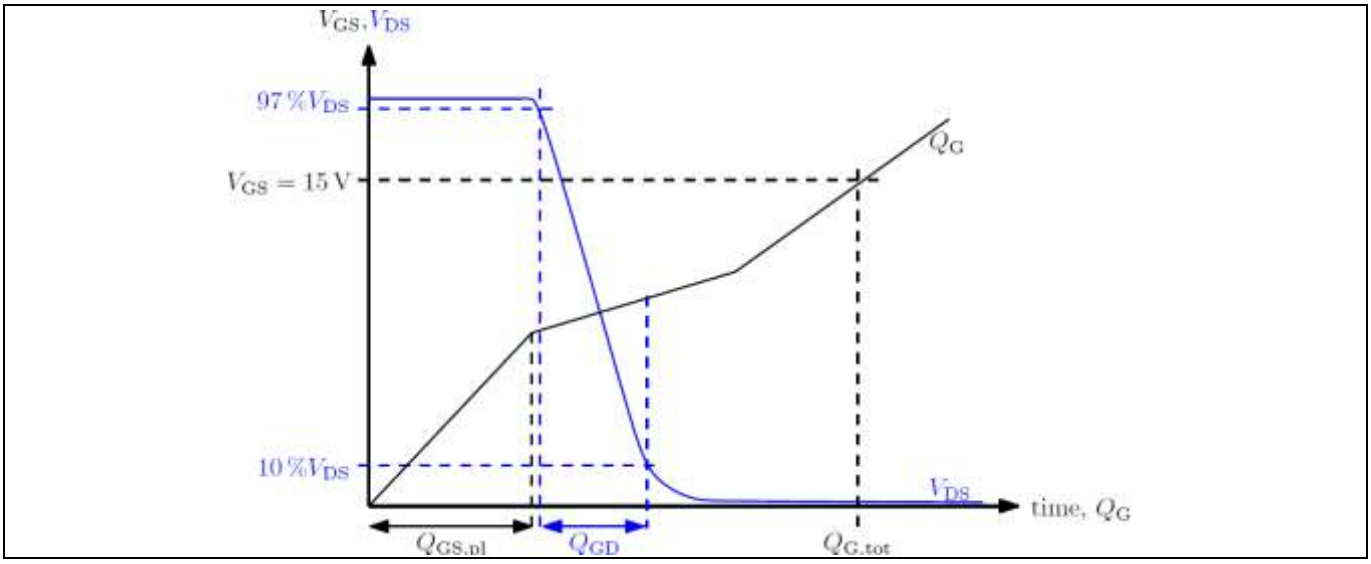



**Figure 11 Typical gate charge, $V_{GS}$ =f($Q_G$), $I_{DS}$=20 A,$V_{DS}$=800 V, turn-on pulse**

# 3 Driver design guideline

This chapter will introduce the gate- drive design considerations, and highlight design tips for paralleling discrete TO-247 4pin CoolSiC™ MOSFETs.

## 3.1 Gate-drive design considerations

The gate-drive design of the CoolSiC™ MOSFET initially needs to consider the on-state and off-state of the gate-to-source $V_{GS}$ voltage. As mentioned in chapter 2, for turn-on $V_{GS}$ voltage of on-state operation, , +15 V is recommended to trade off between long-lifetime and low forward voltage. This is also a common turn-on voltage in today's Si IGBTs. In order to ensure low conduction loss, the supply of the gate driver should be regulated for to maintaining the on-state $V_{GS}$ at ideally 15 V ideally. For the turn-off $V_{GS}$ voltage of in off-state operationng, the CoolSiC™ MOSFET itself is truly normally- off to allow $V_{GS}$=0 V for turn-off because with the high robustness of threshold voltage $V_{GS(th)}$, the CoolSiC™ MOSFET is a true "normally-off" device, allowing operation without negative turn-off voltage in many applications . However, the SiC MOSFET is capable of switching at a very high speed. The voltage slew rate may range from tens to hundreds of volts per nanosecond. In order to improve the noise margin, a negative gate-to-source turn-off voltage is normally recommended if maximum switching speed is targeted.Additionally, for hard-switching topology, the negative gate-to-source turn-off voltage can gain additional loss reduction for turn-off. The typical $V_{GS}$ for turn-off can range from -2 V to -5 V. The value of turn-off $V_{GS}$ can be fine-tuned according to the actual system design, however, it is not recommended to have a turn-off $V_{GS}$ lower than -5 V.More details regarding the favorable choice, also taking into account sufficient parameter stability over time, can be found in AN2018-09 [14].

With an active Miller clamp provided by the gate-drive circuit, the need for a negative $V_{GS}$ at turn-off might be eliminated, depending on the final application conditions.

A gate-drive reference circuit for a discrete CoolSiC™ MOSFET TO-247 package is shown in Figure 12. The circuit generally includes an isolated DC power supply and an isolation gate drive IC. The supply power VCC2 of the gate drive IC is provided by the isolated DC power supply. One is for the positive bias with +15 V and the other is for negative bias, -5 V. The common connection of the DC power supply is referenced to the source terminal, therefore, VCC2 determines the turn-on voltage, and GND2 determines the turn-off voltage.

For the drive IC selections, there are some criteria that need to be considered:

- The maximum $V_{GS}$ of the CoolSiC™ MOSFET is -10 V/+20 V, however, the recommended design voltage window for the $V_{GS}$ driver is -5 V/+15 V to cope with voltage spikes caused by ringing. . With high dv/dt, a higher design margin for maximum rating voltage of the gate drive ICs should be provided. Most drivers designed for Si-MOSFET will not provide sufficient voltage rating. In general, gate drive ICs with a maximum voltage rating of 28 V or above can be selected. Depending on the actual operating conditions, a further restriction of the negative $V_{gs\,(off)}$ might apply (see AN 2018-09 [14]).
- With a high dv/dt slew rate of the device, a high CMTI (common mode transient immunity) rating for signal isolation is highly recommended. Otherwise the gate signal may be corrupted by malfunction of the signal isolator.
- To achieve short rise and fall times, high current capability of the driver IC is needed. This will enable the CoolSiC™ MOSFET's fast switching performance at a high dv/dt slew rate.
- The propagation delay and the delay time matching gate drive ICs are very important parameters that should be as short as possible. The short delay time and especially its matchingcan reduce the dead time for bridge topology, and further improve the switching frequency.

There are several gate driver ICs from Infineon recommended for driving CoolSiC™ power MOSFETs. They offer a broad variety of features tailored for specific applications. In the reference design example of the application note for the EiceDRIVER™compact driver ICs with 1200 V coreless transformer technology are selected to drive the CoolSiC™ MOSFET with a recommended +15 V for turn-on and -5 V for turn-off. There are two types of gate drive ICs with different current capability. The 1EDI60N12AF has a typical 9.4 A peak current drive capability, and

the 1EDI20N12AF has a typical 3.5 A peak current drive capability. Both parts have a small propagation delay (typically less than 105 ns with 40 ns input filter time) and high CMTI robustness of over 100 kV/µs, which can be used to drive the discrete CoolSiC™ MOSFET. Advanced gate drive options for SiC MOSFETs using EiceDRIVER™ are presented in an additional Infineon application note AN2017-04 [12].

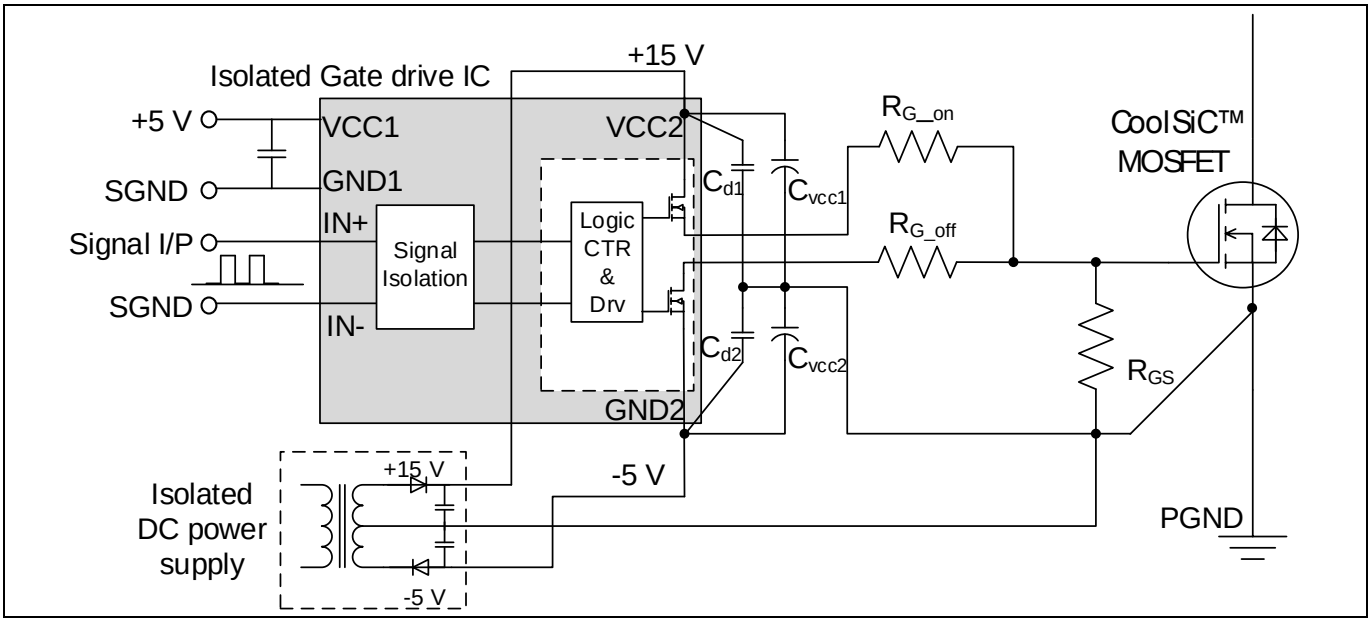



**Figure 12 A gate drive design reference for discrete CoolSiC™ MOSFET**

Here are some design tips for the CoolSiC™ MOSFET TO-247 package:

- Separate gate resistor ($R_G$) into two paths $R_{G\_on}$ and $R_{G\_off}$ individually with a more controllable slew rate, which can prevent an unnecessary increase in switching losses. Normally, a lower value can be selected for the turn-off resistor $R_{G\_off}$ than for the turn-on resistor $R_{G\_on}$ to gain fast fall time and to reduce the risk of a parasitic turn-on.
- For multiple discrete MOSFETs in parallel, ringing may be produced due to the noise oscillation across the MOSFET's Miller capacitors. In this case, a separate gate resistor $R_G$ is recommended for each packaged MOSFET to dampen the noise oscillation between each device.
- Place 1 uF to 2.2 uF capacitor ($C_{VCC1}$ and $C_{VCC2}$) across VCC2 to GND2 at gate drive IC to provide enough peak energy for high switching operations.
- Place some decoupling capacitors ($C_{d1}$ and $C_{d2}$) from 10 nF to 0.1 uF close to the related drive IC's supply terminals. The decoupling capacitors are used to bypass the noise from supply voltage to the power ground to avoid the noise interference between the supply power and gate drive signal. The values of decoupling capacitors can be selected with different values to meet different impedance characteristics with noise frequency. The capacitor $C_{d2}$ should be located very close to the source output PGND and the gate driver IC's ground GND2 to provide very tight coupling between them, which can minimize stray inductance on the gate loop.

## 3.2 Gate drive circuit and PCB layout

Figure 13 shows a gate-drive reference circuit and PCB layout for 2 units IMZ120R045M1 (TO-247 4pin) in parallel. In the circuit, an isolation drive IC U1 1EDI60N12AF is used. One isolated DC-DC converter U2 is used to convert +12 V input on the primary side to +18 V output on the secondary side. A 3 V Zener diode ZD2, with SOD-123 package, is used to split the +18 V into +15 V for turn-on and -3 V for turn-off.

For the PCB layout, the gate source and power source tracks must be separated to avoid the noise interference to the gate signal. This should be applied for both TO-247 3pin and 4pin packages. Normally, gate source tracks

use a narrow width to handle the gate signal, and the power source tracksuse a much wider width to handle high-current and high-power conduction. This enables a Kelvin connection on the PCB board.

In order to reduce commutation loop inductance, the power source and drain trackss are designed as short as possible. The gate resistors and driver IC should be placed close to their corresponding MOSFETs to reduce the gate-loop parasitic inductance. When paralleling TO-247 4pin packages, it is recommended to split part of the gate resistance to the Kelvin source (see $R_3$ and $R_7$ in the circuit below). This limits the circulating current [9] that could form between power source to the Kelvin source of each device.

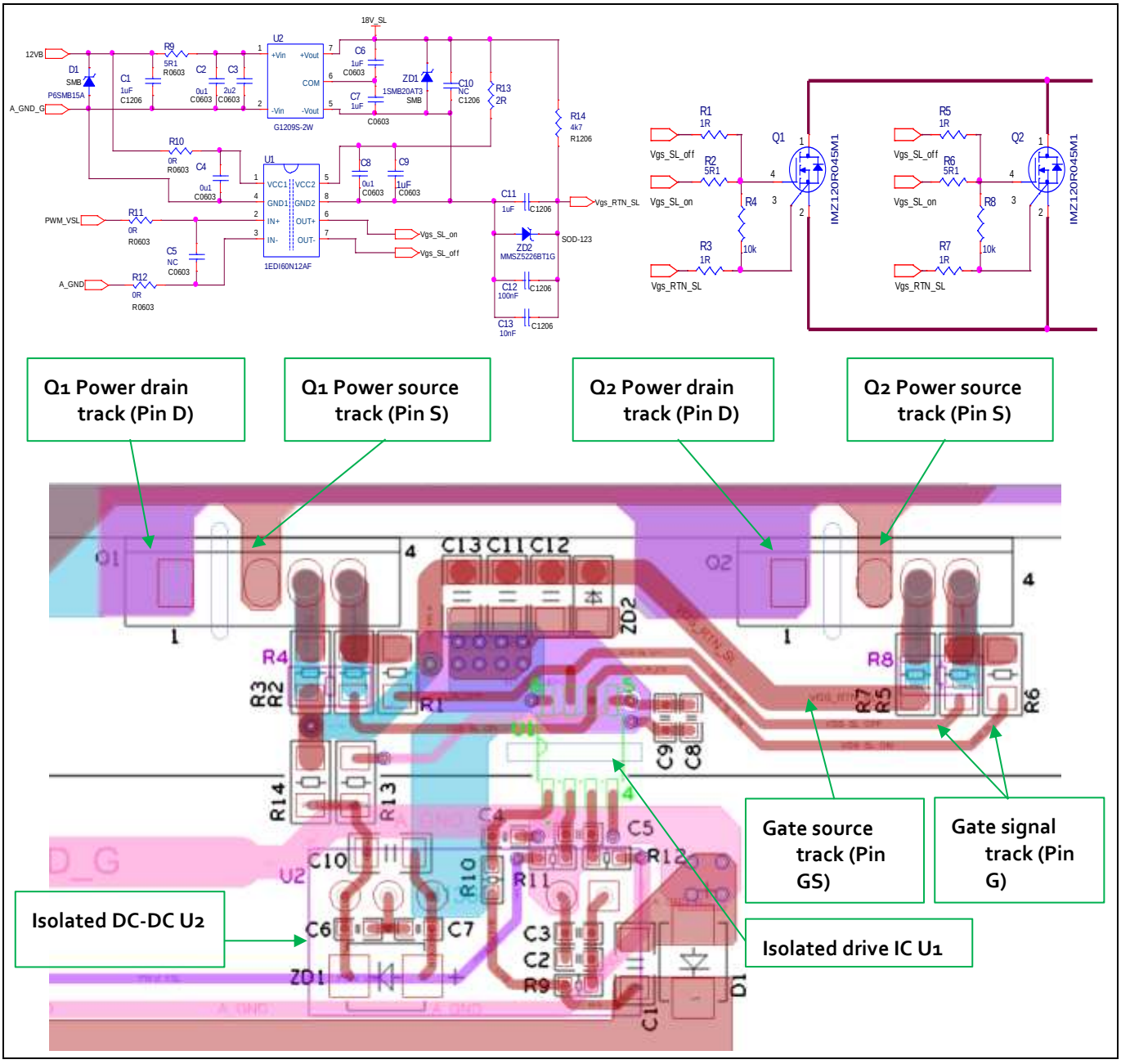



**Figure 13 A drive circuit and PCB layout example of 2 units IMZ120R045M1 with TO-247 4pin package**

The consequence of the high slew rate dv/dt is that it may cause high switching current $I_{GD}$ to flow in the Miller capacitance ($C_{gd}$). If the driver is not properly designed, this effect may cause the device to turn on by mistake, or so called parasitic turn-on on noise, when it is intended to be off. In a conventional hard-switching, half-bridge topology application, this turn-on induced noise increases the risk of shoot-through current, which is a potential

cause of unwanted losses and may damage the device by exceeding its safe ratings. Therefore, it is important to design a driver that not only meets the drive and speed requirements, but also provides a low impedance path.

The CoolSiC™ MOSFET from Infineon has a high $V_{GS(th)}$, typically 4.5 V, and a small ratio of the Miller capacitance $C_{rss}$ related to the gate-source capacitance $C_{gs}$ ($C_{rss}$ / $C_{gs}$ ). This leads to a high robustness against parasitic turn-on. There are other additional practical approaches that help to minimize the turn-on noise:

- Minimize the gate loop inductance by placing the driver as close to the gate and source sense pads as possible.
- Select a driver that has low pull-down output impedance. The low impedance will help to bypass the $I_{GD}$ to the ground. If a gate resistor is used for slew rate control, consider using a separate turn-off gate resistor to minimize the impedance during turn-off. The smaller the turn-off resistor, the smaller the pull-down impedance will be to directly bypass the $I_{GD}$ to the ground.
- Optimize the turn-on speed to limit the dv/dt. This can be achieved by increasing the turn-on resistors, however, this will sacrifice efficiency improvement with higher switching losses. A more advanced technique, called "active Miller clamping" [12], can be used to provide a low impedance path without compromising the turn-off slew rate control.

# 4 The advantages of the CoolSiC™ MOSFET

This chapter outlines the advantages of the CoolSiC™ MOSFET, and highlight the benefits of CoolSiC™ MOSFETs compared to alternative SiC switch devices.

## 4.1 Comparison of switching losses with 1200 V Si IGBT

Figure 14 shows a switching comparison between a 1200 V H3 IGBT (IGW40N120H3) and a CoolSiC™ MOSFET (IMW120R045T1), using the same double-pulse test circuit at 800 V DC, $R_G$=2.2 Ω and recommended $V_{GS}$=+15 V/-5 V. The test setup uses the same freewheeling diode with a 1200 V/20 A G5 SiC Schottky diode (IDH20G120C5) on the high side. Obviously, the CoolSiC™ MOSFET has a significantly lower temperature dependency than the Si IGBT from room temperature to high temperature. Especially for turn-off losses, the Si IGBT has a bipolar nature with approximately ten times higher turn-off losses at 175°C, and five times higher turn-off losses at 25°C. For the turn-on losses, the CoolSiC™ MOSFET has lower turn-on losses than the Si IGBT by a factor of 25% to 50% depending on the drain current $I_D$.

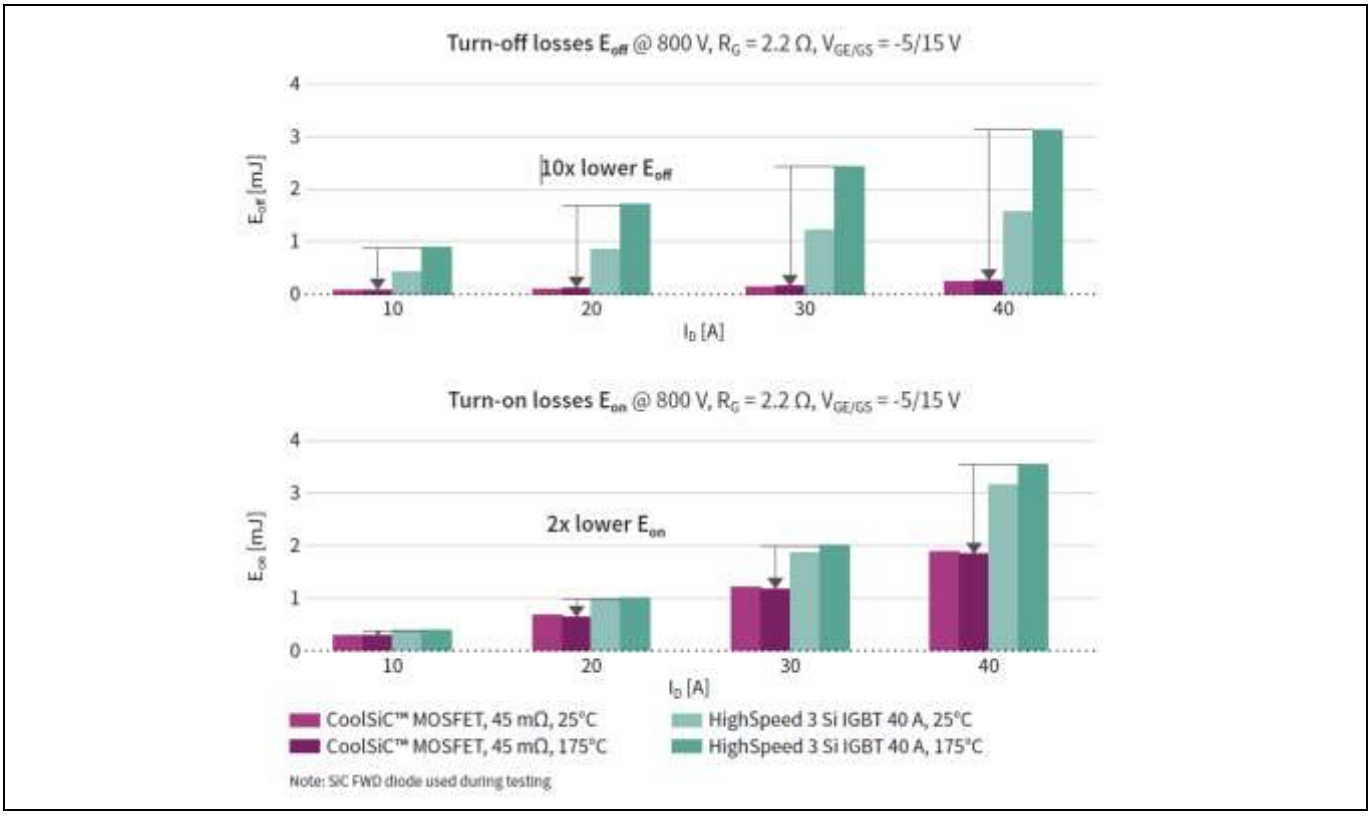



**Figure 14 Switching $E_{off}$ and $E_{on}$ comparison between 1200 V H3 IGBT and CoolSiC™ MOSFET**

## 4.2 Comparison of conduction losses with 1200 V Si IGBT

Figure 15 shows the output characteristics for a 1200 V H3 IGBT (IKW40N120H3) and a CoolSiC™ MOSFET (IMW120R045M1). The forward voltages of both devices are the same at a rated current of 40 A at 25°C. However, the CoolSiC™ MOSFET has a nearly resistive output characteristic when the current is below the rated current. In contrast, the Si IGBT has a diode-like knee voltage drop, typically in the order of 1 V to 2 V, increasing only with the log of the current as shown in the green line. In actual applications, the actual current through the device is normally lower than the nominal rated current of the device. For example, assuming an operating RMS current of 15 A, at room temperature, the forward voltage of the CoolSiC™ MOSFET is half that of the Si IGBTs.At a high temperature of 175°C, the forward voltage of the CoolSiC™MOSFET is around 80% of the Si

IGBT's. This concludes that the CoolSiC™ MOSFET has lower conduction losses than the same rated Si IGBT in actual application condition.

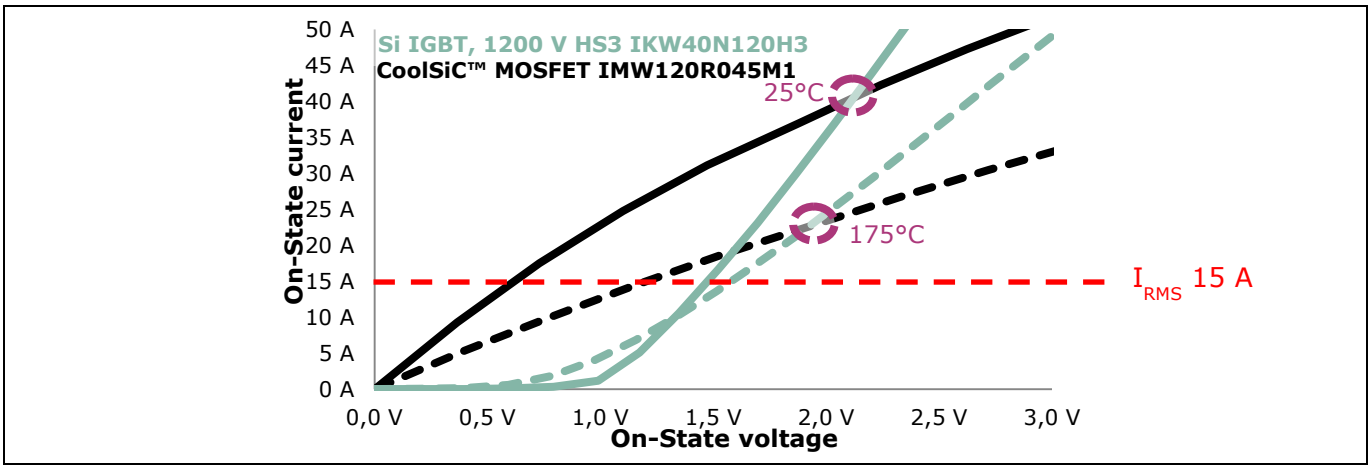



**Figure 15 Output characteristic comparison between 1200 V H3 IGBT and CoolSiC™ MOSFET**

## 4.3 Body diode commutation comparisons

The intrinsic body diode of the CoolSiC™ MOSFET performs in a similar way as a SiC Schottky diode with low reverse-recovery charge $Q_{rr}$. At 25°C, it has almost the same $Q_{rr}$ with the rated current 1200 V G5 SiC Schottky diode. However, the $Q_{rr}$ will increase with the increase of junction tempertature due to the intrinsic pn junction structure with reverse-recovery time. As show in Figure 16 (left), , the body diode of the CoolSiC™ MOSFET has a slightly higher $Q_{rr}$ than a 1200 V 20 A SiC G5 Schottky diode at a high temperature of 175°C. It has a very small influence on the overall performance, even at maximum junction temperatures.

Figure 16 (right) also compares the $Q_{rr}$ between the 650 V 41 mΩ Si MOSFET, which integrates the fast recovery body diode and the CoolSiC™ MOSFET. It proves that the 1200 V CoolSiC™ MOSFET's body diode has less than 10% $Q_{rr}$ of 650 V Si MOSFET at room temperature and at high temperture.

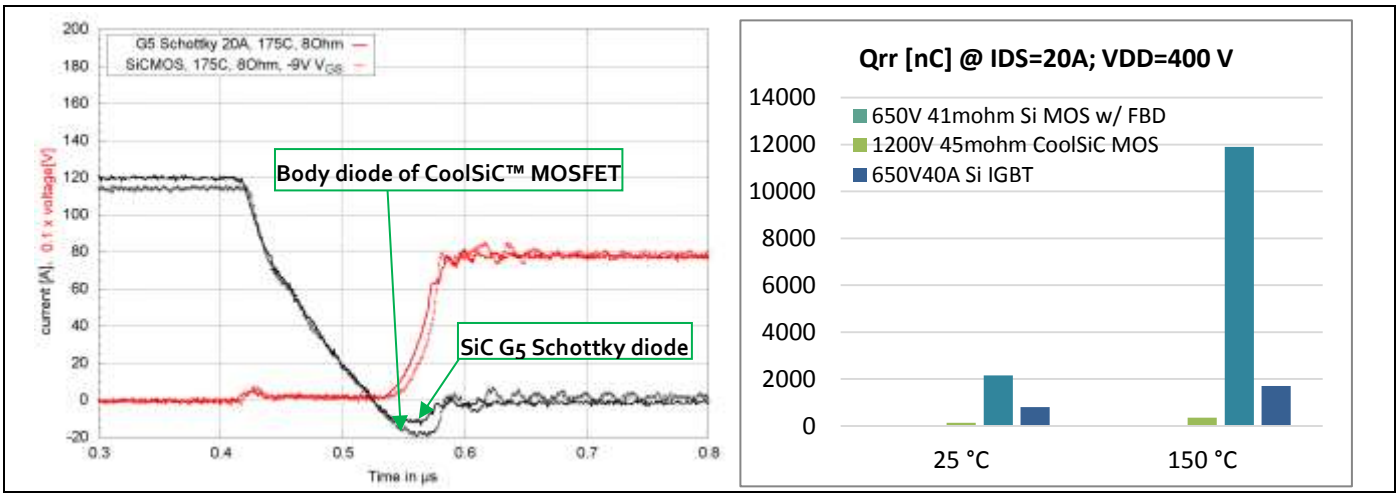



**Figure 16 Body diode commutation and body diode $Q_{rr}$ comparison with 650 V Si MOSFET with fast body diode**

## 4.4 Comparison of CoolSiC™ MOSFET with alternative SiC switches

Given the benefits of the SiC material mentioned in chapter 1, there are extensive investments in research and development of the SiC MOSFET as a normally switched-off transistor. The initial fabrication of the SiC MOSFET

was stifled mainly by the quality of the SiC/SiO2 interface. The poor quality of the boundary between the SiC surface and oxide resulted in low mobility in the inversion layer, while the high electric field generated within the SiC in blocking mode could cause degradation of the gate oxide, thus influence its lifetime and reliability. Although these issues have improved in recent years, there are still many concerns about how to increase channel mobility while keeping the same gate-oxide reliability as with a traditional Si transistor.

Compared to the standard planar SiC MOSFET, the SiC trench MOSFET uses a crystal lattice plane for the inversion channel, which enables high channel mobility, thus allowing a larger thickness for SiC MOSFET's gate oxide, which in turn leads to higher robustness. However, as SiC devices operate in blocking mode with high drain-induced electric fields, the challenge is to limit the electric gate-oxide field at the corners of the trenches. The CoolSiC™ 1200 V trench MOSFET uses a favorable trench structure to increase channel mobility.In addition, the device is specifically realized by deep buried p-type regions that adjoin a part of the trench structure, and reach well below the depth of the actual trench to reduce the off-state induced electric field. The CoolSiC™ MOSFET contains a trench structure in which the MOS channel is aligned to the a-plane to optimize channel mobility and to reduce the $V_{th}$ spread. Finally, the above-mentioned deep p-regions are effectively connected by an ohmic contact to the source and thus, act as a powerful body diode.

With the same high performance as other SiC MOSFETs, the CoolSiC™ MOSFET has the following unique advantages:

- The CoolSiC™ MOSFET has very reliable gate oxide with critical electric field well-limited to guarantee full gate-oxide reliability.
- In order to be compatible with Si IGBT, the CoolSiC™ MOSFET is designed with +15 V typical turn-on, gate-to-source voltage $V_{GS}$, combined with the benchmark gate threshold voltage $V_{GS(th)}$ of 4.5 V at $T_j$=25°C and $I_{DS}$=10 mA with ease of use.
- The CoolSiC™ MOSFET structure has a favorable ratio of the Miller capacitance $C_{rss}$ and the gate-to-source capacitance $C_{gs}$ which provides an excellent trade-off between controllable switching speeds and immunity against parasitic turn-on.
- The large area of the p-emitter enables the device to be used as a rapid freewheeling diode with high commutation robustness and low reverse-recovery charge $Q_{rr}$.
- The CoolSiC™ MOSFET technology offers chips, discrete devices and modules, targeting different applications. The discrete MOSFET is not only available in the well-established TO-247 but also in the TO-247 4pin package with the additional Kelvin source connection to further reduce switching losses. For MOSFET modules, different package types (Easy 1B, Easy 2B, 62 mm, etc.) are offered to cover different power applications.

With the aforementioned advantages, the CoolSiC™ MOSFET brings many benefits to the system design including high reliability and efficiency improvement. It enables high switching frequency and high power density, and reduces system complexity and total system cost.

## 4.5 Gate-oxide reliability of CoolSiC™ MOSFET

The CoolSiC™ MOSFET normally targets high-power applications with high frequency and high voltage, which typically require the highest reliability. Besides the standard reliability topics, gate oxide is one of the most important concerns for the SiC MOSFET [6] [7].

The commercially existing SiC MOSFETs have a relatively thin gate oxide in order to reduce the channel resistance. Therefore, the reliability of the gate oxide for high-gate voltages must be investigated due to the thinner gate oxide. For SiC MOSFETs, the main focus so far was the stability under reverse-bias stress due to the differing fields applied when compared to silicon components. However, for actual applications, the on-state stress on the oxide is much more severe in existing MOSFETs due to the thin oxide layers. Tests of commercial MOSFET products reveal that this issue is still a serious concern for applications in industrial systems.

### The advantages of the CoolSiC™ MOSFET

Thanks to the specific trench structure, CoolSiC™ MOSFETs can increase channel mobility as well as improve gate-oxide reliability. The challenge regarding the gate-oxide reliability of SiC MOSFET devices is to ensure a sufficiently low failure rate, including extrinsic defects, throughout a desired lifetime under given operation conditions. Long-term tests with a large number of CoolSiC™ MOSFETs were performed in order to investigate extrinsic gate-oxide failure rates referring to [2]. This experiment was done in 2 groups of 1000 discrete devices performed at 150°C under constant gate-bias stress for 3 times 100 days. The gate-source voltage was increased by +5 V after each 100 day period. The failure statistics fit well to the linear E-model. By extrapolating these results to 20-years operation lifetime of the device, the model predicts a failure rate of 0.2 ppm with the on-state operation of $V_{GS}$=+15 V. The experiment provides evidence that the CoolSiC™ MOSFET has an IGBT-like reliability of the gate oxide. This matches well with typical industrial requirements.

# 5 Basics of CoolSiC™ MOSFET power modules

Semiconductor power modules offer several advantages in terms of power density, thermal management, manufacturability and reliability. Figure 17 shows the construction of a semiconductor power module.

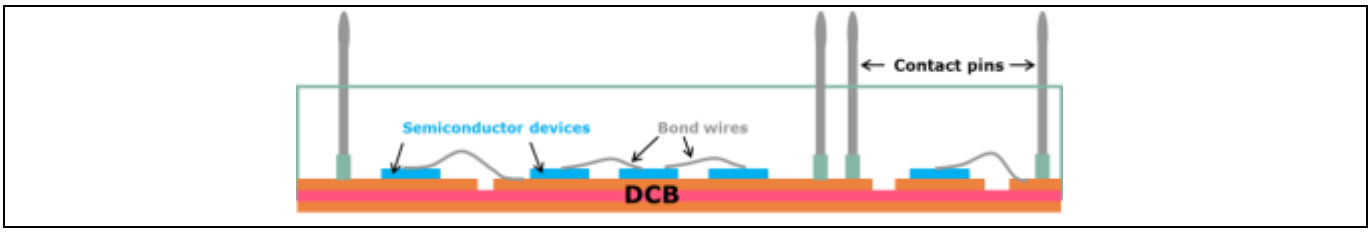



**Figure 17 The construction of a semiconductor power module**

The semiconductor power device is assembled on a substrate. The substrate of a power module has several functions:

- To isolate the power device from the heatsink/baseplate.
- To transfer heat from the power device to the heatsink.
- To connect several power devices in a circuit or parallel assembly.

The connection of the power modules semiconductor chips to the system is performed via terminals at the top of a power module. Infineon power modules use solder or PressFIT pins as well as screw contact terminals. The connection of the devices with the terminals and the internal circuitry not ensured by the DCB is performed with bond wires. In contrast to the well-known standard packages with baseplates, the Easy-module platform enables a highly symmetric, low-inductive design. For this reason, the popular and flexible Easy1B power module is used to implement the first CoolSiC™ MOSFET solutions. The flexible pin grid of Easy modules simplifies the PCB layout, and offers a stray inductance below 10 nH. The 62 mm package offers the possibility of low-inductance connection of systems in the medium power range.

For assembly and mounting Instructions, please refer to Infineon's application notes in AN2009-01 for Easy PressFIT modules, and AN2012-05 for 62 mm modules.

## 5.1.1 Stray inductance

Probably the most important parasitics which have to be taken into account for the development of a power electronic application are stray inductances. Stray inductances are a consequence of internal and external connections between the semiconductor devices and the power electronic system.

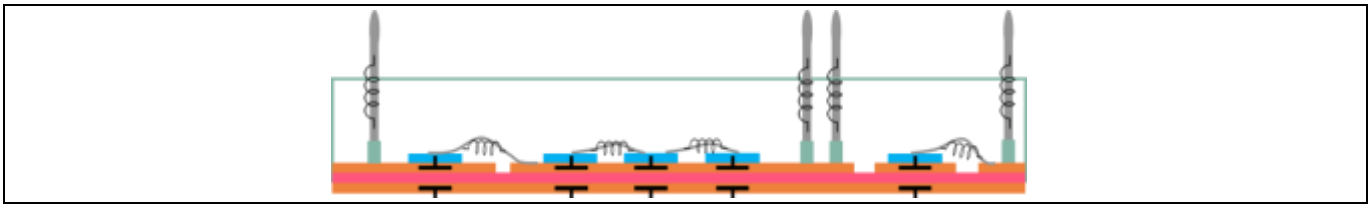


**Figure 18 The construction of a semiconductor power module with equivalent parasitic parameters**

During a switching event, voltage drops along an inductor according to the following equation:

$$\Delta V = L \times di/dt.$$

This voltage drop has an influence on the turn-on and turn-off behavior of a power device. Figure 19 shows the turn-on and turn-off waveforms of a FF11MR12W1M1_B11 CoolSiC™ power module.

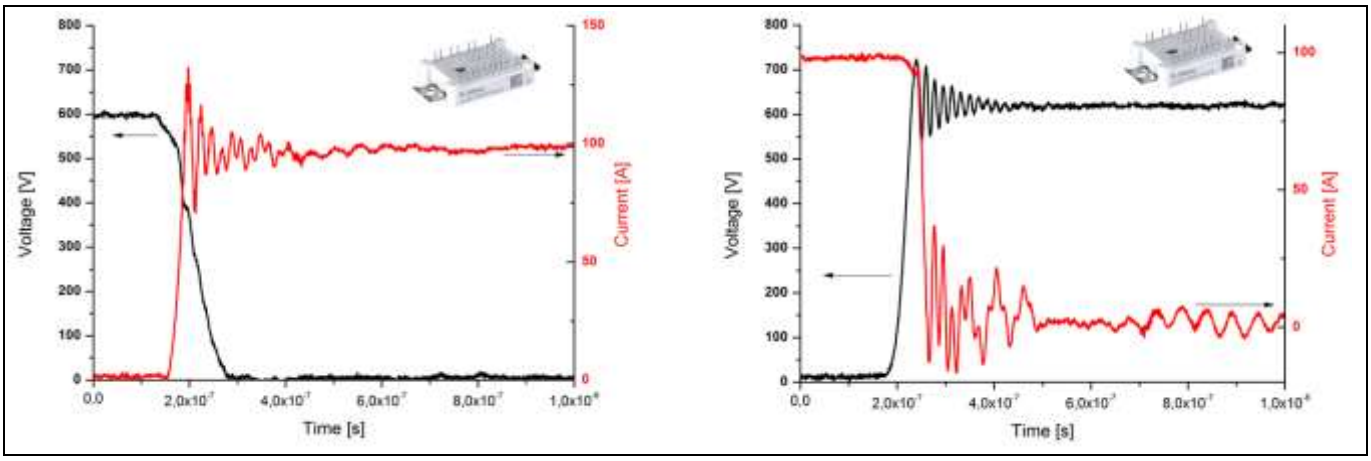



**Figure 19 Switching waveform for SiC Module (FF23MR12W1M1_B11)**

The voltage drop during turn-on leads to a drop of $V_{DS}$ leading leading forcefully a reduction of the turn-on energy. During the turn-off of the device, the voltage leads to an increase of the voltage spike. If this voltage increase is larger than the device breakdown voltage, the device will fail and the power module will be destroyed. Consequently, the turn-off of a power device is the critical event to look at with respect to the stray inductance of power modules.

As the CoolSiC™ MOSFET is much faster than the IGBT within the same voltage class, power modules with large stray inductances (>20 nH) are limiting the use of CoolSiC™ MOSFET power modules with respect to the maximum allowed switching speed and/or applied voltages. That is the reason why CoolSiC™ MOSFET modules have to reduce the stray inductance as much as possible.

Infineon has more than 25 years' experience in the development of low inductive power modules. One example for low inductive modules is the EasyPACK, shown in Figure 20.

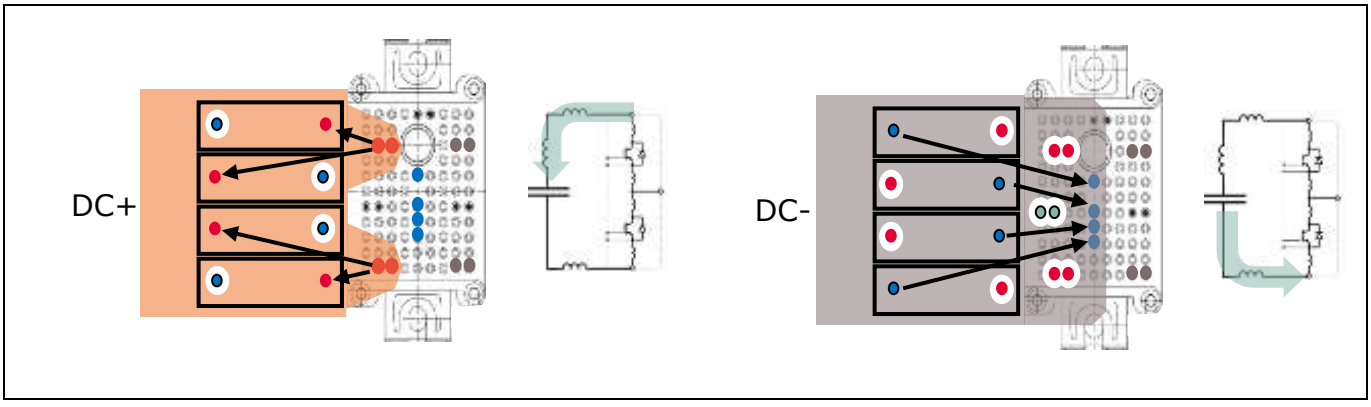



**Figure 20 CoolSiC™ MOSFET EasyPACK module**

The presented module uses a strip-line approach in a thin package leading to low stray inductances. This approach and a smart module design were used in the development of CoolSiC™ MOSFET power modules like the FF11MR12W1M1_B11 as a half-bridge module, or the DF11MR12W1M1_B11 as a booster module, which leads to a stray inductance of only 9 nH. This low stray inductance allows for fast switching at high voltage, for example. MPPT boost of 1100 V solar inverters with DF11MR12W1M1_B11. The half-bridge module with FF11MR12W1M1_B11 can be configured to different inverter or rectifier topologies that target solar, EV charger, UPS and other high-switching frequency converters.

# 6 Conclusion

This application note presents the CoolSiC™ 1200 V SiC MOSFET including the results of a performance characterization and its features. Some general practical design guidelines are highlighted for designing the CoolSiC™ MOSFET in a power system.

# 7 Glossary

$R_{ds(on)}$ is the resistance at the actual junction temperature, given at the datasheet current $I_{DS}$

$T_j$ temperature on the top of the chip where the power dissipation takes place (junction ➔ pn junction

$V_{GS(th)}$ Voltage between gate and source at which current starts to flow, defined for $V_{GS}$=$V_{DS}$ and $I_{DS}$ = 10mA. This threshold voltage must always be measured after the device is brought to a defined state. Here after a VGS= +20V measurement, e.g. an IGSS @ 20V. Otherwise, due to hysteresis effects, this value is different

$I_{DSS}$ This $I_{DSS}$ values (DSS = drain-source at shorted gate-source voltage = 0V) is the leakage current whenever the switch is off at $V_{GS}$ = 0V and $V_{DSS}$= 1200V

$V_{GS}$ bias between drain and source, corresponds to $V_{ge}$ in an IGBT

$I_{DS}$ load current flowing between drain and source, the datasheet current is calculated by

$$I_{D,max} = \sqrt{\frac{T_{vj,max} - T_C}{R_{th(vj-c),max}} \frac{1}{R_{DS,on}}}$$

$V_{DS}$ bias between drain and source, corresponds to $V_{ce}$ in an IGBT

$C_{rss}$ This value is defined as the capacitance effective between gate and drain. It is measured at 800 V which is the typical DC link voltage in the application. It equals the gate-drain capacitance

$C_{gs}$ effective capacitance between source and gate

$C_{iss}$ This value is defined as the capacitance effective between gate and source. It is measured at 800 V which is the typical DC link voltage in the application. It equals the sum of gate-source capacitance and gate-drain capacitance

$C_{gd}$ effective capacitance between drain and gate

$C_{oss}$ This value is defined as the capacitance effective between source and drain. It is measured at 800 V which is the typical DC link voltage in the application. It equals the sum of gate-drain capacitance and gate-source capacitance

$C_{ds}$ effective capacitance between source and drain

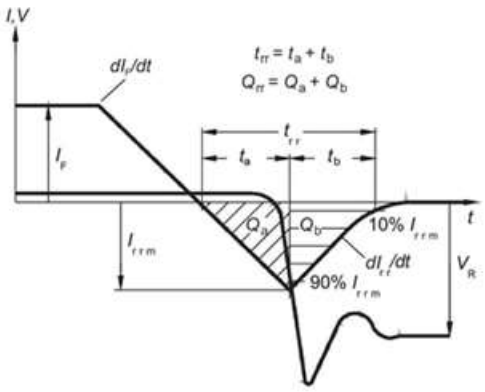
$R_{G\_int}$ effective internal gate resistance, comprising the sum of the resistance of the distributed gate network and additional resistors added to the gate pad

$E_{on}$ Turn-on loss energy, measured according to the guideline available for IGBT's

$E_{off}$ Turn-off loss energy, measured according to the guideline available for IGBT's

$E_{tot}$ Total loss energy, sum of $E_{on}$ and $E_{off}$

$Q_{rr}$ reverse-recovery charge, measured according to guidelines known from silicon pin diodes




$I_{rrm}$ reverse-recovery current, see picture above

## Glossary

| | |
|---|---|
| $Q_{GD}$ | typically the gate charge needed to pass the Miller plateau |
| $Q_G$ | total gate charge |
| $Q_{GS,pl}$ | gate charge needed to reach the Miller from the off-state $V_{GS}$ |
| $R_G$ | externally applied gate resistor, adds to $R_{G\_int}$ |
| $R_{G\_on}$ | externally applied gate resistor for turn-on in case of separated sink and source outputs of a driver circuit/IC, adds to $R_{G\_int}$ |
| $R_{G\_off}$ | externally applied gate resistor for turn-off in case of separated sink and source outputs of a driver circuit/IC, adds to $R_{G\_int}$ |

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## Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| Revision 1.0 | 2018-01-05 | First release |
| Revision 1.1 | 2018-07-01 | Various minor changes and additional information implemented in all paragraphs, Figure 8 revised |
| | | |

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