EiceDRIVER™

Advanced use of pin EN-/FLT

About this document

Scope and purpose

This application note targets to explain the function of the EN-/FLT pin of the 2EDL23 half bridge driver IC in detail and hint out the different solutions between microcontroller and driver IC concerning Enable and Fault function.

Intended audience

Power electronics engineers who want to design gate driving circuits with focus on Enable and Fault functions.

Table of Contents

1 Scope and product family

The 2EDL family consists of high voltage half bridge gate drive ICs up to a maximum blocking voltage of 600V. Typical applications are consumer- and industrial drives, fans, pumps, induction cooking equipment or switch mode power supplies. The 2EDL family is designed in silicon-on-insulator-technology (SOI). This technology provides an excellent ruggedness against negative voltage spikes and noise.

This application note gives information for the advanced use of the pin “EN-/FLT”, which is a combined enable function and fault signal, indicating undervoltage lockout or overcurrent. This double function is implemented in the products 2EDL23x06PJ according to Table 1.

Table 1 Members of the 2EDL family

Product Name	EN-/FLT	deadtime & interlock	typ. UVLO-Thresholds	Bootstrap diode	Package
2EDL05I06PF, 2EDL05I06PJ	No	Yes	12.5 V / 11.6 V	Yes	DSO-8 DSO-14
2EDL05I06BF	No	No	12.5 V / 11.6 V	Yes	DSO-8
2EDL05N06PF	No	Yes	9 V / 8.1 V	Yes	DSO-8
2EDL23I06PJ	Yes	Yes	12.5 V / 11.6 V	Yes	DSO-14
2EDL23N06PJ	Yes	Yes	9 V / 8.1 V	Yes	DSO-14

The 2EDL family provides positive control logic as well as different undervoltage lockout levels for MOSFET and IGBT. The pin designations, control signals, thresholds and parameters described in this application note must be understood according to the individual part.

Target applications are all cost sensitive designs in the consumer- and low end industrial area. All devices are therefore compatible even to microcontrollers with a supply voltage of 3.3 V. The 2EDL is compatible to the same footprint as a number of other gate drive ICs in the market. Nevertheless, many features are built in, which provides add-on values to the application. Please also refer to the product datasheet of the 2EDL23I06PJ and 2EDL23N06PJ.

2 General operation of pin EN-/FLT

This pin is available within the 2EDL23x06PJ devices only. It is a bidirectional open drain output pin, which can shut down the IC in input mode and which indicates either low side undervoltage lockout or overcurrent in output mode.

The signal applied to pin EN directly controls the output sections when used in input mode. All outputs are set to LOW if this signal is lower than V_{EN-} = 0.9 V typically. Operation is enabled with signal levels higher than V_{EN+} = 2.1 V. The electrical function related to the EN-Signal is given in Figure 1. The pull-down resistor has a value of ~73 kΩ. The propagation delay time from EN to the output sections is about t_{EN} = 550 ns.

The IC is permanently enabled when the EN pin is pulled up to the logic section's supply voltage V_{supply}, for instance +5 V / +3.3 V. It is not recommended to pull this pin up to VDD, because this can lead to excessive power dissipation in the input structure of this pin and could destroy the IC.

This pin can be used as a redundant way to shut down the application in case that a repetitive failure occurs or a first shut down mechanism, for example by ITRIP function at PGND pin as over current protection, fails by incident.

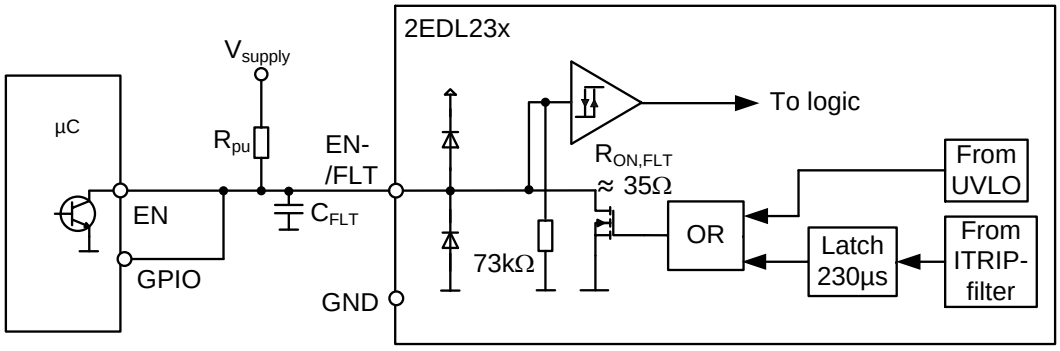

Figure 1 Schematic of the EN-/FLT-pin structure

This pin indicates the failure status of the IC. The signal level at this pin is LOW in case of undervoltage lockout or triggering of the overcurrent protection. An external pull-up resistor to Vsupply, in the range of 4.7 kΩ is necessary to bias this open drain pin. The voltage at this pin is internally clamped to VDD, as can be seen in the internal structure according to Figure 1. The internal pull-down FET has a typical resistance of RON, FLT = 35 Ω. The delay time from the overcurrent trigger event (ITRIP) to the change of status at the EN-/FLT-pin is tFLT = 2.1 µs typically according to the timing diagram depicted in Figure 2.

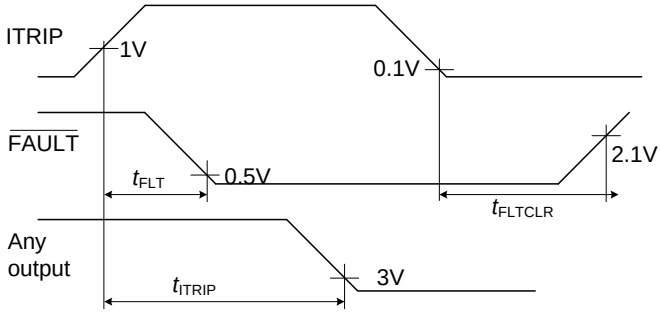

Figure 2 Timing diagram for t_{FLT} propagation delay

3 Temporary fault latch

It is common in cost sensitive applications that emergency signals are captured by polling techniques, as low cost microcontrollers do not offer fast track interrupt pins. Thus, the microcontroller verifies given I/O-ports within a defined interval. As a consequence, failure signals must be latched outside the microcontroller. Such a latch can be implemented by properly using the EN-/FLT pin of the 2EDL23I06PJ and 2EDL23N06PJ. Two different cases of operation must be considered:

- The driver IC indicates a fault condition and the microcontroller port is an input
- Active release and shut down of the driver IC by the microcontroller

3.1 The driver IC indicates a fault condition and the microcontroller port is an input

Figure 3 indicates the connection between the microcontroller and the driver ICs for a three phase drive system. All three EN-/FLT pins are connected directly to each other. This configuration does not consider an enable or shut down option by active manipulation at pin EN-/FLT. A common pull-up resistor R_{pu} enables the drive. The capacitor C_{FLT} has two functions. First, it acts as a filter capacitor for the polling input of the microcontroller and second, it works as a delay component for restart after an overcurrent protection event

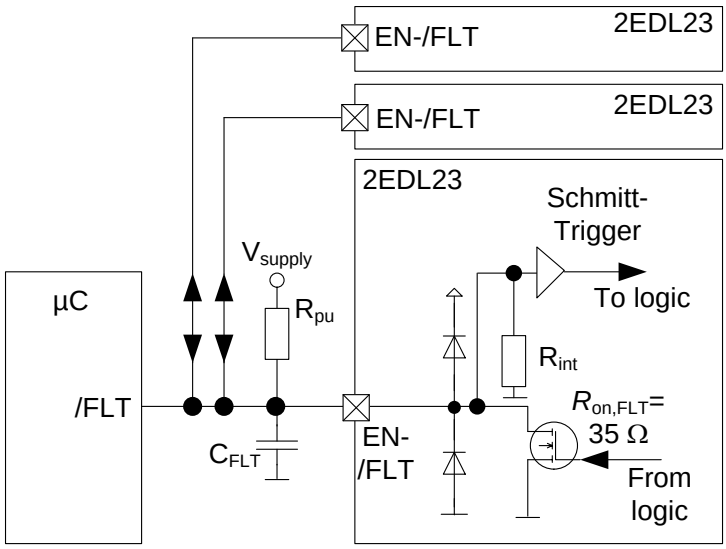

Figure 3 Circuit schematic for temporary latch of fault signal

Four values are influenced by selecting R_{pu} and C_{FLT}:

- $V_{EN,low}$, which is the steady state voltage at EN-/FLT after discharging the capacitor C_{FLT}. This voltage must be lower than the input logic low level V_{ILmin} of the microcontroller
- $V_{EN,high}$, which is the steady state voltage at pin EN-/FLT during normal operation. This voltage must be higher than the input logic high level V_{IHmax} of the microcontroller
- t_{dis}, which is the time interval needed for discharging C_{FLT} from $V_{EN,high}$ to V_{ILmin}. This time must be shorter than the fault clear time t_{FLTCLR}
- t_{ch}, which is the time interval needed for charging C_{FLT} from $V_{EN,low}$ to V_{IHmax}

$V_{EN,low}$ and $V_{EN,high}$ must be calculated to check if the steady state voltages after discharging or after charging can reach the logic threshold levels for V_{ILmin} and V_{IHmax} for both, micorcontroller and driver IC.

Here, the V_{ILmin} should take the lower one when comparing the microcontroller's vaule and driver IC's value, meanwhile V_{IHmax} should take the higher one. The interval T_{dis} must be shorter than the minimal value of t_{FLTCLR} of the 2EDL family. This means that certain conditions must be met:

$$V_{\mathrm{EN,low}} = \frac{R_{\mathrm{pd}}}{R_{\mathrm{pd}} + R_{\mathrm{pu}}} \cdot V_{\mathrm{supply}}\,, \quad R_{\mathrm{pd}} = \frac{R_{\mathrm{int}} \cdot R_{\mathrm{on,FLT}}}{R_{\mathrm{int}} + R_{\mathrm{on,FLT}}}, \text{assuming the input logic low level } V_{\mathrm{ILmin}} = 0.7\,V \tag{1}$$

$$V_{\mathrm{EN,high}} = \frac{R_{\mathrm{int}}}{R_{\mathrm{int}} + R_{\mathrm{pu}}} \cdot V_{\mathrm{supply}}\,, \text{assuming the input logic high level } V_{\mathrm{IHmax}} = 2.4\ \mathrm{V} \tag{2}$$

$$T_{\mathrm{dis}} = R_{\mathrm{C}} \cdot C_{\mathrm{FLT}} \cdot \ln\left(\frac{V_{\mathrm{EN,high}}}{V_{\mathrm{ILmin}}}\right) < t_{\mathrm{FLTCLR}} \quad , R_{\mathrm{C}} \approx R_{\mathrm{pd}} = \frac{R_{\mathrm{int}} \cdot R_{\mathrm{on,FLT}}}{R_{\mathrm{int}} + R_{\mathrm{on,FLT}}} \tag{3}$$

From equation (1) and (2), the allowed range of the pull-up resistor R_{pu} can be derived. The boundary conditions are

$$\text{from equation (1):}\ R_{\mathrm{pu}} > \frac{V_{\mathrm{supply}} - V_{\mathrm{ILmin}}}{V_{\mathrm{ILmin}}} \cdot \frac{R_{\mathrm{int}} \cdot R_{\mathrm{on,FLT}}}{R_{\mathrm{int}} + R_{\mathrm{on,FLT}}} \tag{4}$$

$$\text{from equation (2):}\ R_{\mathrm{pu}} < \frac{V_{\mathrm{supply}} - V_{\mathrm{IHmax}}}{V_{\mathrm{IHmax}}} \cdot R_{\mathrm{int}} \tag{5}$$

Equations (4) and (5) only depend on one application specific parameter, which is the supply voltage of the microcontroller. The mainstream microcontrollers such as Infineon´s XC800 or XMC4000 series usually are supplied from a 5V or a 3.3V source, while the switching thresholds of the 2EDL family are defined for accepting 3.3V logic signals. Additionally, the capacitor C_{FLT} is given for an enlarged fault clear time T^*_{FLTCLR}.

$$T^*_{\mathrm{FLTCLR}} = R_{\mathrm{C}} \cdot C_{\mathrm{FLT}} \cdot \ln\left(\frac{V_{\mathrm{supply}}}{V_{\mathrm{supply}} - V_{\mathrm{IHmax}}}\right)\,, \ R_{\mathrm{C}} \approx R_{\mathrm{pu}} \tag{6}$$

Please note, that the integrated pull-down resistor R_{int} is n-times in parallel when operating a n-phase system. In this case $R^*_{int,N} = R_{int}/n$ should be used to replace R_{int} in the related equations.

Table 2 presents the range of the pull-up resistor R_{pu} for 5V and for 3.3V.

Table 2 Evaluation and design proposal for R_{pu} and C_{FLTCLR}

V_{supply}	Phases	$R_{pu,min}$ / $R_{pu,max}$	$R_{pu,select}$	C_{FLTCLR}	$V_{EN,high}$	$V_{EN,low}$	T_{dis}	T^*_{FLTCLR}
3.3 V	1	130 Ω / 27.3 kΩ	6.8 kΩ	220 nF	3.019 V	0.017 V	12.5 µs	1.9 ms
5 V	1	215 Ω / 79,0 kΩ	8.2 kΩ	330 nF	4.495V	0.021V	21.5 µs	1.8 ms
3.3 V	3	130 Ω / 9.1 kΩ	5.6 kΩ	220 nF	2.683 V	0.020 V	10.3 µs	1.6 ms
5 V	3	215 Ω / 26.2 kΩ	8.2 kΩ	330 nF	3.740 V	0.021 V	19.3 µs	1.8 ms

3.2 Active release and shut down of the driver IC by the microcontroller

Some applications require an active option to release and to shut down the power transistors. This can be implemented in a simple way by activating the EN-/FLT pin. Three possible cases have to be taken into account:

- Release and shut down including temporary latch of failure mode
- Release and shut down without temporary latch of failure mode
- Using a microcontroller providing output pins with open drain option

Please note that all options described in section 3.2 can be combined with any option of section 3.1.

3.2.1 Release and shut down including temporary latch of failure mode

It can be derived from equations (1) to (5) that there is no technically reasonable solution by extending the circuit of Figure 3 by simply adding an additional EN-pin of the microcontroller. A solution can be introduced by an additional small signal transistor or a diode, which actively pulls down the voltage level at the EN-/FLT pin in a short time. Thus, the microcontroller's EN-pin can act as an emergency shut down for the application according to Figure 4. Transistor T1 or diode D1 disable all driver ICs by pulling down all connected EN-/FLT pins and overriding the external pull-up resistor.

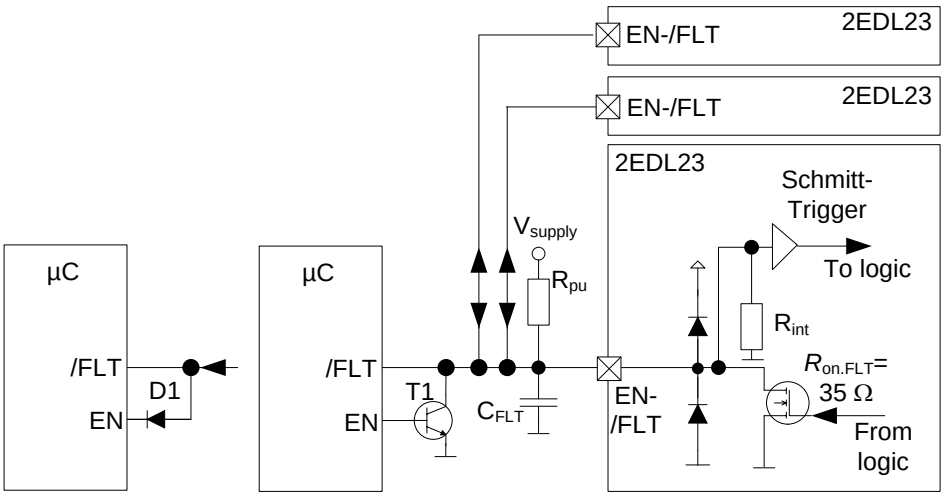

Figure 4 Circuit diagram for release and shut down by microcontroller with a diode or a transistor

A restart signal by enabling from microcontroller side will follow the charging curve of capacitor C_{FLT} through pull-up resistor R_{pu}, when using the circuit of Figure 4. The charging curve is described by equation (6).
With $R_C = R_{pu}$ the period of time $T_{EN,\mu C}$ until the system is finally released by the microcontroller is

$$T_{EN,\mu C} = R_{pu} \cdot C_{FLT} \cdot \ln\left(\frac{V_{supply}}{V_{supply} - V_{IHmax}}\right). \quad (7)$$

3.2.2 Using a microcontroller providing output pins with open drain option

Some microcontrollers, such as the XC800 series [1], the XE16x series [2] or the XMC4000 series [3] from Infineon provide general purpose I/O pins which are configurable as open drain outputs. This makes the two ideas discussed in section 3.2.1 very simple to be implemented just by connecting the capacitor C_{FLT} to the particular microcontroller pin, which is configured as an open drain pin as shown in Figure 5. The schematic clearly depicts how simple an intelligent use of the 2EDL family can be.

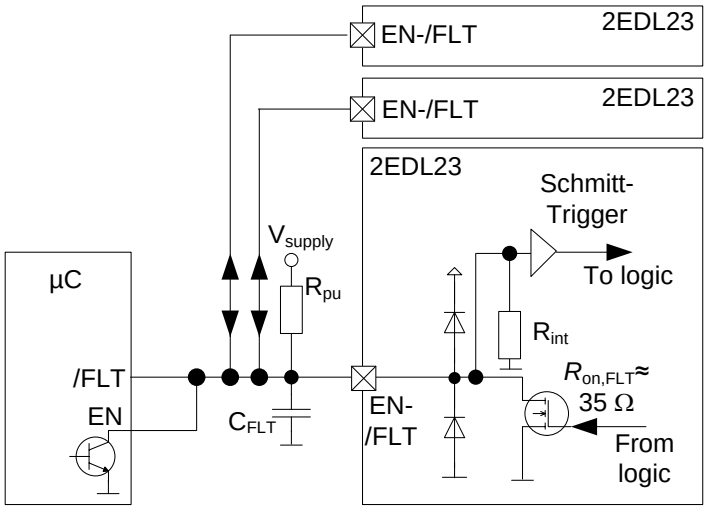

Figure 5 Circuit diagram for release and shut down directly by open drain output of microcontroller

All equations (1) to (7) have to be considered in this case for the design of the pull-up resistor R_{pu} and the filter capacitor C_{FLT}.

3.2.3 Release and shut down without temporary latch of failure mode

This option is very simple to implement, because no timing conditions have to be considered. Figure 6 depicts the related application circuit. The enable / shut down function is included by using a decoupling resistor R_{dec}. The filtering capacitor C_{FLT} is basically neglected because it is usually very small in the range of a couple of 100 pF for filter purposes only. Also the external pull-up resistor R_{pu} can be left out, because the EN-pin of the microcontroller takes over the pull-up function.

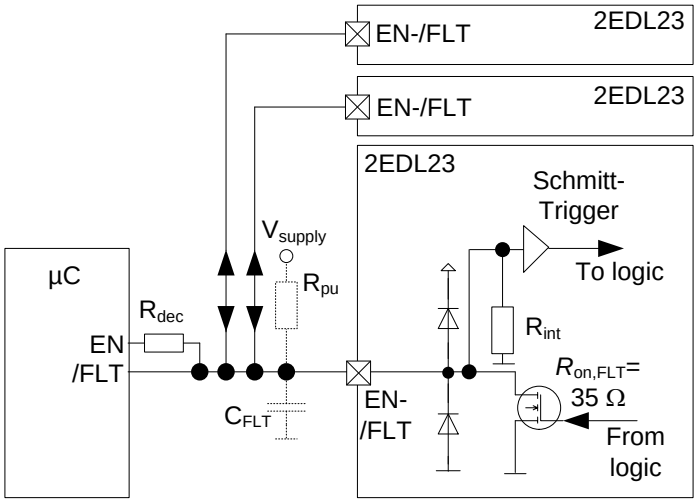

Figure 6 Circuit diagram with release and shut down without temporary latch

The decoupling resistor R_{dec} must be dimensioned in a way that the integrated active pull-down transistor inside of the driver IC can still pull down the signal. As a result, the voltage at the µC-pin /FLT can reach the lower switching threshold in case of shut down.

Thus, only a single equation must be considered, in case R_{dec} is chosen as a pull-up resistor in the range of a couple of kΩ.

$$R_{\mathrm{dec}} > \frac{V_{\mathrm{supply}} - V_{\mathrm{ILmin}}}{V_{\mathrm{ILmin}}} \cdot \mathrm{R}_{\mathrm{on,FLT}} \qquad (8)$$

Please note that there may occur timing issues when R_{dec} is quite high.

During normal mode, the driver IC has a high resistive input as R_{int} = 73 kΩ, so that this case can usually be covered by the µC capabilities. Please note here, as shown in section 3.1, that the integrated pull-down resistor R_{int} is n-times in parallel, when operating an n-phase system. This means $R^{*}_{int,N} = R_{int} / n$. In this case, please carefully calculate the proper value for R_{dec} to ensure the $V_{EN,high}$ level can still reach the maximum EN positive going threshold $V_{EN,TH+}$ of the driver IC which is 2.4 V for the 2EDL23. In case the driving capability of the microcontroller output pin is not enough to drive the EN/-FLT pin, an external pull-up resistor to V_{supply} as depicted in Figure 3 is recommended.

4 References

[1] Infineon Technologies: XC800 family; User´s manual; Infineon Technologies, Germany, 2010

[2] Infineon Technologies: XE16x family; User´s manual; Infineon Technologies, Germany, 2011

[3] Infineon Technologies: XMC4000 family; User´s manual; Infineon Technologies, Germany, 2012

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Major changes since the last revision

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