AN201317

S29GL-N (32 Mb/64 Mb) Package Routing Guide

AN201317 provides a general routing guide for packages (substrate and/or lead frame) designed with S29GL-N, 32 Mb and 64 Mb, die.

1 Introduction

This document provides a general routing guide for packages (substrate and/or lead frame) designed with S29GL-N, 32 Mb and 64 Mb, die.

This document does not eliminate the need for customer signal integrity/power delivery simulations. Customers should use Cypress provided IBIS models for signal timing/crosstalk simulations.

2 Signal Descriptions

The following table describes various pads used in the S29GL-N die.

Signal/Supply Pad Name	Description
A21-A0	Address inputs
DQ7-DQ0	Data I/O
CE#	Chip Enable Input
OE#	Output Enable Input
WE#	Write Enable Input
ACC/WP	Program Acceleration input/Hardware Write Protect input
RD/BY	Ready/Busy input
BYTE#	Selects 8-bit or 16-bit mode
RST#	Hardware Reset input
$V_{CC}Q$	Output Buffer Power
V_{CC}	3.0 volt only single power supply
V_{SS}	Device ground

3 Signal Groupings

The following table describes various signal/supply groupings to assist in package routing/signal integrity simulations.

Signal/Supply Group	Description
A21-A0	Address inputs
DQ7-DQ0	Data I/O
CE#, OE#, WE#	Control signals
ACC/WP, RD/BY, BYTE#, RST#	Miscellaneous
$V_{CC}Q$, V_{CC}, V_{SS}	Supply

4 Supply Routing Guidelines

We recommended that you meet or exceed the following supply routing recommendations:

- Provide a dedicated V_{CC} ball for V_{CC} pad.
- Provide a dedicated $V_{CC}Q$ ball for $V_{CC}Q$ pad if using $V_{CC}Q$ functionality (Models 1 and 2).

- Provide at least two dedicated V_{SS} ball for flash. All V_{SS} balls should be shorted together in the substrate.
- Maintain a low inductance and resistance path from supply pad (V_{CC}, V_{SS} or $V_{CC}Q$) to solder ball.
- Keep path inductance for each of the supply nets (from each supply pad to its solder ball) ≤3 nH.
- Keep path resistance for each of the supply nets (from each supply pad to its solder ball) ≤100 mΩ.
- Except for necking/bondfinger breakout region, maintain supply (V_{CC}/$V_{CC}Q$/V_{SS}) trace width □100 µm (wider the better).
- Route V_{CC} and/or $V_{CC}Q$ close to V_{SS} trace (regardless of the bondwire location) to maintain V_{CC}–V_{SS} and $V_{CC}Q$–V_{SS} inductance loop constant. In general, a 50 µm separate between V_{CC}/V_{SS} supply traces is ideal, whenever possible.
- Select V_{CC} and V_{SS} solder ball location next to each other on the ball map.
- In Models 1 and 2 (where V_{IO} where $V_{CC}Q$ is bonded out) V_{CC} trace should not be routed next to $V_{CC}Q$. Provide V_{SS} isolation traces (150 µm minimum width as much as possible) to avoid V_{CC} noise coupling onto $V_{CC}Q$ and vice-versa.
- While doing layer transitions in a BGA substrate use dual vias as much as possible to reduce via current crowding.

5 Signal Routing Guidelines

We recommended that you meet or exceed the following signal routing recommendations:

- Maintain all DQ routing within ±1 nH of each other. Limit DQ routing to ≤5 nH.
- Maintain all address routing within ±1 nH of each other. Limit address routing to ≤7 nH.
- Maintain all DQ routing within ±1 nH of WE#. Maintain all address routing within ±2 nH of /WE.
- CE# and OE# routing should be limited to ≤7 nH.
- All other signals should be routed as short as possible and kept ≤10 nH.
- As much as possible, maintain via count on all signals within a signal group (DQ and address only) similar.

6 Multi-chip Package Routing

If S29GL die is used along with other (non-flash) dies in a single MCP, the following routing recommendations should be followed in addition to those in *Supply Routing Guidelines* and *Signal Routing Guidelines*.

- Keep flash V_{CC}/$V_{CC}Q$/V_{SS} separate from other die/interface V_{CC}/$V_{CC}Q$/V_{SS} (routing as well as solderball/pin allocations).
- It maybe possible to share V_{SS} between Cypress flash and PSRAM die (if present) provided PSRAM speed does not exceed flash speed. Controller V_{SS} can only be shared if it pertains to flash interface only. Do not share V_{SS} between different interfaces (e.g. DDR and flash).
- Provide V_{SS} shielding between flash traces/supplies and other interface supply/signal traces (150 µm minimum trade width).
- If signals are shared with another die such as PSRAM/controller, the following general routing rules should be used:
  - All address/inputs should be routed in Y configuration. Maintain the overall inductance from pad to ball within guidelines specified in *Supply Routing Guidelines* and *Signal Routing Guidelines*. However, the fork lengths going to both dies should be electrically matched (provided both dies have similar input capacitance. If they have different input capacitance, IBIS simulations need to be performed to determine fork lengths).
  - All DQ topologies need to be simulated to provide adequate topology (daisy chain or Y). However, it is recommended that flash path inductance from signal pad to ball/pin follows guidelines specified in *Supply Routing Guidelines* and *Signal Routing Guidelines*.

Document History Page

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Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	05/18/2010	Initial version
*A	4994031	MSWI	10/29/2015	Updated in Cypress template
*B	5844198	AESATMP8	08/04/2017	Updated logo and Copyright.

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