AN201303

Verifying Flash Operability

AN201303 provides information for verifying flash operability and guidance to determine if a system level issue can be isolated to a flash related fault.

1 Abstract

Cypress flash devices are used in many different market segments; some of these markets like Automotive, Aerospace, Networking, and others provide high reliability end products. Many times high reliability markets require thorough analysis, understanding and, corrective action for any identified module failure to mitigate its re-occurrence. This document provides information for verifying flash operability and guidance to determine if a system level issue can be isolated to a flash related fault.

2 Verifying Basic Flash Operability

The following provides a basic guide for verifying flash operability. For the purpose of these discussions it is assumed that the subject design has proven basic functionality and the intent is to determine if a system level issue can be isolated to a flash related fault in terms of Read, Erase, or Program. Prior to discussing any system or device level analysis, the subject design's basic configuration should be understood in terms of the flash hardware and software configuration and operating environment.

2.1 Basic SOC / Flash Configuration

The basic flash configuration and accesses are fundamentally defined in terms of being parallel NOR (asynchronous, page, or synchronous accesses) or SPI flash (Single or Multi I/O). For example, a parallel bus interface between the SOC is typically straight forward but it should be noted if the SOC address bus is accessing the flash using byte, word, or double word access. A Cypress S29GL256S is configured to support word access where the flash address line A0 controls word level addressing. Please reference Cypress's Application Note *Connecting Cypress Flash Memory to System Address Bus* for additional details (http://www.spansion.com/Support/AppNotes/flash_to_sys_addr_bus_an_a0_e.pdf)

The flash operating mode is defined in some cases by a simple pull-up or pull-down tied to a flash input signal. For example the S29GL256P Byte# signal's logic state defines whether the flash read and write accesses are byte or word mode. On the other hand a S25FL129P supports a configuration register used to setup access configurations. Depending on the system requirements, the S25FL129P could be left in default Single I/O Read/Write mode or be reconfigured to support Multi I/O read and write accesses. Please reference the subject data sheet for additional details regarding configuration options and appropriate means to modify configuration setups.

2.2 Flash Operating Environment

Providing the flash an appropriate operating environment is essential and basic to reliable flash start-up and operation. The flash data sheet provides the criteria for proper flash operation, Access timing, along with the Absolute and Recommended Operating Conditions. These basic areas must be met to ensure reliable flash functionality across all operating conditions.

The absolute maximum operating conditions define the electrical and thermal parameters that are never to be exceeded. Exceeding these defined conditions can damage the flash silicon which could compromise the reliability of the device's current or future functional operability. Capturing details concerning what exposures the flash incurs during manufacturing, test, and application usage should be reviewed to assure that the flash Absolute Maximum Operating conditions are not exceeded.

The data sheet also provides the recommend operating conditions for the flash device. Prior to delivery, the flash is fully tested and verified to meet the data sheet specification. Operating the flash device outside the conditions specified in the data sheet could result in access failures including but not limited to read failures, failure to start, or properly completing an embedded operation. It is recommended to verify that a system provides the flash device an operating environment that at a minimum meets the data sheet recommended operating conditions.

The flash AC Operating characteristics define the required timings to access a flash device to perform Read, Erase, or Program operation. Cypress flash data sheets provide detailed timing specifications and diagrams showing the setup and hold conditions for control signals, address and data lines for each type of flash access. One comment along these lines concerns the flash device interfaced to the system controller external bus interface; it is recommended to thoroughly review SOC bus controller timing to insure its minium and maximum timing setups and hold times have been configured to meet the timing requirements for all utilized flash accesses.

2.3 Overview of Flash Basic Operability

The following highlights the basic flash functionality in terms of three fundamental operations: Read, Erase, and Program.

The Read operation enables access to digital data contents of the flash memory array. A particular flash device could support parallel or SPI read modes. A parallel flash may support standard asynchronous, page, and/or synchronous read accesses; while a SPI flash may support Single and/or Multi I/O read accesses in standard, fast, or high performance mode.

The Programming operation sets a bit or group of bits from '1' (erased state) to '0' (programmed state) and can be performed on a bit, byte word, or write buffer basis. For example, a S25FL129P SPI flash supports standard Page Programming or Quad Programming to fill the page buffer. Once the flash device successfully receives a program sequence, the flash initiates an internal programming operation. Program pulses are directed to subject cells to be programmed followed by verification of the cell's charge level using internal references to determine if the cell is appropriately charged. In the case when the cell is not sufficiently charged the process of sending a programming pulse followed by verification is repeated. Note that depending on the particular flash device, standard or accelerated programming may be utilized.

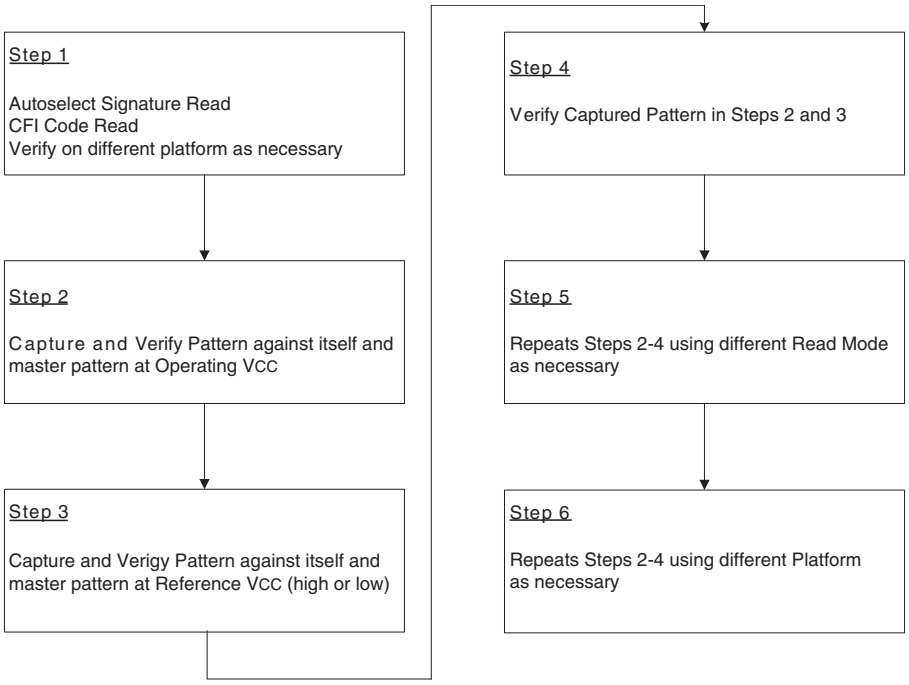
The Erase operation converts bits from '0' (programmed state) to '1' (erase state) and is performed on a sector basis. The erase operation first preconditions the sector and then launches internal operations that complete erasure of a subject sector with maximum reliability. The preconditioning or preprogramming operation internally programs all bits in the sector to a ‘0’ state. The pure Erase operation erases bits in the array followed by Post Erase Conditioning, which optimizes Erase charge state.

It is not recommended to remove the flash V_{CC} Bias during an embedded operation. These actions can leave the flash in an undesired state, which may impede or prohibit proper flash operation. In cases of a power drop out while an embedded operation is in progress, it is recommend to send a HW Reset to the flash while the V_{CC} is valid.

2.3.1 Read Verification

Performing Read verification is the initial step to be completed for all suspect flash failures.

Figure 1. Flow to Verify a Reported Read Failure



The recommended read verification step is to perform a basic read of the flash Manufacturing ID and Device ID. This will determine if the system controller is communicating with the flash device correctly and provides a good indication of basic continuity, appropriate access timing, and voltage bias. If the flash device fails in the original system, it is highly recommended to re-verify these basic Read operations on a reference system such as an industry standard flash programmer and determine if the reference system successfully completes the read verification steps.

If the read verification fails on both systems, then the flash appears to be exhibiting gross operational failures and should be examined for signs of mechanical stress or electrical over stress.

The second step is to determine if the flash array pattern has good stability and integrity under the module operating conditions. This can be completed via capturing and recording any addresses where read failures occur in the flash array.

Example: Master Pattern verses Flash Dump

Always try to capture the “actual” Failure Analysis (FA) data set for the read failure verses relying on high level information like a checksum failure.

- Confirm and document file comparison between the original Master pattern and current flash dump: Example:
  - No mismatches observed
  - Document observed read mismatches
    - address(s) of all confirmed read failures
    - expected and actual data at these locations
  - Capture flash read mode used during observed read failure

(Any flash areas that have been erased and reprogrammed with new data will have mismatch errors against the master pattern.)

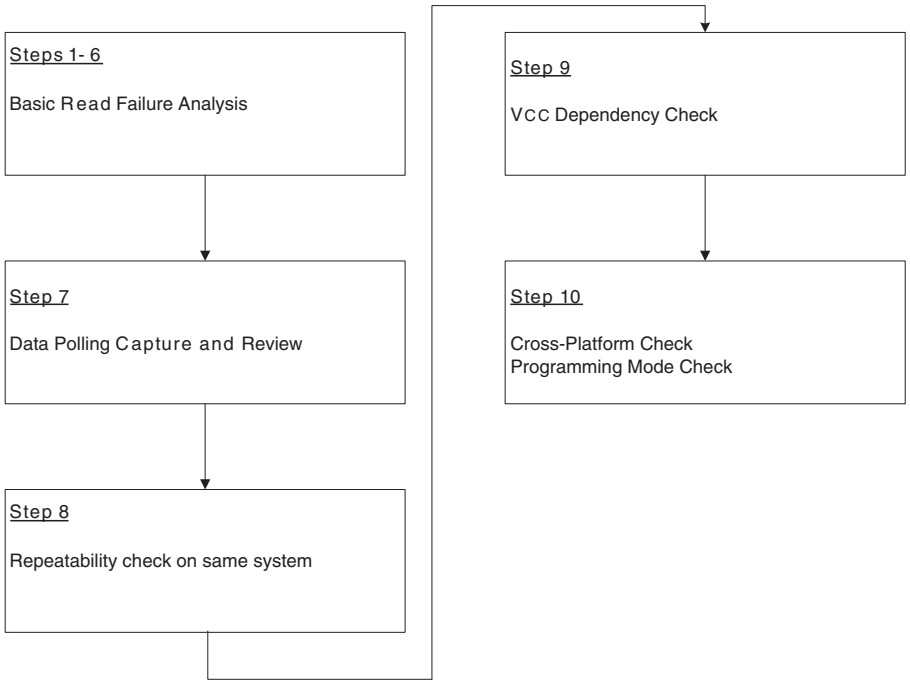
Additional important FA details for suspect Read Failure:

- Sequencing / Programming mode used
- Preconditioning of the parts (e.g. how many cycles, duration of stress etc)
- Operating Conditions – V_{CC} / Timing / Address / Temperature / Repeatability
- Master Pattern for cases where failure is solid (failure is readily repeatable)
- System level information related to how the flash/module has been processed, tested, and application usage

2.3.2 Program Verification

The first step for programming validation is to complete the read verification as outlined in Figure 2.

Figure 2Flow to Verify Program Failure



Once the device is shown to have good read integrity it is essential to understand the system programming algorithm, any block protection, and time out constraints. Is the system using an auto timer with no register checks or periodic register polling for program operation status? To determine additional detail for a programming failure, it is useful to monitor the status bit or status register at the point of failure.

For example, the S25FL129P's status bits WIP and P_ERR indicate if the Program Operation completed successfully or if there was an error.

Reading the Status Register WIP bit after sending a program command provides insight into whether the device successfully accepted the programming command. In instances where P_ERR = 1 (Program Error) is observed during a program operation is a significant indication of a device fault. The reliability of the programming operation should be verified across the flash V_{CC} range.

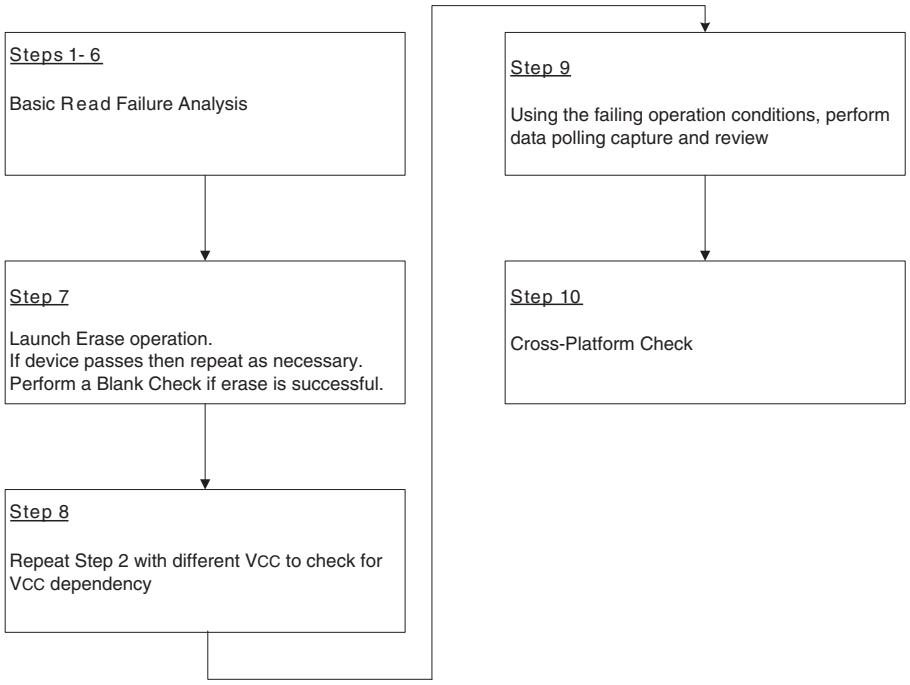
Additional important FA details for Suspect Program Failure:

- Programming Algorithm and mode used
- Note customer verification scheme: timeout vs. polling
- Failing Sector and Addresses if possible
- Status at time of failure
- Preconditioning of the parts (e.g. how many cycles, duration of stress etc)
- Operating Conditions – V_{CC} / Timing
- Repeatability
- Master Pattern (useful when exact failing address cannot be provided and part does not fail outgoing QA CKBD pattern during CCAR analysis)
- System level information related to how the flash/module has been processed, tested, and application usage

2.3.3 Erase Verification

The first step for programming validation is to complete the read verification as outline in the previous Section 2.3.1, *Read Verification* on page 3.

Figure 3. Flow to Verify Erasure Failure



Once the device is shown to have good read integrity it is essential to understand the system Erase algorithms, any block protection, and time-out constraints. Is the system using an auto timer with no register checks or periodic register polling for Erase operation completion and error status? To determine the nature of any Erase failure, it would be very useful to monitor the state of the status bits at the point of failure.

For example, the S25FL129P status bits WIP and E_ERR indicate if the Erase operation completed successfully or if there was an error.

Reading the Status Register after sending an Erase command to determine if the erasure is in progress provides insight into whether the device successfully accepted the Erasure command. In instances where E_ERR = 1 (Erase Error) is observed during an Erase operation is a significant indication that there is a device fault.

The Erasure operation should be checked to determine if there are any V_{CC} dependencies.

Additional important FA details for Suspect Erasure Failure:

- Failing Sector.
- Status at time of failure
- Note customer verification scheme: timeout vs. polling
- Preconditioning of the parts (e.g. how many cycles, duration of stress etc)
- Operating Conditions – V_{CC} / Timing / Address Sequencing
- Repeatability
- System level information related to how the flash/module has been processed, tested, and application usage

3 Summary

This previous information provides the user with a high level and step by step means to verify flash operability in terms of the flash's fundamental Read, Erase, and Program operations. After performing a thorough analysis and it is determined the flash device is not functioning as expected, the failure analysis details should be captured in terms of the observed failing operation (Read, Erasure, or Programming).

Document History Page

Document Title: AN201303 - Verifying Flash Operability Document Number: 002-01303				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	08/17/2010	Initial version
*A	5009330	MSWI	11/10/2015	Updated in Cypress template
*B	5867936	AESATMP8	08/30/2017	Updated logo and Copyright.

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