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EiceDRIVER™ Enhanced 1EDI30J12Cx

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Application Note AN2013-17 EiceDRIVER™ Enhanced 1EDI30J12Cx
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1 Introduction

The EiceDRIVER™ Enhanced 1EDI30J12Cx utilizes an optimized driving topology called Direct Drive JFET Topology (DDJT) to switch a CoolSiC™ JFET and a low voltage MOSFET in a cascode configuration.

It is available in two package variants: a 150mil wide PG-DSO-16-24 and a 300mil wide PG-DSO-19-4 (see Chapter 2.1). It is designed to drive the discrete CoolSiC™ JFET.

The driver consists of two galvanically separated chips that are interconnected using an Infineon Technologies Coreless Transformer. A description of the two chips can be found in Chapter 2.1.

1.1 Direct Drive JFET Topology (DDJT)

In the classic cascode the normally-off MOSFET is used to switch the normally-on device. This is done by connecting the n-channel MOSFET at the source pin of the JFET and connecting the gate of the JFET to the NMOS source (see Figure 1). The necessary V_{gs} to switch off the JFET is created by the blocking voltage of the MOSFET. This indirect way of controlling the JFET could lead to repetitive avalanche in the MOSFET. Another drawback of this solution is the high stray inductance that is introduced in the JFET gate loop due to the fact that the MOSFET is inside this loop.

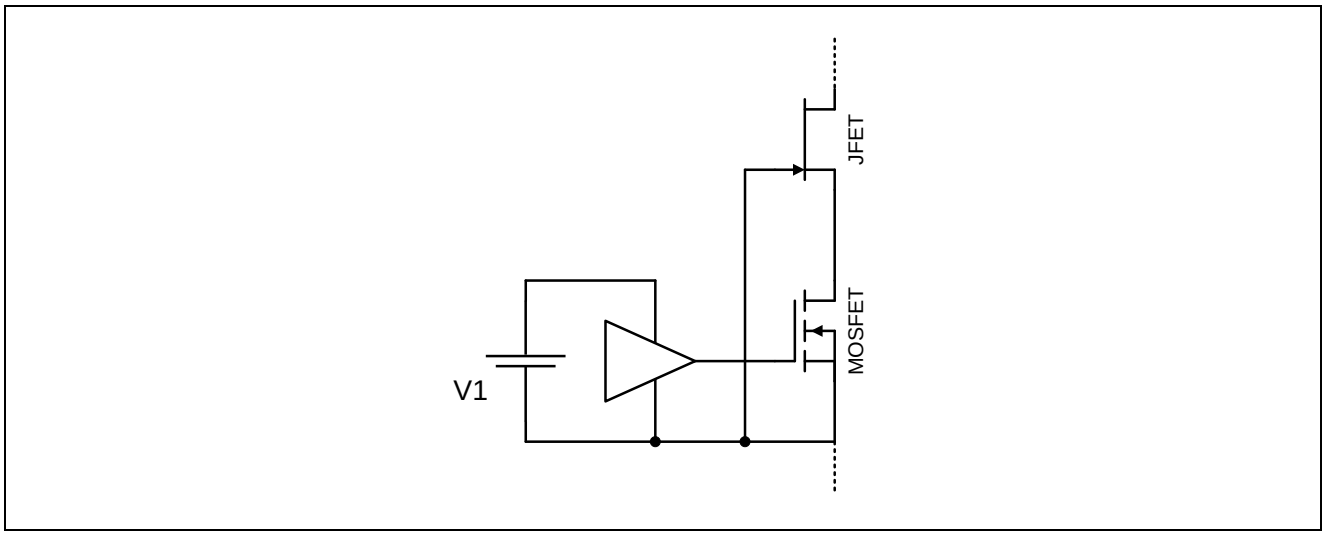


Figure 1 Classic cascode

To avoid these weaknesses Infineon Technologies introduced the Direct Drive JFET Topology (see Figure 2). In this solution the JFET gate is driven directly by the driver. The MOSFET is only used to ensure a safe JFET turn-off stage during startup, shutdown and driver power supply failure in/of the system. When the driver is not supplied the normally-off behavior is ensured by a diode connecting the JFET gate with the MOSFET drain. During normal operation the MOSFET is kept in its on-state while the JFET gate is directly driven by a gate driver. The solution is utilizing a p-channel MOSFET instead of the n-channel MOSFET that is used in the classic cascode solution. This enables the driver to be connected to the common source point and refer all voltages to this potential. Furthermore this solution makes it easier to monolithically integrate both driver stages on one die.

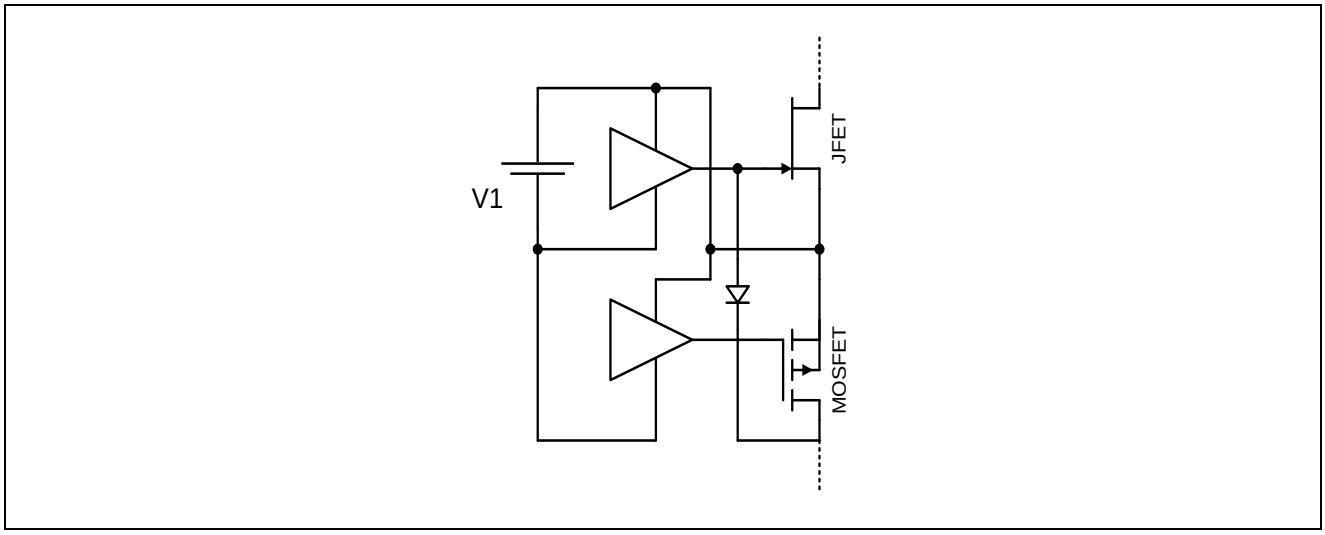


Figure 2 Direct Drive JFET Topology

As a benefit this topology creates less switching losses due to the fact that the MOSFET is switched only once during the startup of the system and is kept in an on-state during normal operation. That is why only the JFET switching losses are accounted for. The additional conduction losses of the LV MOSFET can be kept at a minimum.

A typical realization of a Direct Drive JFET Topology stage can be seen in Figure 3.

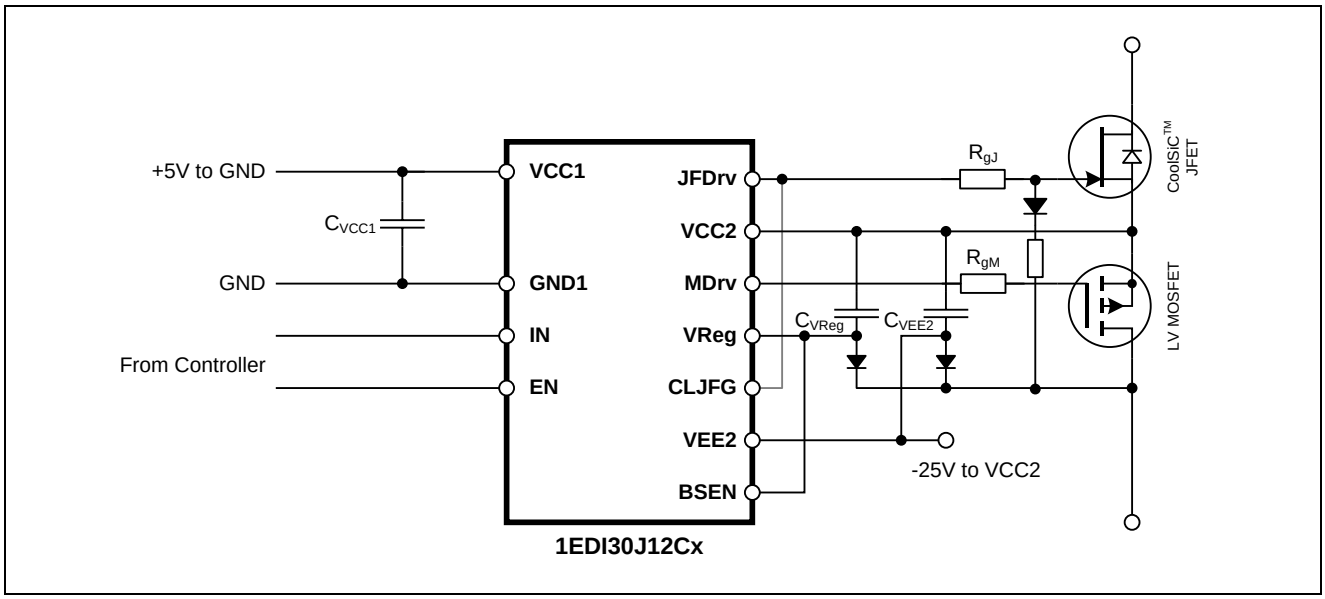


Figure 3 Typical DDJT stage

2 Technical Description EiceDriver™ Enhanced 1EDI30J12Cx

This section of the application note gives a description of the EiceDRIVER™ Enhanced 1EDI30J12Cx. First an overview over the packages and pins are given, followed by a description of the internal blocks.

2.1 Pin Configurations

Figure 4 and Figure 5 show the pin configurations of the two driver package versions.

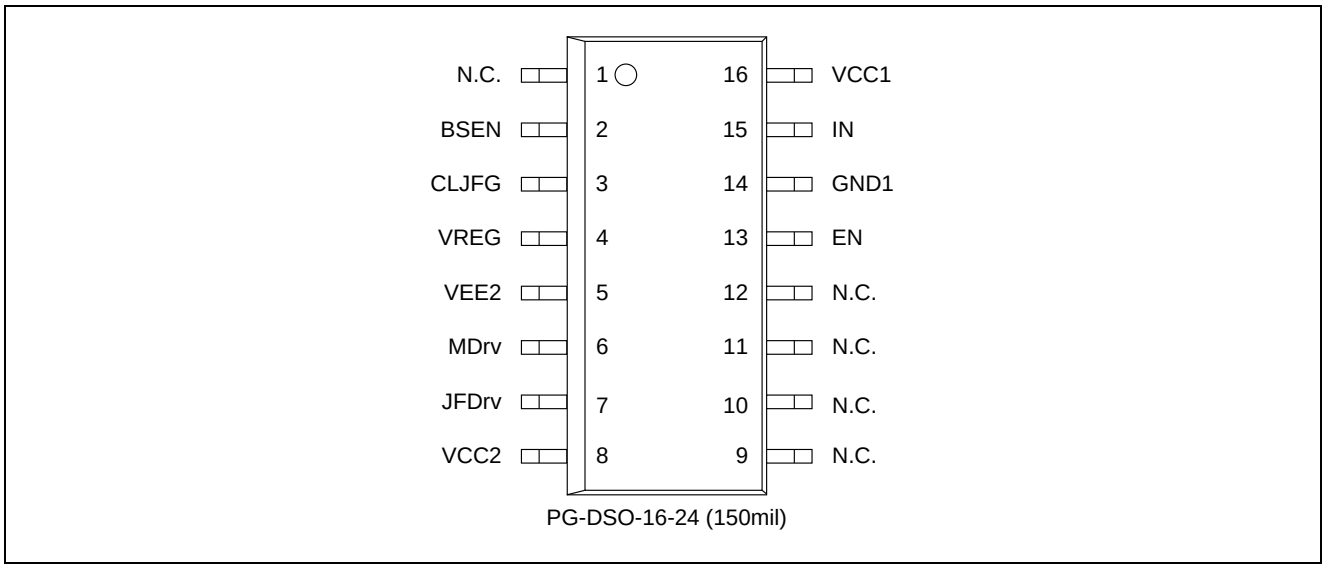


Figure 4 Pin Configuration PG-DSO-16-24 (150mil width)

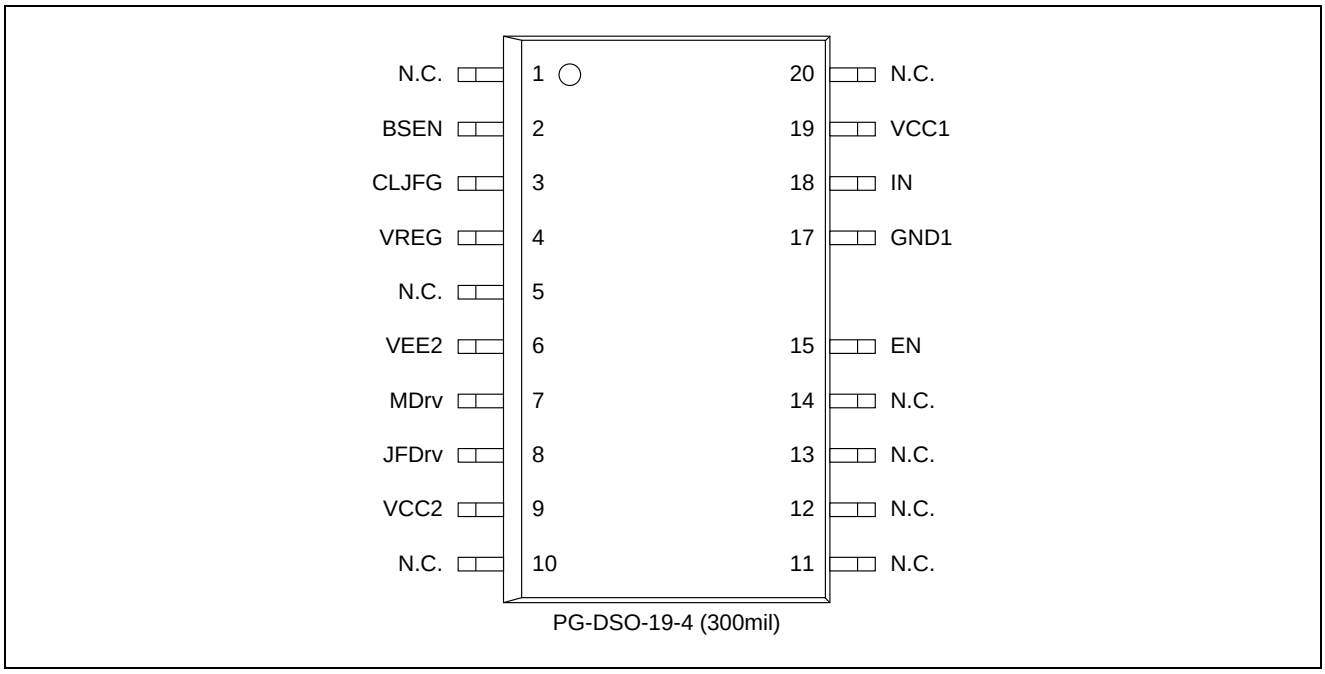


Figure 5 Pin Configuration PG-DSO-19-4 (300mil width)

2.2 Pin descriptions

This section gives a very brief introduction into the functionality of the different pins. Detailed information about maximum ratings and electrical behavior can be found in the corresponding datasheet.

2.2.1 Power Pins

Due to the galvanic isolation of the two chips it is necessary to supply the input side as well as the output side of the driver separately.

The input side is supplied via the VCC1 pin and referred to the ground pin (GND1).

The output side supply is connected between VCC2 and VEE2. This supply is related to VCC2 and VEE2 is the negative potential.

There are several ways to actually connect the auxiliary supply on the output side. Specifics about the different topologies will be discussed in a section 4.

Table 1 Power pins

Pin	Typ. values[1]	Description
VCC1	4.75 V – 17.5 V	Powering the input side of the driver.
GND1	0 V	Ground pin. All voltages on the input side are referred to this reference.
VCC2	0 V	Reference level for the output side of the driver. Connected to the common source potential of JFET and PMOS
VEE2	-19 V – -28 V	Output side supply pin. Voltages in the range of -19 - -22 V lead to a decreased PSRR. To ensure that small ripples in the power supply do not disturb the driver a capacitor is placed between this pin and VCC2.
VREG	-19 V	VREG output pin. -19 V output from the internal linear regulator. To ensure a smooth operation a decoupling capacitor is placed between this pin and VCC2.

[1] These values represent the typical values taken out of the datasheet. Please refer to the corresponding datasheet for verified and updated values!

2.2.2 Logic & Output pins

Table 2 Logic & output pins

Pin	Direction	Description
IN	IN (input side)	A PWM signal is applied here. This signal is transmitted over the Coreless Transformer to the JFDrv pin (output side) if the signal at the EN pin is high and the UVLO (Under Voltage Lock-Out) of both chips is released.
EN	IN (input side)	Enables the driver. Only when a 'high' signal is applied to this pin a transmission over the Coreless Transformer can occur.
JFDrv	OUT (driver side)	Gatedriver output for the CoolSiC™ JFET. This PWM signal is following the signal on the IN pin.
MDrv	OUT (driver side)	Gatedriver output for the low voltage MOSFET. After startup and in normal operation this driver drives a constant signal to keep the MOSFET on.
CLJFG		Reserved; keep this pin connected to JFDrv or leave the pin unconnected and floating
BSEN	IN/OUT (driver side)	If connected to VREG bootstrapping is disabled. If connected to VCC2 bootstrapping is enabled. An optocoupler can be connected between BSEN and VCC2 to relay a bootstrapping UVLO event to the controller. Additional information on bootstrapping can be found in the sections 4.4and 5.8.

2.2.3 Not Connected Pins

Several pins in both packages are not connected internally. It is strongly recommended to leave the solderpads unconnected and floating and not connect these pins to any potential on the PCB. These pins should not be connected together.

The reason for this is to use the maximum creepage/clearance isolation distance the IC is designed for, outside and inside of the IC.

3 Block Description

The driver is built up of two separate Si-chips that are interconnected with an Infineon Technologies Coreless Transformer. An overview can be seen in Figure 6.

The input side chip consists of a linear regulator, the Under Voltage Lock-Out (UVLO) logic and the Coreless Transformer (CT) transmitter.

The driver side chip consists of the receiving end of the Coreless Transformer, a logic block, an UVLO logic block and a linear regulator. Furthermore there are two driver stages and some accompanying logic. To ensure a safe off state in any situation a diode with a current-limitation resistor is already integrated in the driver.

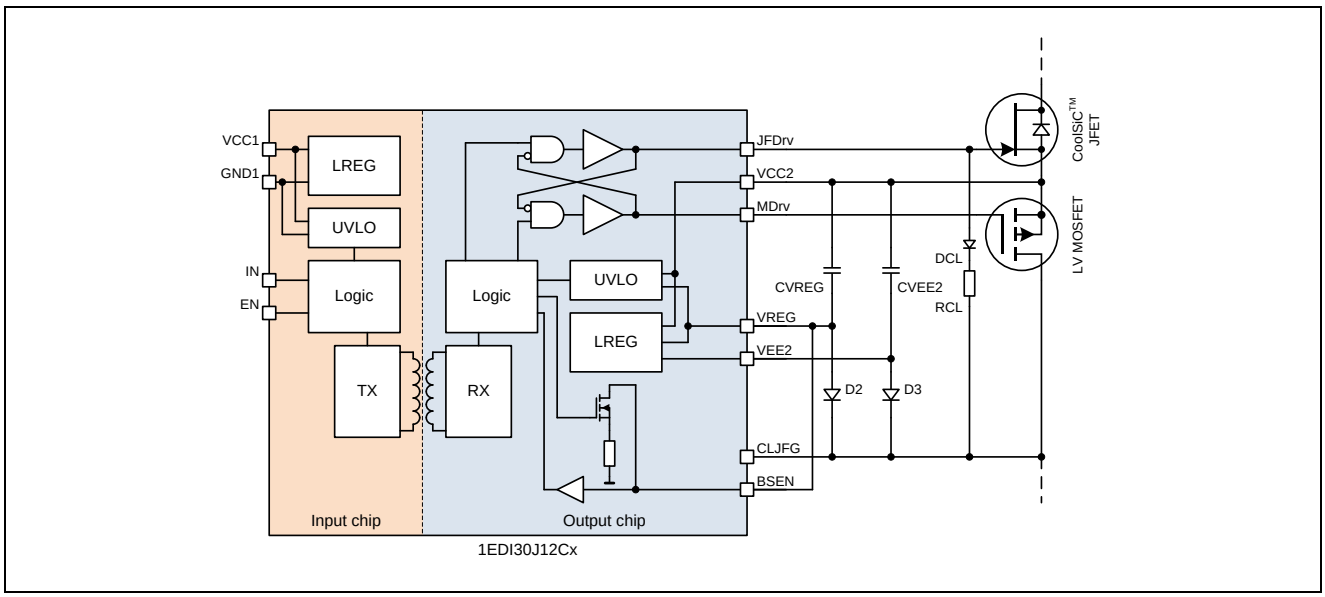


Figure 6 1EDI30J12Cx block diagram

3.1 Input Side

3.1.1 Supply Pins: input side

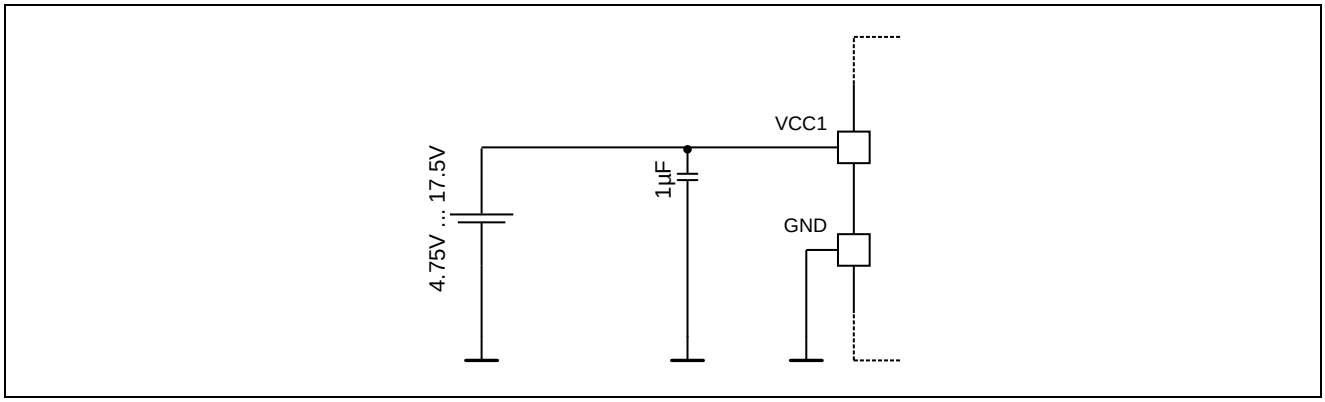


Figure 7 Input side supply pins (VCC1, GND)

The input side is supplied by the voltage applied to the VCC1 pin (4.75 V – 17.5 V). To filter any possible disturbances a decoupling capacitor should be placed near the VCC1 pin. (see Figure 7)

3.1.2 Linear Regulator & Under Voltage Lock-Out (UVLO)

The supply voltage is used by the linear regulator to supply the input side with the needed internal voltages.

As soon as the input voltage reaches more than 4.75 V the Under Voltage Lock-Out (UVLO) releases and the input side is ready for operation.

3.1.3 IN/EN input stages

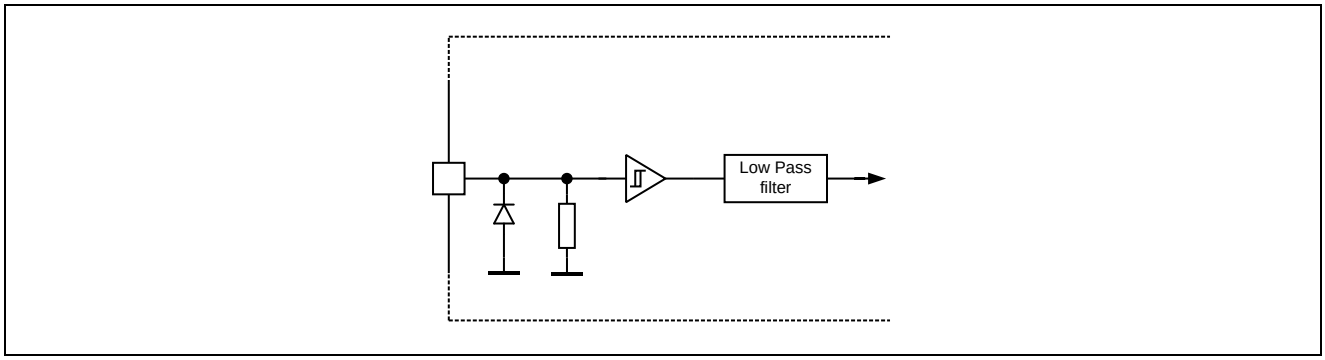


Figure 8 IN/EN input stage

A schematic representation of the input stages is shown in Figure 8. An ESD diode is placed at the pad to protect the pin against ESD discharges. A pull down resistor is placed near the pad as well to pull the potential at the pin down in case of a signal interruption or bad soldering to ensure that the JFET is being switched off.

The Schmitt-trigger is setting its output to low when the input signal is below 1 V. As soon as the level is reaching 2 V the output is set to high. This enables the driver to be connected directly to any micro controller or IC that is utilizing LSTTL logic level signals.

The absolute maximum voltage allowed at the pin is 18 V. The threshold of the signals however remains constant. Voltages above 18 V can lead to destruction of the device and must never be applied.

The signal is negated after the Schmitt-trigger and is passed on to the Input Noise Filter. The minimum pulse width is 40ns. Pulses that are shorter than this limit are ignored and are not relayed to the logic block.

In disturbed environment please keep in mind, that every signal larger than the input filter time of 40 ns is handled from the driver IC as a correct input signal regardless of the signal source, e.g. interference or PWM-signal form µC. It has to be made sure of that any interference on the signal is kept low enough that the distortions do not trigger the Schmitt-trigger unintentionally. Even though filtering is done internally the integrity of the signal can be further improved by adding a RC-filter close to input pins. If used, this filter has to be designed carefully due to the time delay that is automatically created. Therefore the identical filter has to be placed at all driver stages in the system.

3.2 Logic block

The logic block is checking the IN and EN signals and is relaying the necessary information to the Coreless Transformer transmitter. As soon as the EN signal is high, the logic block enables the transmission of the IN signal over the CT.

If the UVLO is triggered due to a drop at the power supply VCC1 the logic block is sending a shutdown sequence over the CT. The gate of the JFET is being pulled low until the UVLO releases again. The same procedure is triggered when the signal applied to the EN pin is being pulled low.

3.3 Coreless Transformer

The Coreless Transformer is a reliable galvanic isolator utilized in many of Infineon Technologies HV gate drivers. It is capable of transmitting the gate control signals from the input to the output side within a very short propagation delay (typ. 80 ns) while still maintaining a high isolation capability and common mode transient immunity. The transmission of the signal is realized by inductive coupling. Therefore no optical transmission is utilized and no photo diode aging can occur.

The sender is located on the input chip, the receiver and the transformer coils are located on the output chip.

The functional isolation voltage is +/- 1200 V. All voltages including spikes and transients have to stay within this voltage range for proper operation. The common mode transient immunity of the transformer is 100 V/ns. The input to output capacitance of the driver is typically 2.9 pF for the PG-DSO-16-24 and 2.6 pF for the PG-DSO-19-4.

3.4 Driver Side

3.4.1 Power supply pins – output side

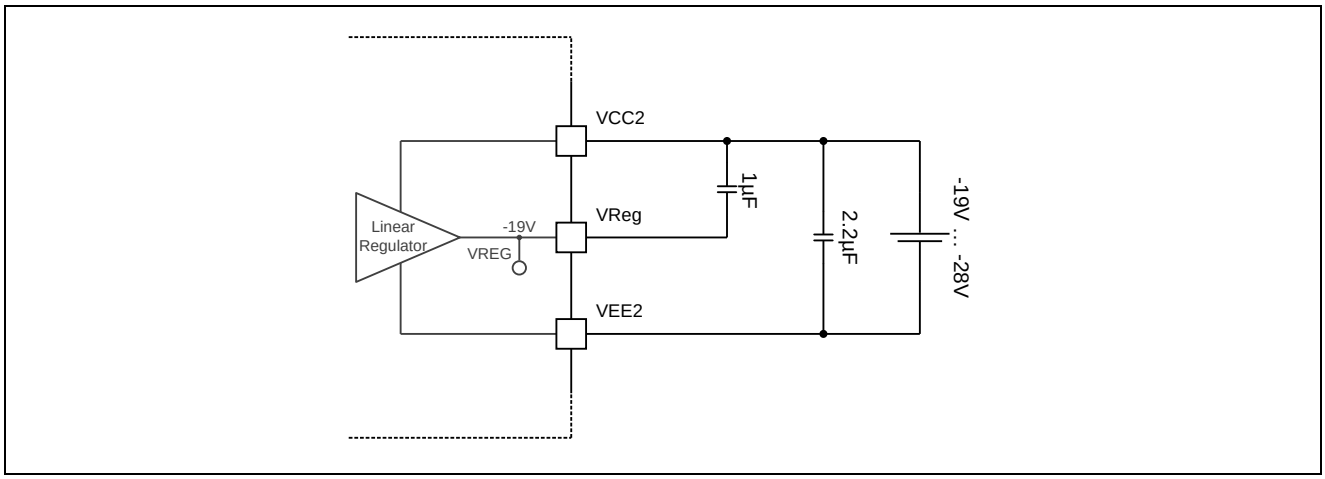


Figure 9 Output side supply pins (VCC2, VEE2, VReg)

Since the CoolSiC™ JFET is a normally-on device a negative voltage is needed to turn off the device. Therefore the output side of the driver needs to be supplied with a negative voltage. This voltage is referred to VCC2 and is applied at the VEE2 pin and decoupled with an external capacitor (see Figure 9, 2.2µF capacitor).

An additional decoupling capacitor is placed at the VReg pin to filter the VReg supply voltage. This supply is created internally by a Linear Regulator. This capacitance must not exceed 2.2 µF to ensure the small signal stability of the internal regulator. If a bigger capacitor is required a value above 10 µF can be chosen. However it has to be made sure of that the capacitance over temperature and productions spread must never be between these boundaries (2.2 – 10 µF).

3.4.2 Linear regulator & UVLO

The Linear Regulator (see Figure 9) is using the VEE2 supply to create the regulated supply voltage of -19 V which is used to supply the internal blocks of the output side.

When powering up the VEE2 supply from 0 V it has to be kept in mind that the linear regulator has a maximum dv/dt of 125 V/ms (with C_{VReg} = 2.2 µF) or a maximum V_{VEE2} minus V_{VReg} dropout of -12 V. To ensure that the regulator is not stressed above its limit the external power supply at VEE2 must not be faster than this.

The best Power Supply Rejection Ratio (PSRR) can be reached when a voltage lower than -22 V is applied at VEE2. It is possible to short the VEE2 pin with the VREG pin. By doing so the internal regulator is disabled

and the output side can be powered with -19 V directly. In this case the supply has to be very precise: +/-5 % is required to ensure stable operating conditions for the driver. Please refer to chapter 4 for further information on the auxiliary supply options.

3.4.3 Driver stages

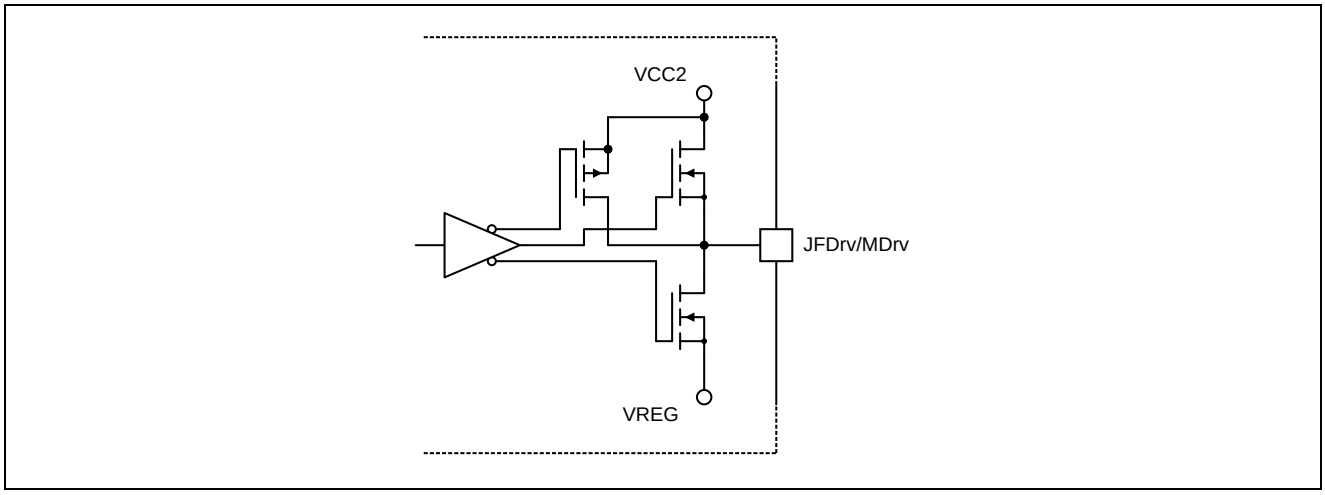


Figure 10 Driver stages JFDrv/MDrv

Two driver stages are implemented on the output side (Figure 10). The driver stage for the CoolSiC™ JFET is capable of sinking and sourcing up to 4 A. This is sufficient to drive a 100 mΩ CoolSiC™ JFET with 100 kHz directly. Depending on the application, f_{SW}, etc. even the 70 mΩ JFET could be driven.

If the design requires paralleled JFETs or faster switching frequencies it is recommended to use a booster stage in between the driver and the JFET. This stage helps to keep the switching losses low. In case of high switching frequencies it also helps to keep the internal power dissipation of the driver low to ensure maximum lifetime.

The driver stage of the MOSFET is capable of sourcing up to 3 A and sinking up to 2 A. Due to the fact that the MOSFET is only switched on once during startup (as long as normal operation occurs) a stronger driving stage for the recommended MOSFET is not required. More information about the recommended MOSFET can be found in chapter 5.4.

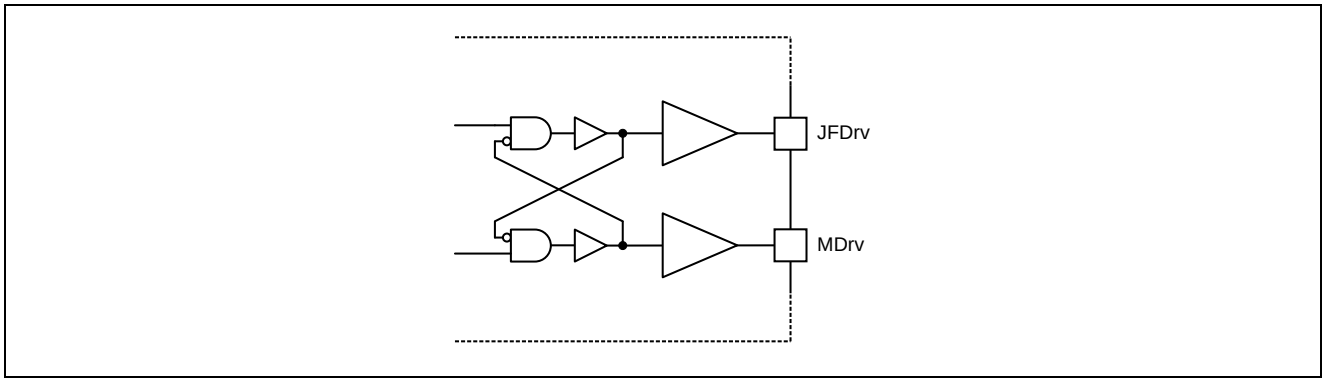


Figure 11 Driver stages interlock

The driver stages have an interlock feature in place (see Figure 11). This ensures that the JFET cannot be turned on unless the MOSFET is turned on. It also ensures that the MOSFET cannot be turned off until the JFET is turned off.

3.4.4 CLJFG Pin

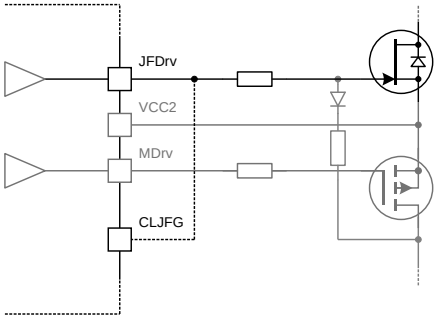


Figure 12 Internal CLJFG diode

The Pin CLJFG is reserved. It should be connected to JFDrv. If this is not possible due to layout reasons it should be left unconnected and floating.

3.4.5 BSEN Pin - bootstrapping mode

To activate the bootstrapping operation the BSEN pin of the 1EDI30J12Cx has to be connected to VCC2. (In normal operation this pin is connected to VReg.)

In normal operation the driver is activated as soon as the VReg supply voltage reaches -16.9 V. At this point the MOSFET is switched on permanently and the JFDrv potential is following the control signals coming from the Coreless Transformer.

If the bootstrapping mode is active a second Under Voltage Lock-Out (UVLO) threshold is activated. In this case the driver is active as soon as VReg reaches -9.5 V. As long the VReg potential is between -9.5 V and -16.9 V the driver is switching both MOSFET and JFET every time a turn-on/off signal is reaching the output side. As soon as the supply reaches -16.9 V the MOSFET is turned on permanently and only the JFET is switched.

As long as the supply is between the two UVLO levels, the propagation delay is enlarged by the time it takes the MOSFET to switch. This leads to the situation that the duty cycle and the dead time between high-side and low-side switching signal must be adapted to compensate for the MOSFET charging time. (See Figure 13)

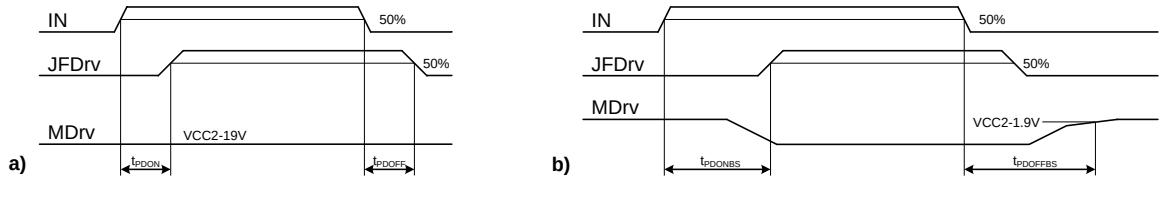


Figure 13 Timing of IN to JFDrv, a) normal mode, b) bootstrap mode

In this case it is also helpful if the controller would prolong the on-time to lengthen the energy transfer period.

This special operation mode can be indicated to the controller by placing an optocoupler diode between VCC2 and BSEN. In this case the driver is signaling the optocoupler as long as the driver remains between the two UVLO thresholds. This is done by sending pulses that are corresponding to the switching signal through the optocoupler diode.

A simplified schematic of this block can be seen in Figure 14.

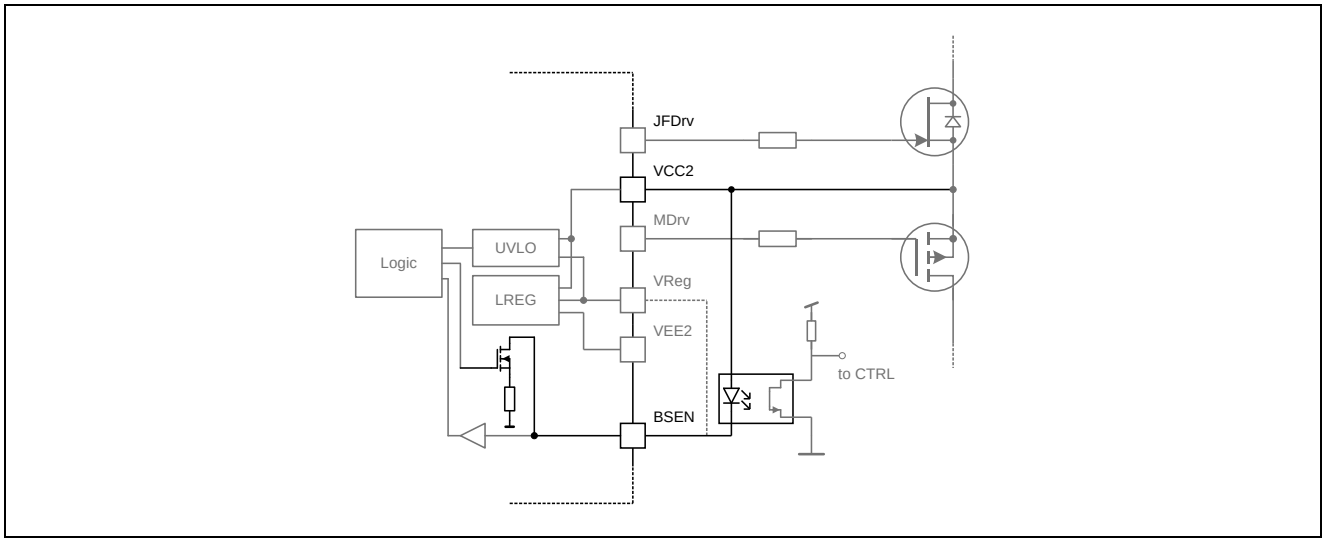


Figure 14 BSEN circuit

4 Auxilliary Supply Options

This section describes the possible auxiliary supply options for the output side of the driver. The auxiliary supply of the input side is not described in detail since it is a typical positive supply with a positive voltage between +5 V and +17.5 V.

The power supplies in the following pictures are depicted as directly connected batteries. It is however important that the used power supplies do not short circuit in case of a power supply failure or when the power supply is turned off. In that case the p-channel MOSFET would be shorted and the system cannot be safely turned off via the clamping diode.

4.1 Isolated floating supply

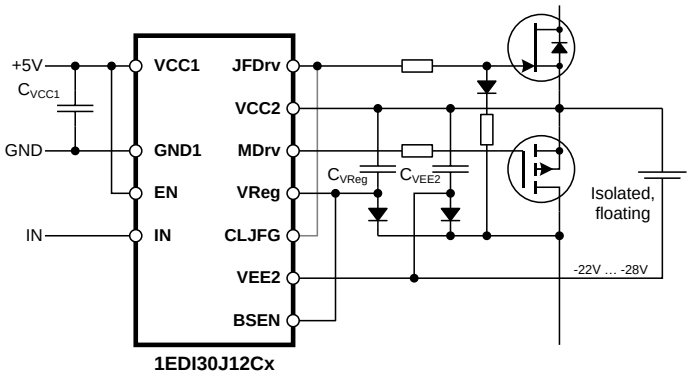


Figure 15 Aux. supply - isolated floating

The normal configuration of the auxiliary power supply for the output side of the 1EDI30J12Cx driver stage can be seen in Figure 15. The isolated and floating power supply is connected between VCC2 and VEE2. The supplied voltage in the range of -22 V to -28 V is fed into the driver and the decoupling capacitor C_{VEE2}.

The internal regulator of the driver creates the necessary -19 V for the nominal operation of the driver stage.

VCC2 acts as a reference potential in this configuration for the whole stage.

4.2 Isolated direct supply

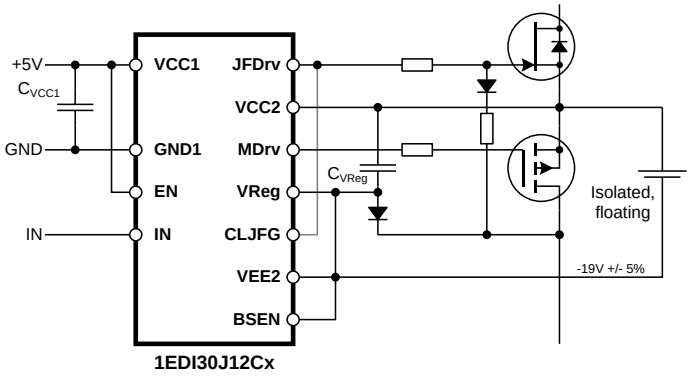


Figure 16 Aux. supply - isolated floating direct

Figure 16 shows a typical driving stage utilizing the isolated direct supply. The supply is connected like the isolated floating supply between VCC2 and VEE2. In this case however the VReg and VEE2 pins are shorted. This deactivates the internal regulator that creates the regulated voltage of -19 V. Therefore no second decoupling capacitor and diode are necessary.

However, in this configuration the auxiliary power supply has to create the -19 V directly. Therefore it needs to be precise enough to only allow a ±5% DC supply voltage deviation including load and line regulation. Otherwise the correct functionality of the driver cannot be guaranteed.

4.3 MOSFET drain related supply

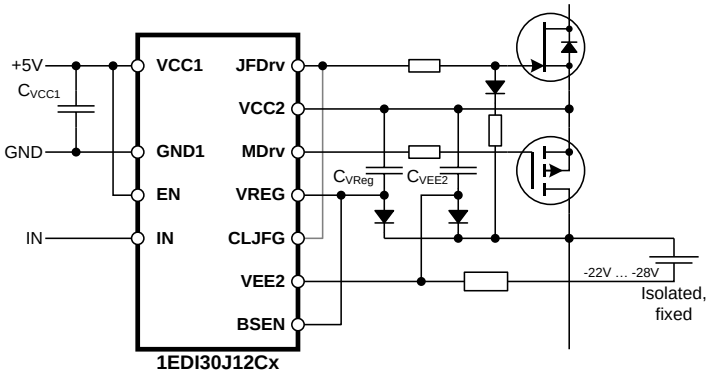


Figure 17 Aux. supply – MOSFET drain related

Another way to power the 1EDI30J12Cx driver stage is shown in Figure 17. In this case the auxiliary power supply is connected between the CLJFG pin (the MOSFET drain) and VEE2 pin.

Since the auxiliary power supply is not connected to the reference node of the driver stage (VCC2) an additional resistor is needed between the power supply and the VEE2 pin. This resistor limits the current coming from the supply. 10 Ω or larger is recommended.

When a current is switched by the JFET a voltage is induced in the parasitic inductances of the MOSFET and the surrounding PCB traces which leads to a voltage difference between the reference node of the driver and the supply reference node. To this induced voltage an additional voltage drop is added due to the $R_{DS\ ON}$ of the MOSFET. Due to this changing voltage and the fact that the power supply reference node stays fixed, an additional current might be fed into the driver. This current can be limited by the mentioned resistor.

The internal regulator is active in this topology. Therefore this circuit requires the second capacitor (C_{VEE2}) again; as with the isolated and floating supply (refer to chapter 4.1).

4.4 Bootstrapping supply

In order to spare one isolated power supply per half-bridge it is possible to power the driving stages via bootstrapping. It is also possible to power all high-side driving stages in a full-bridge or B6-bridge with one isolated power supply via bootstrapping.

Contrary to other bootstrapping solutions the power supply is placed on the high-rail (DC-link+) due to the negative supply voltages used.

When powering the system via bootstrapping the isolated power supply is connected to the JFET drain (high-rail). The power is transferred to the high-side stages via a bootstrap diode (D_{BS_HS}) and current limiting bootstrap resistor (R_{BS_HS}). As a bootstrap capacitor C_{VEE2_HS} is used (see Figure 18 for the high side driver). In this way all the high-side driving stages in a full-bridge or B6-bridge can be powered.

To power the low-side via bootstrapping a cascaded bootstrapping is needed (see Figure 18). In a first stage the power is transferred to a dedicated bootstrap capacitor C_{BS} via a bootstrap diode (D_{BS}) and a current limiting resistor (R_{BS}). In the second stage this energy is then transferred to the low-side decoupling capacitor C_{VEE2_LS} via the bootstrap diode D_{BS_LS}.

The bootstrap diodes, one for the high side and two for the low side driver are used to isolate the high- from the low-side. These diodes have to be able to block the full DC link voltage. They have to have a high peak current rating so that the bootstrap capacitor can be charged quickly. Additionally a low reverse recovery charge is also recommended. During the evaluation phase of this topology a STTH112 diode (V_{RRM} = 1200V, $I_{F(AV)}$ = 1A) was used. Resistors placed in series with the diodes are used to limit the current to the maximum current rating of the diodes.

When using this supply option the BSEN pin needs to be connected to VCC2 (in all other supply options this pin is connected to VReg). When connected to VCC2 the drivers UVLO level of the output side is changed to -9.5 V.

A more detailed description of the bootstrapping operations can be found in chapter 5.8.

A schematic of the whole topology can be seen in Figure 18.

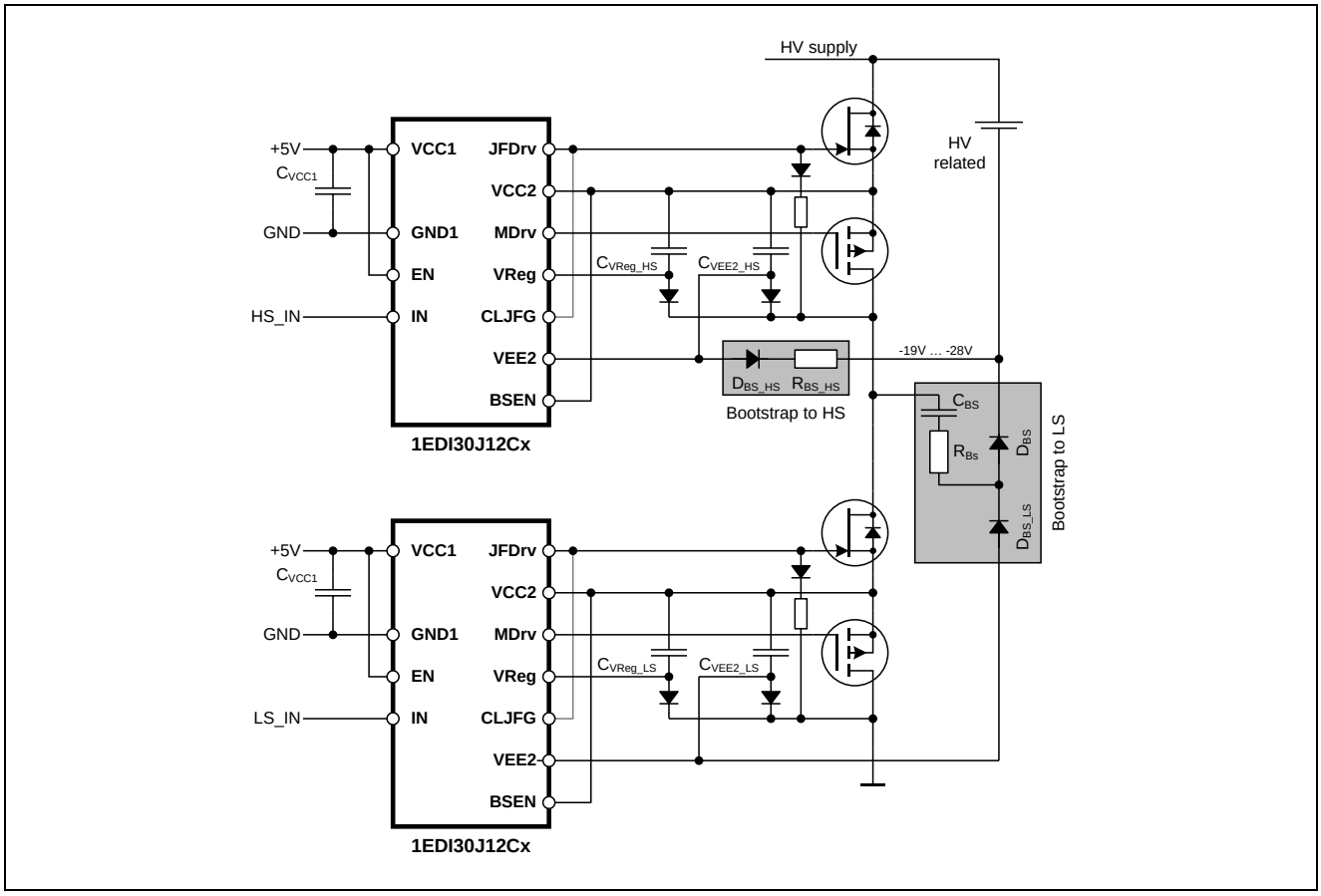


Figure 18 Aux. supply – cascaded bootstrapping

5 Application & BOM recommendations

This chapter describes necessary components and their recommended values in the application.

5.1 JFET gate drive options

There are two main ways to drive the CoolSiC™ JFET with this driver: it is possible to drive the JFET directly or with an additional booster stage.

5.1.1 Resistor

The simplest way of driving the JFET is to use a simple gate resistor (R_G) between the driver and the switch.

To limit any kickback that might come back to the driver it is not recommended to use a 0 Ω resistor or no resistor at all. The resistor should have at least 1 Ω. The exact value is depending on system and EMI requirements.

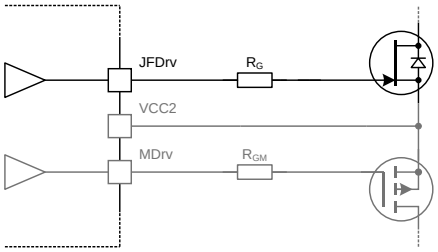


Figure 19 Gate drive circuit - R_g

This circuit can be used for the 100 mΩ as well as a 70 mΩ JFET with a maximum switching frequency of 100 kHz.

5.1.2 Emitter follower

If a higher switching frequency is desired or paralleled JFETs are required a booster stage (push-pull stage) has to be placed between the driver and the JFET.

One simple circuit would be an emitter follower stage.

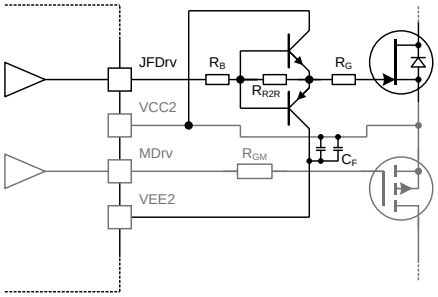


Figure 20 Gate drive circuit – emitter follower as booster stage

The resistor R_B is required to minimize any potential kickback to the driver. It also limits the current into the bases of the bipolar transistors. The resistor R_{R2R} can be used to have a rail to rail output stage. A value of

several tenths of ohms is recommended here. This value however is again system dependent. If needed a gate resistor R_G can be placed between the JFET gate and the common emitter point. The value of this resistor can be chosen depending on the desired switching speed of the JFET as well as EMI considerations.

As supply for the booster stage the potentials V_{CC2} and V_{EE2} should be used. In this way the internal regulator does not have to power the emitter follower in order to lower the power dissipation in the driver.

The capacitors C_F are used as decoupling capacitors.

5.1.3 Miller Clamp

It is also possible to use a Miller Clamp circuit to clamp the JFET gate during the turn off phase to VCC2. A possible Miller Clamp circuit can be seen in Figure 21.

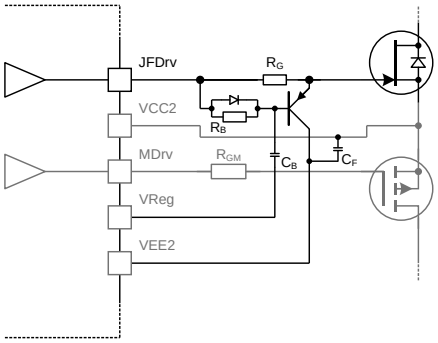


Figure 21 Gate drive circuit – Miller Clamp

This Miller Clamp circuit is designed to only clamp the JFET gate during the off-phase. Therefor the τ of the low pass created by R_B and C_B should be long enough that the clamping starts after the JFET is fully switched. If the τ is too small the Miller Clamp would act like a booster stage during the switching off event which is not the desired functionality here.

Keep in mind that the capacitor C_B should be kept small so that it is only a fraction of the C_{iss} of the CoolSiC™ JFET in order not to increase the power dissipation in the driver.

5.2 Capacitor recommendation

For stable operation several capacitors are needed:

Name	Description	Min.	Typ.	Max.	Unit	Remarks
C_{VCC1}	Decoupling cap.	0.1	1.0		µF	Can be chosen according to system requirements
C_{VEE2}	Decoupling cap.		2.2		µF	Can be chosen according to system requirements
C_{VReg}	V_{Reg} cap.	0.22		2.2	µF	See additional text below

These values represent typical values that were used during the evaluation phase with the nominal circuit. If, the ciruit is changed by adding components these values have to be adapted. If for example an additional capacitor is placed parallel to the JFET gate-source capacitor to enlarge the C_{gd}/C_{gs} ratio the C_{VReg} capacitor and then furthermore the C_{VEE2} capacitor might have to be enlarged to compensate for the higher gatecharge. In this case a booster stage might have to be used as well!

If a higher capacitance than 2.2 µF at the V_{Reg} pin is needed, a capacitor with a value larger than 10 µF can be used. The value of the C_{VReg} capacitor however must, under all conditions (over production spread as well as temperature), never be between 2.2 µF and 10 µF. Otherwise the stability of the internal regulator cannot be guaranteed.

5.3 Maximum regulator drop out voltage

During the power supply startup phase it is necessary to limit the maximum slope of the driver side power supply (V_{EE2}) to 125 V/ms (with C_{VREG} = 2.2 µF) or a maximum V_{VEE2} minus V_{VReg} dropout of -12 V. This limitation is given so that the internal regulator can follow the external supply and the drop between V_{VEE2} and V_{VReg} is not too high. Otherwise the strain on the internal regulator is too big and the regulator could be damaged.

5.4 PMOS recommendation

As p-channel MOSFET an Infineon BSC030P03NS3 G is recommended. This transistor was used in all evaluations of the Direct Drive JFET Topology. It comes in a PG-TDSON-8 package. This MOSFET has a V_{DS} of -30 V with an $R_{DS(on)}$ of 3.0 mΩ. The maximum current I_D is -100 A.

The driver is capable of switching up to two of these MOSFETs in parallel if a lower $R_{DS(on)}$ is required. This limitation is relevant for the power losses of the MOSFET driver in Bootstrapping mode, when the PMOS's are switched on and off with each cycle during the time the VReg supply has not reached the Under Voltage Lock Out level (typ. 16.9 V).

5.5 MOSFET gate resistor

As with the JFET, a gate resistor (R_{GM}) between PMOS and driver is recommended to protect the driver against any feedback coming back from the gate. Since the PMOS is not switched in normal operation the value is not very important. During the evaluation phase of the circuit a resistor between 2 Ω and 5 Ω was used.

5.6 Clamping diode

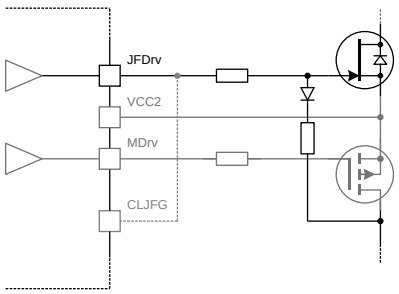


Figure 22 External clamping diode

The clamping circuit is built up by a diode and an accompanying series resistor that are connected between the MOSFET drain and the JFET gate.

The ripples created by the parasitic inductances during high di/dt events in the switching path are defining the necessary voltage class of the clamping diode. In most layouts an 80V BAS16 diode will suffice. The induced voltage should be checked in the layout to be sure that blocking capability is not superseded.

To limit the current going through the diode a resistor in series to the diode is recommended. The value should be chosen according to the maximum diode current. In order not to violate the maximum diode current or to limit the current so that the switching behavior of the JFET isn't affected by the voltage ringing over the PMOS related stray inductances.

5.7 Necessity of external bypass diodes

In the schematic depicting the Direct Drive JFET Topology (Figure 3) two diodes are connected between the capacitors C_{VEE2} and C_{VReg} and CLJFG (PMOS drain). In normal operation these diodes are not active and not used. They are only necessary in case of reverse startup (the DC-link is present before the auxiliary supply is active – see datasheet 3.2.3) or a failing auxiliary power supply.

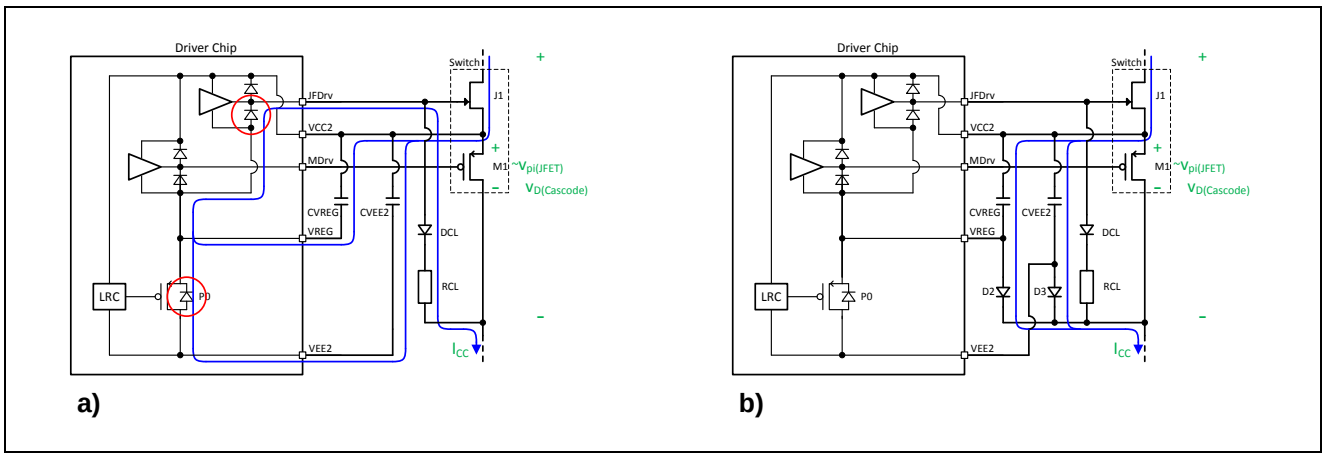


Figure 23 External bypass diodes

If the auxiliary power supply fails the JFET is pinched off by the MOSFET via the clamping diode DCL. Since this voltage only reaches the pinch-off threshold a small leakage current is still flowing through the device. This current charges the capacitors C_{VEE2} and C_{VReg}. Figure 23a shows the path the current takes during this failure scenario. It can be seen that the current flows through an ESD diode as well as the body diode of an internal pass device. These diodes (marked with a red circle) are not designed to handle this current. To prevent the main current flowing through the driver, the current is bypassed via two external diodes D2 and D3 (see Figure 23b). In the evaluation phase ES1A diodes were used.

Figure 23 also shows that the both the C_{VEE2} and C_{VReg} capacitors are charged to the pinch-off voltage during the time the auxiliary power supply is not active. Since both V_{VEE2} and V_{VReg} are rising at the same time and the internal regulator is not active, the dV/dt limitation of 125V/ms for the supply is not relevant here.

This charging of the capacitors however helps the circuit to reach the Under Voltage Lock Out Level faster when the auxiliary power supply it turned on afterwards.

5.8 Bootstrapping

The fact that the capacitors are charged to the pinch-off level is also helpful during bootstrap operation.

In this case it helps to minimize the time it takes for the driver to reach the UVLO level and continue with normal operation.

The basic functionality of the circuit is already described in chapter 4.4. The following sub chapters are meant to give a more detailed look on the bootstrapping scheme.

5.8.1 How does bootstrapping with the 1EDI30J12Cx work

The basic idea is to transfer the energy that the driver needs for normal operation from the high-side to the low-side. This is done by charging a bootstrapping capacitor C_{BS} to the level of $VEE2_{HS}$ and this capacitor in turn charges the low-side C_{VEE2} to the same potential. Most bootstrapping schemes transfer energy from the low-side to the high-side, the negative supply voltages however require this reversed approach.

As mentioned in chapter 4.4 a secondary UVLO level is activated in case BSEN is connected to VCC2. Without this connection the driver would behave “normal”: if the VReg level is above -16.9 V the driver is deactivated. When the level has reached this threshold the PMOS is turned on permanently and the output side of the driver starts switching the JFET according to the signals received from the input side.

If BSEN is connected to VCC2 the secondary UVLO level is activated: if the VReg level is above -9.5 V the driver output side is disabled. If the level is between -9.5 V and -16.9 V the output side already starts to switch the JFET. However the MOSFET is switched together with the JFET during the time the power supply stays between these levels. As soon as VReg reaches -16.9 V the PMOS is turned on permanently and normal operation can proceed.

This second UVLO level is specially designed for bootstrapping, so that the driver can start switching even when the power transfer to the low-side has not yet reached the nominal supply voltage.

5.8.2 Necessity of additional bootstrap capacitor

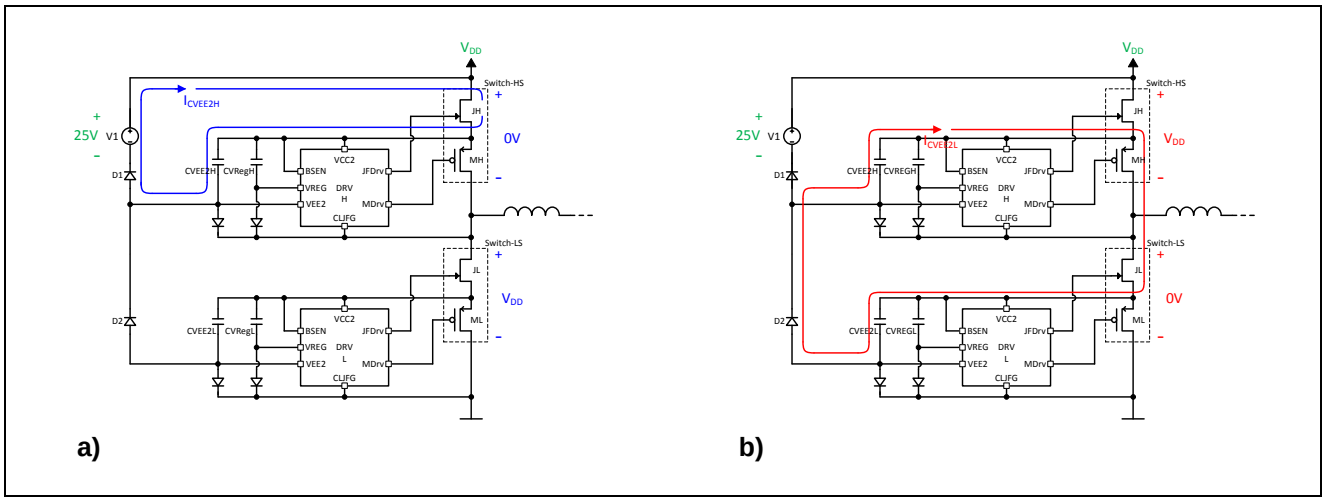


Figure 24 Bootstrapping loop without C_{BS}

Figure 24 shows how the energy is transferred if no additional bootstrap capacitor is used. During the time when the high-side JFET is turned on the capacitor C_{VEE2H} is charged to the voltage of the isolated power supply V1 (Figure 24a). When the high-side is turned off and the low-side is turned on, the capacitor C_{VEE2L} is charged from the capacitor C_{VEE2H} (Figure 24b). This energy transfer is working fine as long as the UVLO threshold is not crossed and the high-side p-channel MOSFET does not switch in conjunction with the JFET: If this would happen the loop in Figure 24b would be broken and C_{VEE2L} cannot be charged any more.

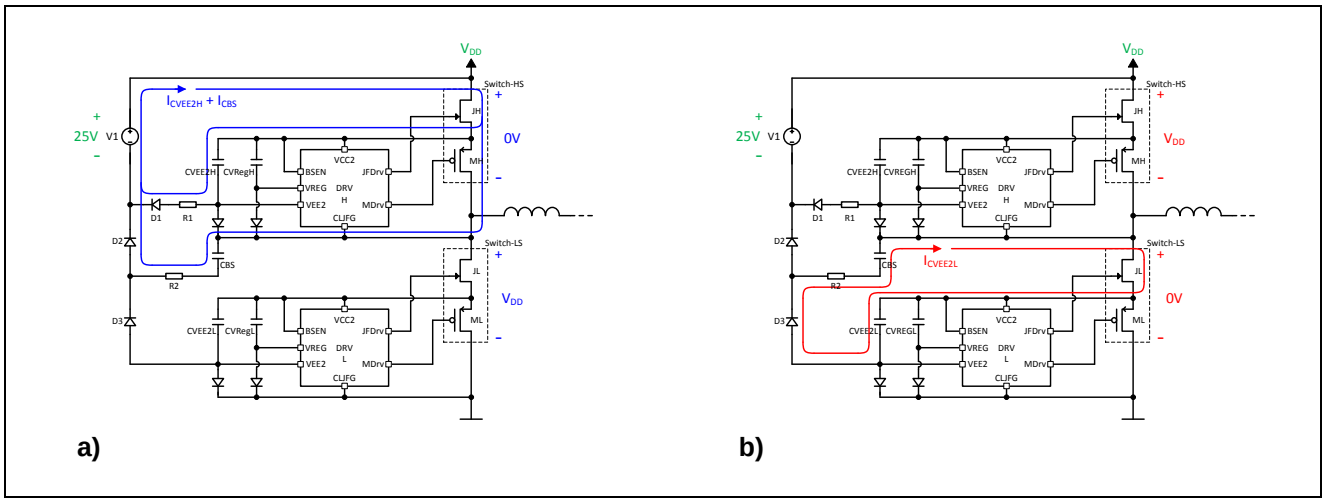


Figure 25 Bootstrapping loop with C_{BS}

Figure 25 shows how this can be avoided. In Figure 25a the circuit is reconfigured so that next to C_{VEE2H} a secondary capacitor C_{BS} is charged at the same time. The energy stored in C_{BS} can be transferred to C_{VEE2L} even if the high-side PMOS is switched together with the JFET (Figure 25b).

Therefor a bootstrapping circuit as shown in Figure 25 is recommended.

5.8.3 Dimensioning of bootstrapping components

For an effective bootstrapping circuit several low cost passive components instead of the expensive low-side isolated power supply are used:

- 1 capacitor
- 3 diodes
- 2 resistors

Capacitor C_{BS}

The capacitor C_{BS} should be larger than the C_{VEE2} capacitors. In that way it is never fully discharged when charging the low-side C_{VEE2} capacitor. The dimensioning is depending on the system requirements. The minimum C_{BS} capacitance should exceed the sum of C_{VEE2} and C_{VReg}.

Diodes

The diodes are placed so that the high voltage at the switching node is blocked.

The diodes have to be able to block the full DC link voltage. Furthermore they should have a high peak current rating to be able to quickly charge the capacitors. They should also have a low reverse recovery charge so that no additional energy is dissipated.

Resistors

The resistors are primarily used to limit the forward current and reverse recovery current of the diodes and in this way ensure that the peak current ratings of the diodes are not violated. It is recommended to use resistors capable of handling the still occurring peak currents.

6 Layout CL & CP

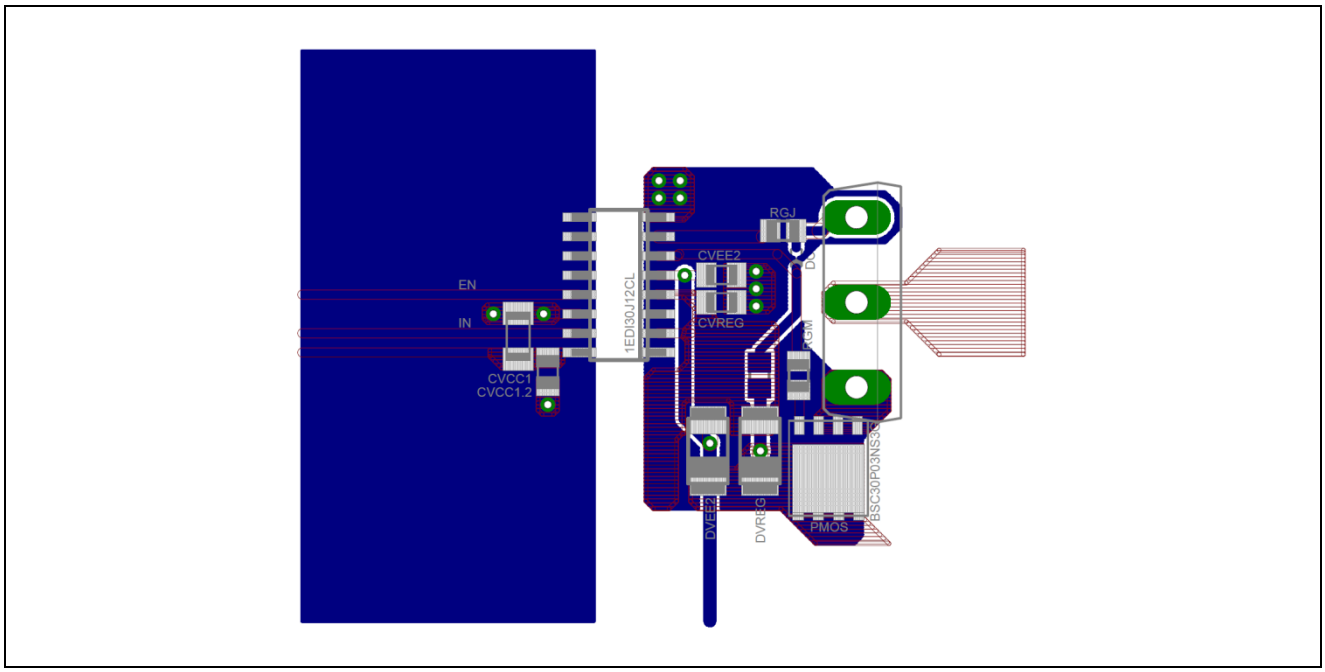


Figure 26 Layout of a typical 1EDI30J12CL driver stage

Figure 26 and Figure 27 show typical layouts of 1EDI30J12Cx driver stages. These layouts are optimized for low parasitics and space efficient design. These layout examples are not proven for mass production and should therefore not be taken 1 to 1 without design rule check and tests according to customer guidelines as they only serve as a guideline.

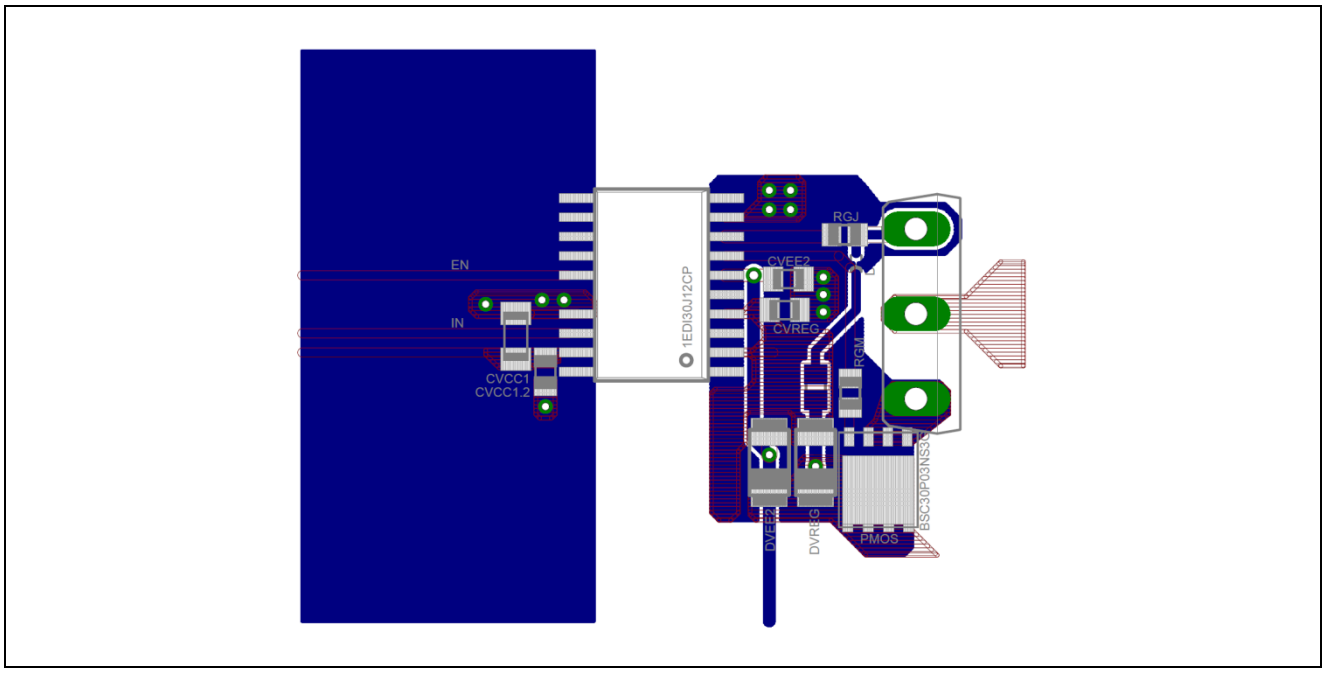


Figure 27 Layout of a typical 1EDI30J12CP driver stage

6.1 Placement priorities

Some aspects have to be kept in mind when designing a 1EDI30J12Cx driver stage:

- The gate loop has to be designed with low parasitics
- All routes should be kept as short as possible to reduce the parasitic inductance
- JFET and PMOS sources should be connected as close as possible
- Place the power supply decoupling capacitors as close to the driver as possible (C_{VReg} has priority over $C_{VEE2)}$
- The control signal has to be clean and not be disturbed by any coupling effects

6.1.1 Reference Layers

To minimize the coupling effects a reference plane should be used. On the input side of the driver this plane should be connected to GND. The output side reference plane should be connected to VCC2. In this way all parasitic capacitances that are built up are in parallel to pre-existing placed and/or parasitic capacitors.

6.1.2 Capacitors

The power supply pins should be connected to capacitors to block any disturbances of the power supply lines. On the input side the decoupling capacitor is placed near VCC1.

On the output side the VEE2 pin as well as the VReg pin have to be connected to capacitors. These capacitors should be placed near the respective pins. If space is at a premium the VReg capacitor has priority since it decouples the internal voltage regulator.

Details on the size of these components can be found in chapter 5.2.

6.1.3 Control signals

The control signals IN and EN should be kept clean of any disturbance. If the integrity of the signal is disturbed the Schmitt-trigger might change the state unwantedly.

Therefor the controller should be placed near the driver stage. If this is not possible the signals might have to be filtered with a RC-filter. The necessity and parameter of this filter will have to be checked on the final design of the application.

6.1.4 Clamping diode

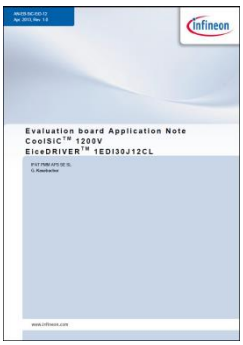
The loop created by the clamping diode and the accompanying series resistor between the MOSFET drain and the JFET gate should be as short as possible to pinch off the JFET as fast and safe as possible.

6.1.5 Gate loop

To minimize any disturbances created by parasitic inductances the route should be kept as short as possible. The gate resistor should be placed near the JFET to minimize ringing and return-on.

For more detailed information on the placement of the components as well as the reason behind please refer to the layout guidelines document.

7 Evaluationboard



The Infineon CoolSiC™ 1200V and EiceDRIVER™ Enhanced 1EDI30J12CL evaluation board is built to demonstrate the functionality of the devices and especially the function of the Direct Drive JFET Topology. A separate Application Note (AN-EB-SiC-EiD-12) is available as well as the prebuilt board itself.

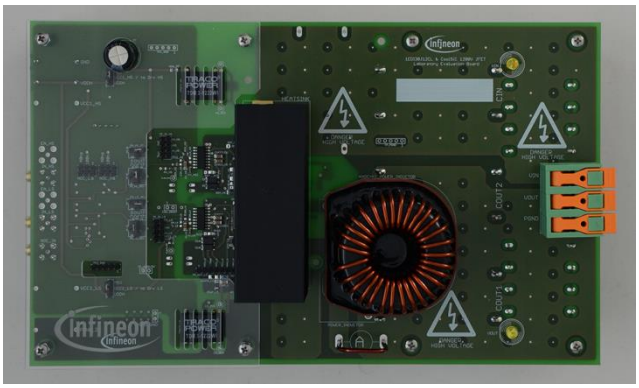


Figure 28 Evaluation board – top view

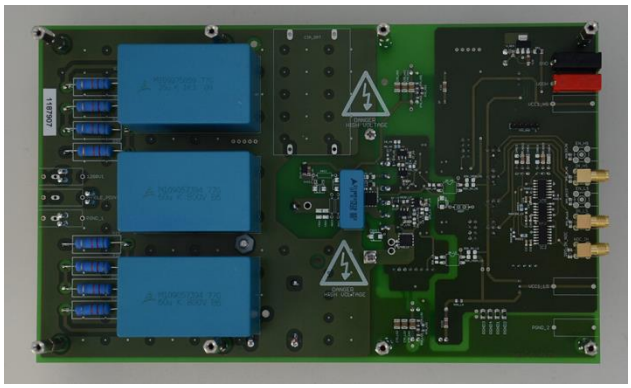


Figure 29 Evaluation board – bottom view

The board is built as a half-bridge and can be configured as buck converter, boost converter as well as high-side buck converter.

Figure 30 Evaluation board – view of JFET and driver

8 References

1. 1EDI30J12Cx Datasheet
2. Evaluation Board Application Note: AN2013-16
3. Layout guidelines 1EDI30J12Cx