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Evaluation Board Application Note CoolSiC™ 1200V EiceDRIVER™ Enhanced 1EDI30J12CL

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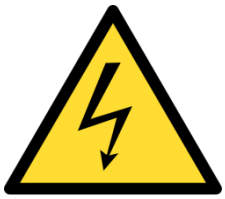
Introduction

This document is intended to give an introduction into the CoolSiC™ 1200V evaluation board.

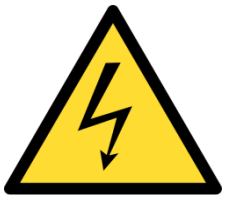
This document is only describing the evaluation board and its functions. For more information about the used **CoolSiC™ JFET** as well as the **EiceDRIVER™ Enhanced 1EDI30J12CL** please refer to their datasheets as well as application notes.

For safe operation please read the whole document before handling the evaluation board!



High Voltage

Dangerous Equipment!



Do NOT touch the board during operation.

Depending on the configuration of the board as well as the chosen supply-voltage, life-threatening voltages might be present!

Even brief accidental contact during operation might result in severe injury or death!

Always make sure that the capacitances are discharged before touching the board.

Only qualified personal are allowed to handle this board!

The board described is an evaluation board dedicated for laboratory environment only. It operates at high voltages. This board must be operated by qualified and skilled personnel familiar with all applicable safety standards.

1 Board overview

This evaluation board was built to test the CoolSiC™ 1200 V JFETs in conjunction with the EiceDRIVER™ Enhanced 1EDI30J12CL.

The board contains two switches that are controlled separately by one driver each. Each driver additionally controls a low-voltage p-channel MOSFET (OptiMOS™ BSC030P03NS3 G). These three devices are building up the Direct Drive JFET Topology.

On this board the components are placed in such a way that they are building a half-bridge circuit.

Additionally to the switching stage a NOC (non overlapping clock generator, dead-time generator) is implanted to ensure that no shoottthrough is possible.

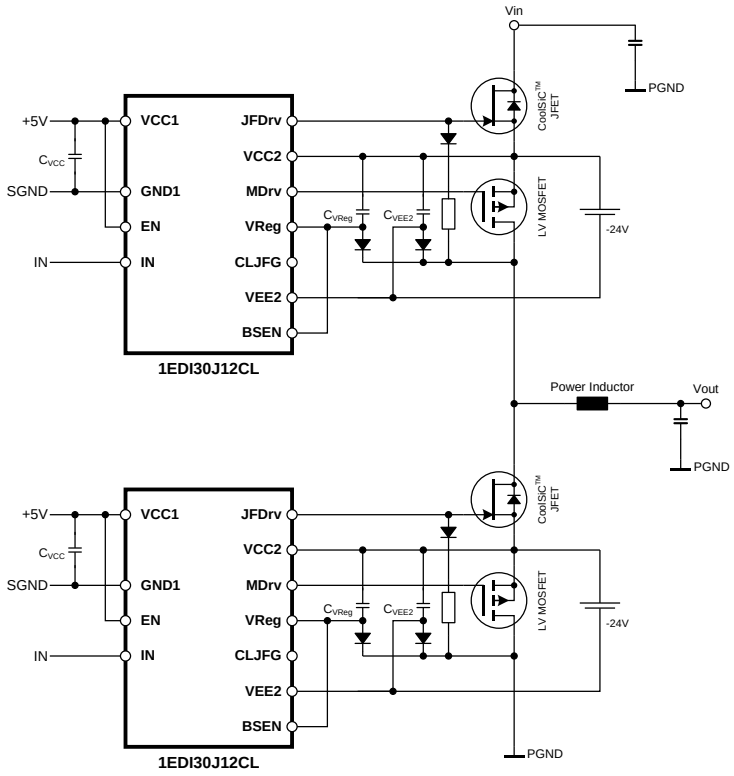


Figure 1 Simplified schematic

This document describes the board and how to handle it during the evaluation phase.

The maximum ratings as well as operating parameters can be found in chapter 2.

Chapter 3 details the board functionality. The best way to measure signals is explained in chapter 5.

Chapter 8 is detailing the first steps to get the board up and running.

It is possible to test several topologies with this board: synchronous buck converter, synchronous boost converter and high-side buck converter. The setups are described in chapter 309.

Information about the different gate drive circuits that can be tested can be found in chapter 10.

The schematic and layout information can be found in the Appendix.

Additional information on the CoolSiC™ JFET and the driver can be found in the corresponding datasheets.

2 Board Specification

2.1 Absolute Maximum Ratings

Absolute maximum ratings are listed in Table 2. Stresses above the maximum values may cause permanent damage to the board and or the mounted devices. Exposure to absolute maximum rating conditions for extended periods may affect board/device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the board or the assembled components.

Parameter	Symbol	Min.	Max.	Unit	Remarks
Input voltage DC	V_{VIN}		1300	V	Referred to PGND[1] [2]
Output voltage	V_{VOUT}		800	V	Referred to PGND[2] Limited by output cap.
Aux. supply voltage	V_{VDDH}	-0.3	18	V	Referred to GND[2]
Control signal NOC_IN	V_{NOC_IN}		7	V	See DS SN74AS04 (part of the onboard NOC)
Control signal IN/EN	$V_{IN\_LS/HS}$ $V_{EN\_LS/HS}$	-0.3	$V_{VCC1\_LS/HS}$ +0.3	V	See DS 1EDI30J12CL
Specification of optional inputs					
Aux. supply voltage LS	V_{VCC1_LS}		18	V	Referred to GND[2]
Aux. supply voltage HS	V_{VCC1_HS}		18	V	

[1] Max. Value is referred to the maximum Voltage of the evaluation board. The CoolSiC™ 1200 V JFET cannot handle this voltage!

[2] PGND and GND are shorted in the standard assembly

2.2 Operating Range

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Input voltage DC	V_{VIN}	-	-	800	V	Referred to PGND[3] Limited by capacitances
Output voltage	V_{VOUT}	-	-	800	V	Referred to PGND[3] Limited by capacitances
Aux. supply voltage	V_{VDDH}	-	12	17.5	V	Referred to GND[3]
NOC_IN low input voltage	$V_{NOC\_IN\ (L)}$			0.8	V	See DS SN74AS04 (part of the onboard NOC)
NOC_IN high input voltage	$V_{NOC\_IN\ (L)}$	2			V	
IN/EN_LS/HS low input voltage	$V_{IN\_LS/HS\ (L)}$ $V_{EN\_LS/HS\ (L)}$			1.0	V	
IN/EN_LS/HS high input voltage	$V_{IN\_LS/HS\ (H)}$ $V_{EN\_LS/HS\ (H)}$	2.0			V	
Frequency control signal	$f_{LOG\_IN\_HS/LS}$		50		kHz	Tested up to 200kHz
Specification of optional inputs						
Aux. supply voltage LS	V_{VCC1_LS}	4.75	5	17.5	V	Referred to GND[3] Direct supply of driver – Jumpers *VCC1_LS_SEL*, *VCC1_HS_SEL* have to be changed; see chapter 0 & 1EDI30J12CL DS
Aux. supply voltage HS	V_{VCC1_HS}	4.75	5	17.5	V	

[3] PGND and GND are shorted in the standard assembly

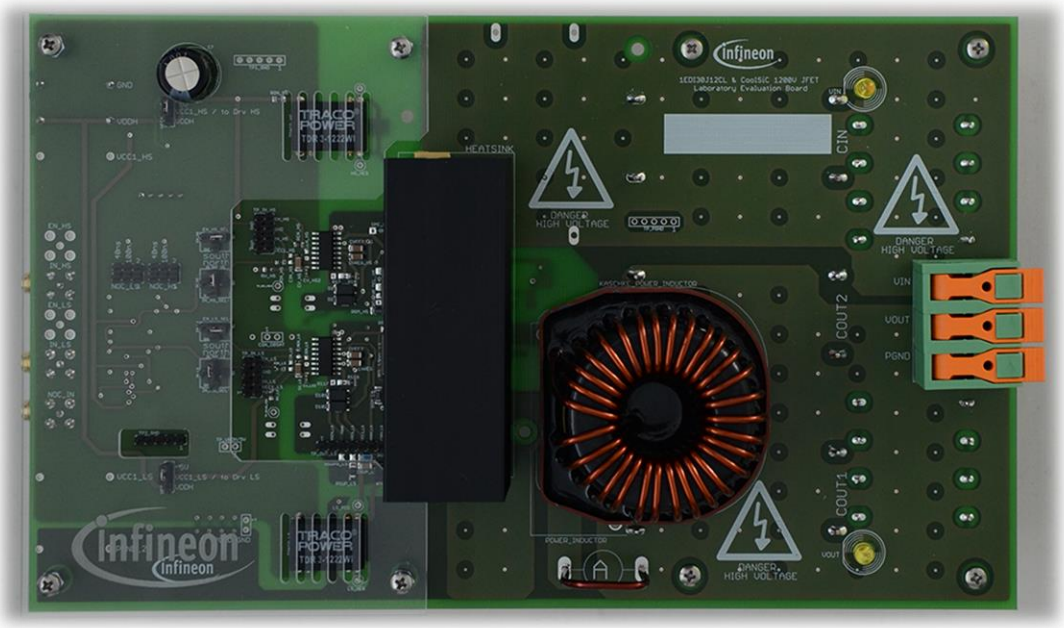


Figure 2 Board overview - top side

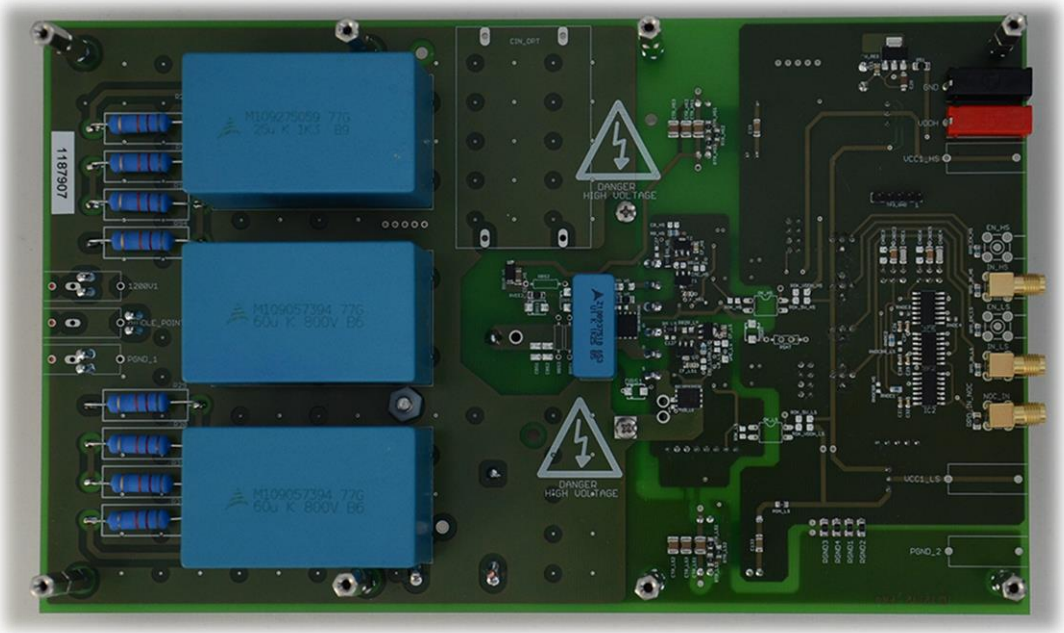


Figure 3 Board overview - bottom side

3 Board functionality

In this chapter the board functionality and connections are described. A full schematic of the board can be found in Appendix A, the layout can be found in Appendix D.

3.1 Connectors & Signals

Figure 4 shows an overview of the evaluation board. The highlighted areas are representing the various connectors with the corresponding chapters in this document.

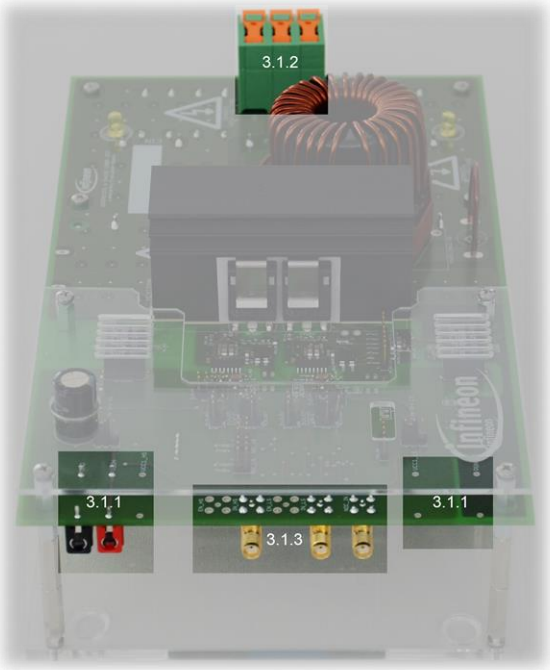
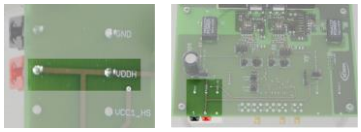


Figure 4 Connector overview

3.1.1 Auxiliary supplies

VDDH 	Supplies the low voltage (LV) side of the board. Should be connected to a 12 V source that is referenced to GND. The needed 5 V supply for the mounted logic ICs is created on the board by a linear voltage regulator.
GND 	Ground potential for the LV side of the board.

Not mounted

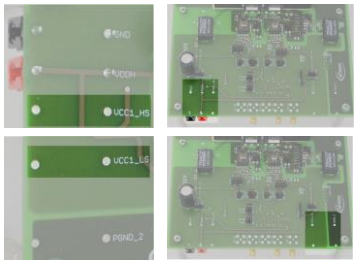
VCC1_HS, VCC1_LS 	Could be used when the HS and LS drivers should have separate VCC1 supplies. Not needed/mounted in standard assembly.
PGND_2 	PGND and PGND_2 are connected together with four 0 Ω resistors, thus this connector is not needed in the standard assembly.[4]

Table 1 Auxiliary supplies

3.1.2 Primary supplies (high-voltage supplies)

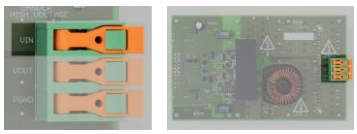
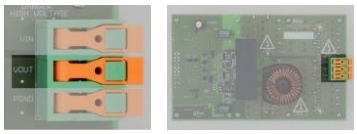
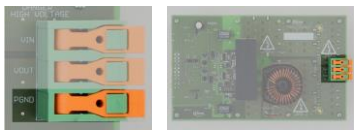
VIN 	HV input connector. The DC link voltage is applied here.
VOUT 	Output pin of the circuit.
PGND 	Power ground. This potential is shorted with GND in the standard assembly. [4]

Table 2 Primary supplies

[4] Please refer to chapter 3.1.4

3.1.3 Control signals

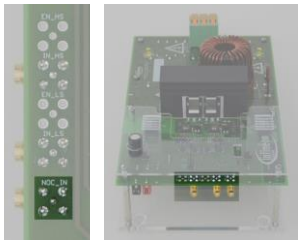
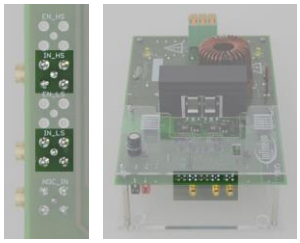
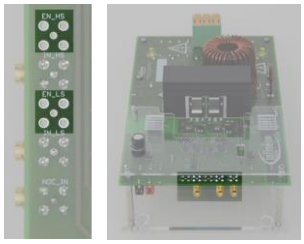
NOC_IN 	Input to the onboard NOC (non-overlapping clock generator) (see chapter 3.4) that generates the complementary control signals for the LS and HS drivers.
IN_LS, IN_HS 	Can be used to provide separate IN signals to the drivers. In this case the NOC has to be disconnected by changing the jumper settings of IN_LS_SEL and IN_HS_SEL (see chapter 3.2) Additionally an external dead-time generation will have to be used.
Not mounted	
EN_LS, EN_HS 	Can be used to enable/disable the drivers directly. In the standard assembly these connectors are not mounted and the EN pins are always connected to 5 V (driver enabled, see chapter 3.2).

Table 3 Control signals

3.1.4 PGND, GND connection

In the standard assembly GND and PGND are connected with four 0 Ω resistors at the bottom of the PCB (*RGND1-4*). If desired the high-voltage side of the board can be isolated by desoldering these resistors.

3.2 Jumper selections

The jumpers on the left side of the board control the signal flow of the IN and EN signals, the auxiliary power supplies of the driver and the NOC.

An overview of the jumper banks can be viewed in Figure 5. During transport the jumpers are covered with an acrylic glass plate which can be removed at any time to access the pinheads.

This plate is not supposed to be a protection against accidental contact!
The board must never be touched during operation!

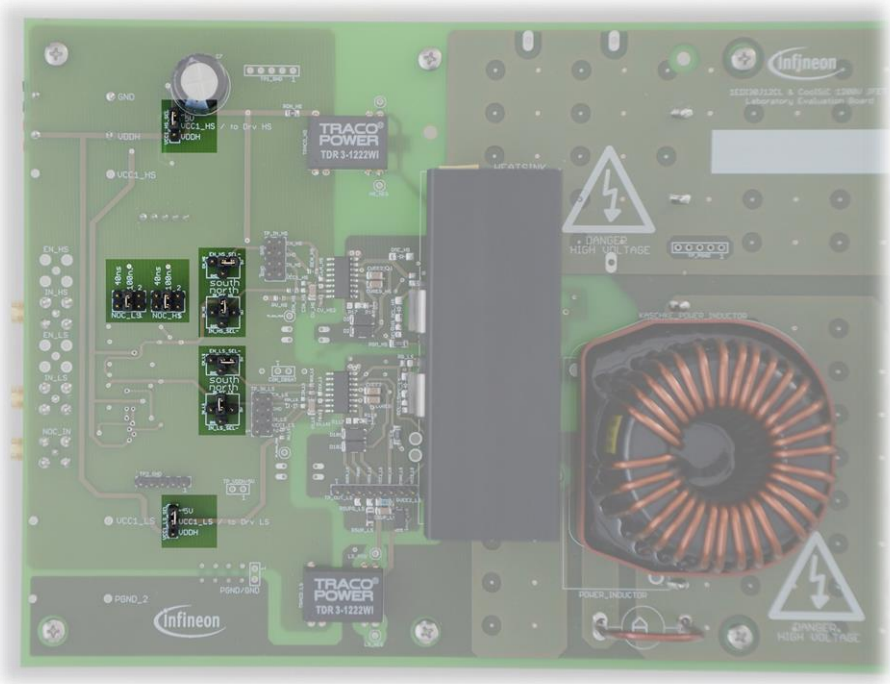
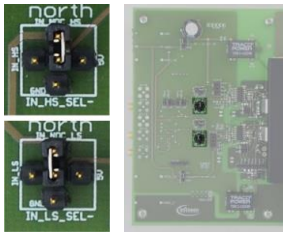
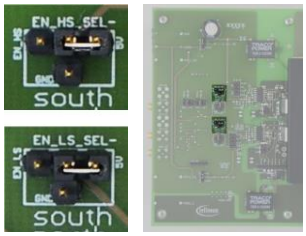
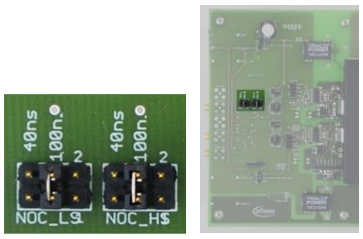
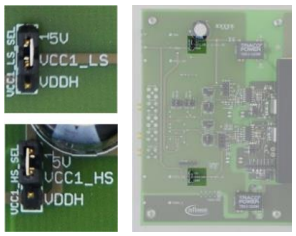


Figure 5 Overview of the jumper banks

Jumper cross **IN_LS_SEL, IN_HS_SEL**	If the jumper is connected *NORTH* (like in the standard assembly) it connects the on-board NOC to the driver inputs. By using the SMA connectors IN_LS/HS the two driver stages can be addressed separately. In that case the jumper will have to be connected to *WEST* (IN_LS and IN_LS). It is also possible to send a continuous low (0 V, GND / connected *SOUTH*) or high (5 V / connected *EAST*) signal to the driver. [5]
	

[5] Please refer to the schematics in the Appendix.

Jumper T **EN_LS_SEL, EN_HS_SEL** 	When connected *EAST* the driver enable (EN) signal is always high (5 V). By changing the jumper it is possible to utilize the EN_LS/HS SMA connectors (not mounted) by connecting *WEST* or constantly disabling the drivers (0 V, GND / connected *SOUTH*). [6]
Jumper row **NOC_LS, NOC_HS** 	These jumpers control the dead-time that is created by the NOC. If the jumper is in the middle position it translates to a dead-time of ~100 ns; using the left position the dead-time is ~40 ns By mounting an additional capacitor at position CNOC3 and CNOC6, different dead-times can be realized. [6]
Jumper row **VCC1_LS_SEL, VCC1_HS_SEL** 	Selection for the drivers input-side power supply. If connected mid-point to high (5 V, std. assembly) the 5 V linear voltage regulator (TLE4264-2G) is used. To use the connectors VCC1_LS and VCC1_HS the jumpers need to be removed. If the jumper is placed between the mid-point and low (VDDH) the supplied voltage at the connector *VDDH* is fed directly to the driver. [6]

[6] Please refer to the schematics in the Appendix.

3.3 Auxiliary supply options

The low power part of the board is supplied via *VDDH*. The recommended voltage is 12 V.
The drivers are supplied with two voltages:

- The supply on the input side of the driver is 5 V or 12 V referred to GND. Either the input side is powered directly from the *VDDH* connector or from a 5V linear voltage regulator (TLE4264-2G). Theoretically it is possible to supply the driver with up to 17.5 V. In that case the jacks *VCC1_LS* and *VCC1_HS* have to be used.
- The output side is supplied with -24 V created by a TRACO POWER TDR 3-1222-WI.

The board is designed to enable the user to test different auxiliary supply options for the output side supply:

1. Isolated floating supply (standard assembly)
2. MOSFET drain related supply
3. Bootstrapping supply

Details about these supply options can be found in the following chapters.

When testing the different power supply variations it is recommended to use the standard synchronous rectification buck converter (see chapter 9.1). This is the simplest and safest topology on the board and is therefore ideal for different tests.

3.3.1 Isolated floating supply

The driving side of the 1EDI30J12CL is supplied with an isolated floating supply. The transformer is connected between VCC2 and VEE2.

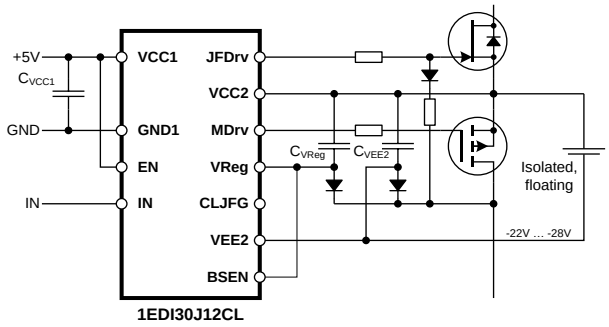


Figure 6 Isolated floating supply

The standard assembly schematic (isolated floating supply) can be viewed in the Appendix B.
To use this supply option, RSUP_LS and RSUP_HS have to be assembled with 0 Ω resistors.

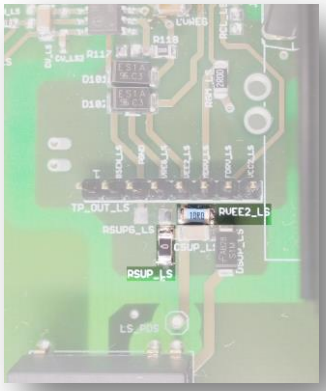


Figure 7 Assembly isolated floating supply - low-side

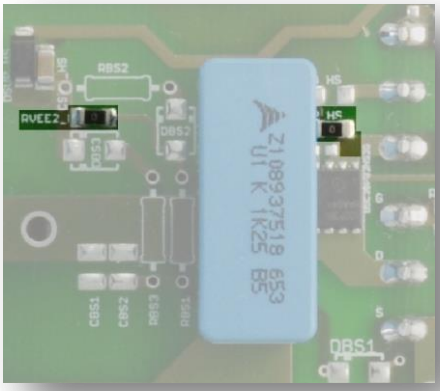


Figure 8 Assembly isolated floating supply - high-side

3.3.2 MOSFET drain related supply

This supply option can only be used for the low side driver of the half-bridge. In this case RSUP_LS must not be mounted; instead RSUPG_LS is used. (Please refer to the schematic in Appendix A and Appendix B)

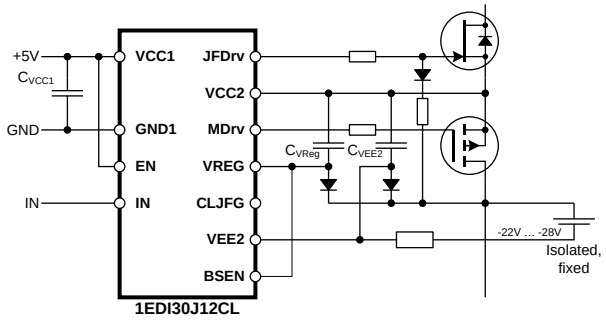


Figure 9 MOSFET drain related supply

For this supply option RVEE2_LS has to be mounted with at least a 10 Ω resistor to decouple VEE2 from the power supply. Due to the PMOS related stray inductance the VEE2 capacitor has a different reference node (VCC2) compared to the power supply (PMOS drain). When the JFET is switching high currents, high voltage can be induced over the PMOS related stray inductance. To decouple the VEE2 capacitor from this voltage a resistor is placed as a current limiting element.

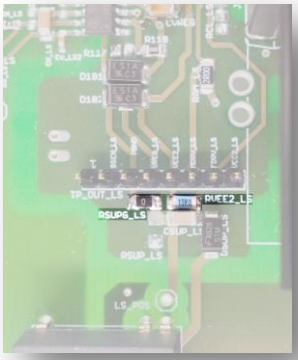


Figure 10 Board assembly MOSFET drain related supply

Although the supply is referred to the MOSFET drain potential in this case all other voltages on the output side of the driver are still referred to VCC2. This has to be taken into account when measuring any voltages on this side of the driver (see chapter 5.2)

3.3.3 Bootstrap supply

The LS driver can also be supplied with a bootstrapping scheme.

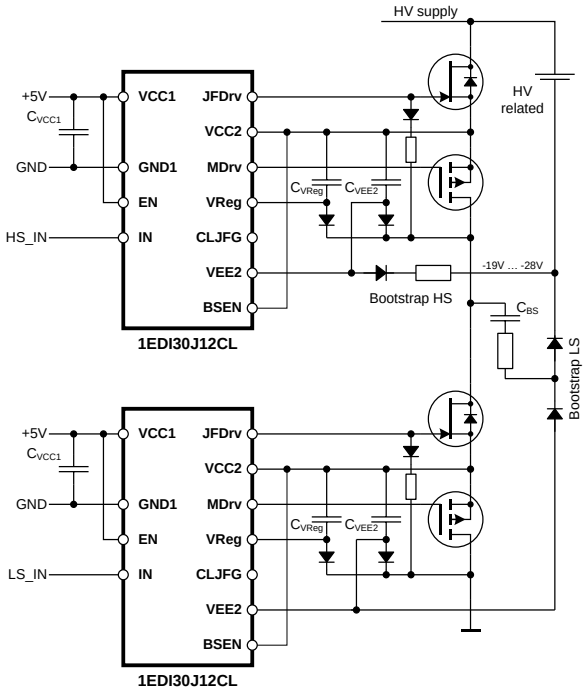


Figure 11 Bootstrapping supply

In this case RSUP_LS, RSUPG_LS, RVEE2_LS and RSUP_HS are desoldered and RSUPD_HS is assembled with a 0 Ω resistor.

To enable the energy transfer to the low side, several diodes and resistors have to be mounted: DBS1, DBS2, DBS3, RBS2, RBS3 as well as CBS1 and CBS2. As diodes STTH112 are recommended. The value of the resistors should not be lower than 2.2 Ω and they should not be SMD devices. As a possible starting point for testing the bootstrap mode, 2.2 µF capacitors are recommended to be used for CBS1 and CBS2.

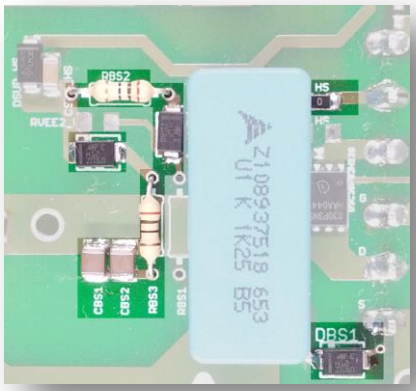


Figure 12 Board assembly bootstrapping supply

Furthermore R18 and R118 are taken out as well and the BSEN pin is connected to VCC2 via R17 and R117 or by two opto couplers (OK_LS and OK_HS) and jumpers at ROK_LS and ROK_HS. The opto couplers are supplied either with 5 V or VDDH. This can be chosen by assembling either ROK_5V_LS and ROK_5V_HS or ROK_VDDH_LS and ROK_VDDH_HS.

When the driver power supply is between the two under voltage lockout levels (UVLO) in bootstrapping mode the driver gives out pulses at the BSEN pin. These pulses could be used to signal to a controller that an increased deadtime is necessary during this phase of the bootstrap operations. Please refer to the datasheet of the driver.

The schematic utilizing bootstrap supply can be viewed in Appendix C.

3.3.4 Isolated direct supply

It is also possible to supply the driver directly with -19 V.

Using this supply option it is possible to spare the capacitor and the diode at *VEE2*. Instead the Pins *VReg* and *VEE2* have to be connected together. This deactivates the internal regulator. Since a clean power supply is necessary to ensure safe and correct operation the auxiliary power supply has be designed to have a -19 V output voltage with a maximum ripple of 5%.

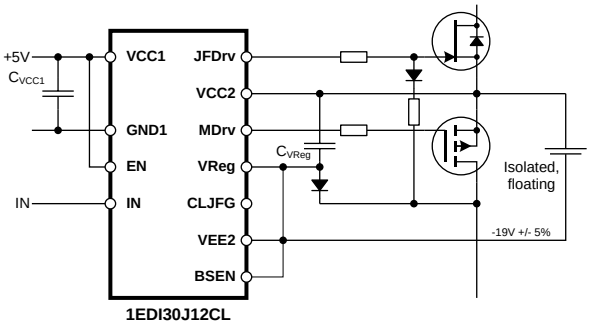


Figure 13 Isolated direct supply

This supply cannot easily be realized on this evaluation board. For this the TRACOs need to be unsoldered, and a new isolated supply has to be mounted in their place. Additionally the driver pins VReg and VEE2 have to be shorted. This can for example be done at the SMD pads of the VReg and VEE2 capacitors

It is highly recommended that this supply option is only tested when the functionality of the board is fully understood!

3.4 Control signal (NOC_IN)

For ease of use a non overlapping clock generator has been implemented so that only one single PWM signal is necessary to control the board in a first evaluation. This NOC logic is creating the PWM signals for both the LS (low side) and HS (high side) driver.

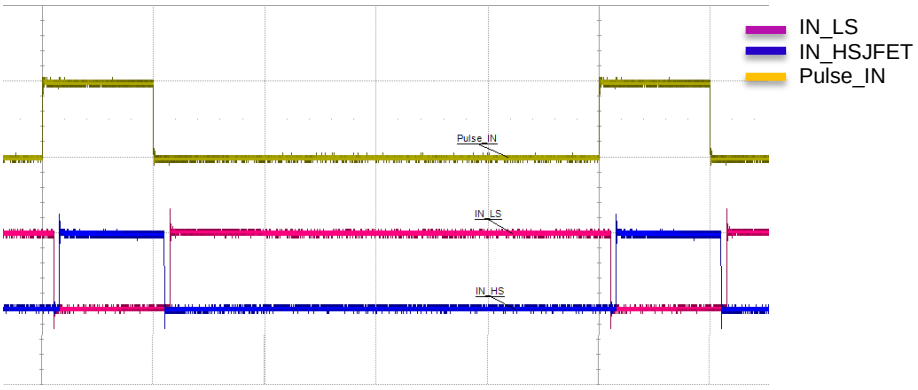


Figure 14 PWM signals

An example can be seen in Figure 14. The yellow line represents the signal coming from the signal generator or controller. The magenta line represents the inverted signal coming from the NOC that is fed into the LS driver. The blue line is the signal from the NOC for the HS driver.

This picture also shows the dead-time between the signals that is produced by the NOC.

Figure 15 shows how the probes are connected to measure these signals.

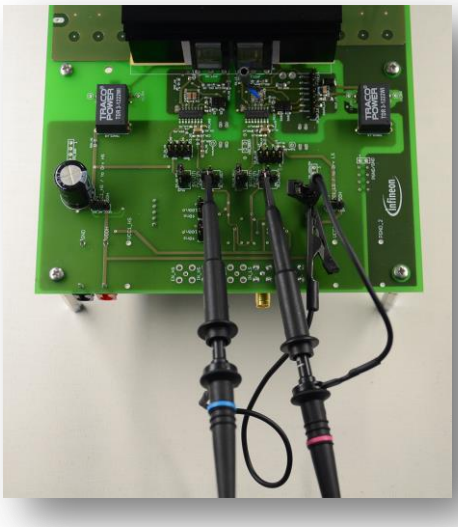


Figure 15 Probe connection NOC signal

4 Mounting of SiC JFET to the heatsink

When mounting the heatsink to the JFETs a thermally conductive isolating film has to be placed between the JFET and the heatsink. This film must be able to block the DC link voltage and the thermal resistance of the material should be as low as possible.

The isolation material used in this board has a dielectric breakdown voltage (AC) of 9 kV and a thermal resistance of ~0.3 K in²/W.

Figure 16 Isolating Film between JFET and heatsink

When mounting the heatsink to the board an isolating film has to be placed between heatsink and PCB to avoid any possibility of shorting two voltage potentials. This film must be able to block at least the DC link voltage.

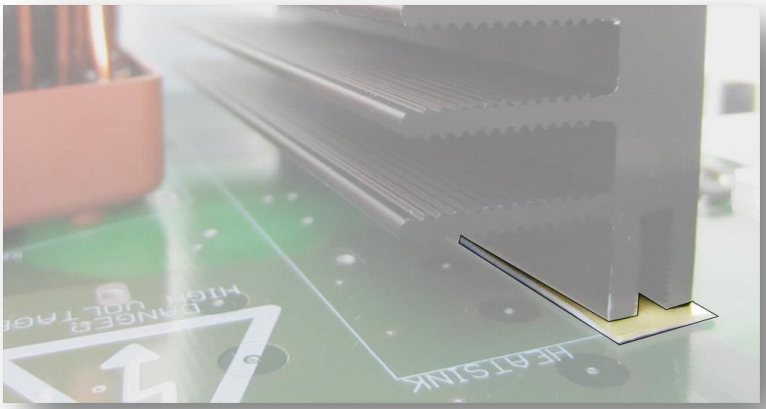


Figure 17 Isolating film between heatsink and PCB

5 Measurements

5.1 Current measurements

To measure the current it is possible to mount a coaxial shunt on the board. In this case the LS p-channel MOSFET has to be unsoldered and the shunt can be placed in the prepared holes. The footprint of these holes is designed to fit a T&M RESEARCH SDN-414 series shunt. The polarity of the shunt has to be checked so that the ground potential is mounted at the JFET source!

It has to be kept in mind that the shunt resistor has a higher inductance compared to the PMOS related stray inductance. At high di/dt measurements it is possible that the driver can be disturbed through the CLJFG pin by the induced voltage over the shunt resistor. For these measurements it is recommended to desolder the resistor *RCLJ_LS* to disconnect the CLJFG pin from PGND.

REMARK: the replacement of the PMOS by a low ohmic shunt resistor disables the normally off behavior of the switch. Therefore it has to be made sure that the auxiliary supplies are present before the DC link is activated. Otherwise the driver will not pinch off the JFET and the device could be damaged.

To measure the current of the power inductor a current probe can be clamped onto the enameled wire next to the choke. (See Figure 28)

5.2 Voltage measurements

Voltages on the output side of the driver are always referred to VCC2, which is connected to the source pin of the JFET. The ground connection of the oscilloscope probes must be connected to this point and not to GND. Referring the probes to GND would lead to interference of the signals since there is a potential difference between VCC2 and GND due to the $R_{DS(on)}$ and stray inductance of the low-voltage MOSFET.

In order to get a clean signal it is not recommended to use the probe ground connector cable but to use probe holders instead. These are normally soldered on the board directly. Since this would lead to increased space requirements this would also lead to increased board parasitics.

To avoid this, twisted cables can be soldered to the pins of the probe-holders. These can then be soldered to the board. Figure 18 shows the steps that are required to create such a probe holder.

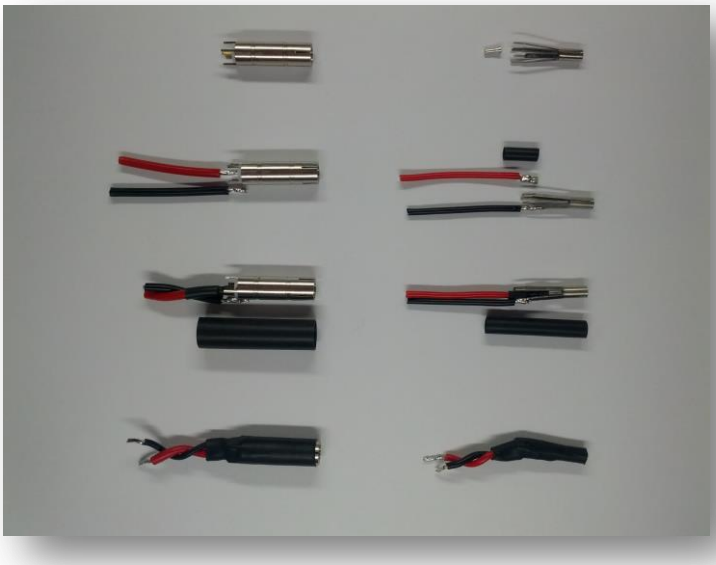


Figure 18 Evolutionary steps in creating probe holders for LeCroy probes

Figure 19 and Figure 20 show the difference between using a probe holder for the oscilloscope probe (yellow signal) and using the oscilloscope hook and an alligator ground clamp (blue signal). The blue signal shows higher voltage swings compared to the signal measured with the probe holders.

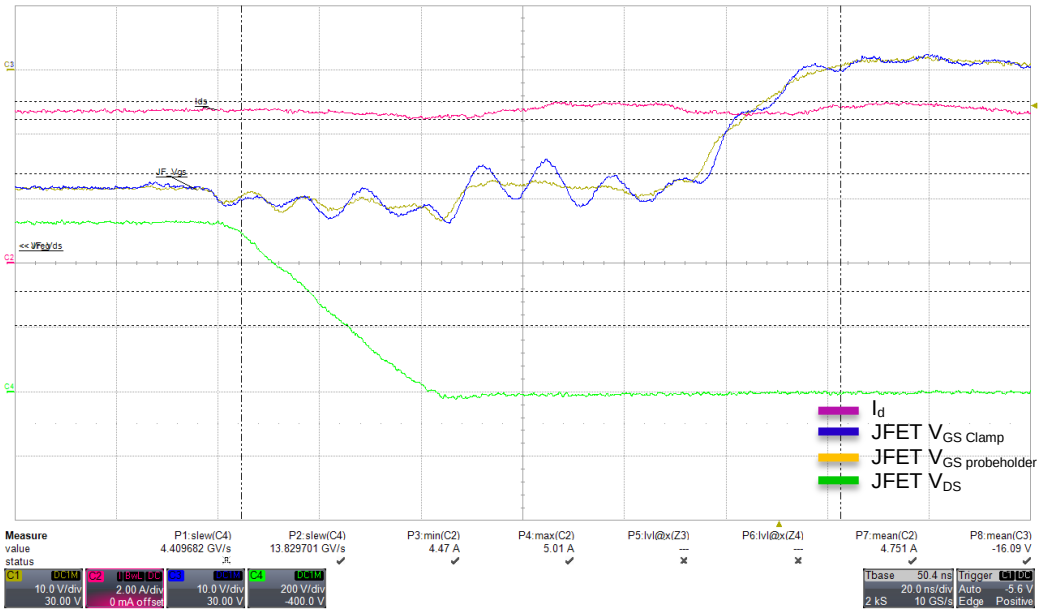


Figure 19 Comparison JFET V_{GS} probeholder (yellow) vs. aligator ground clamp (blue) – turn on

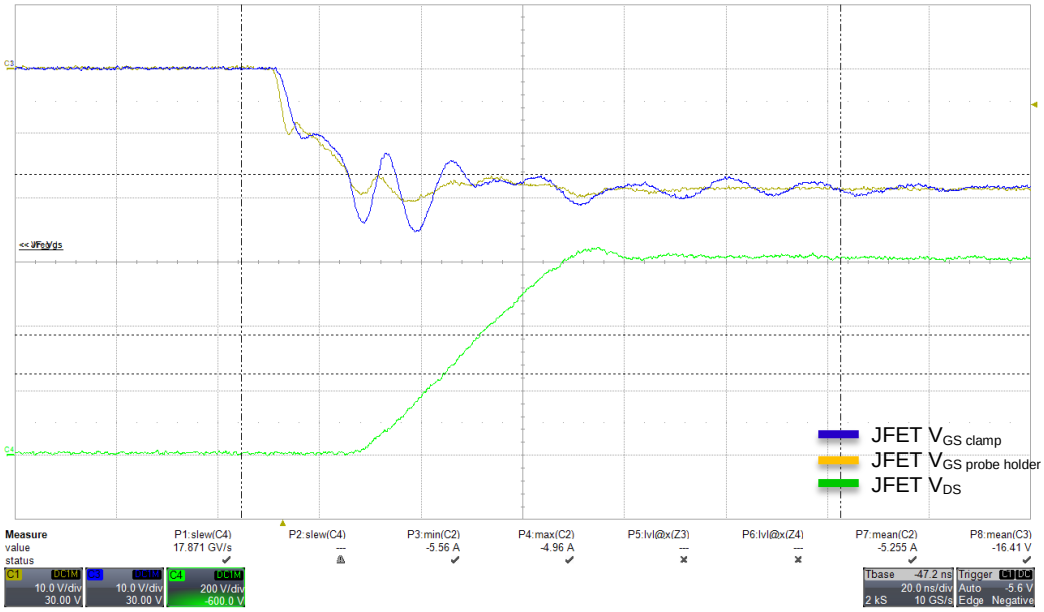


Figure 20 Comparison JFET V_{GS} probeholder (yellow) vs. aligator ground clamp (blue) - turn off

5.2.1 Measurements at the driver input side

When measuring the driver input side all voltages are referred to GND. Therefore the low side as well as high side driver input signals can be measured.

5.2.2 Measurements at the driver output side

As mentioned in section 5.2 as well as the 1EDI30J12CL datasheet all voltages at the output side (VEE2, JFDrv, MDrv, VReg, BSEN) of the driver are referred to *VCC2*.

When measuring these signals it is recommended to have a galvanic isolated oscilloscope (isolation transformer on the oscilloscope power supply) since the reference potential is not PGND/GND. If the oscilloscopes ground is not galvanically isolated a short circuit over the PMOS can be created between the power source ground and the oscilloscope ground. The signals of the low side driver output can be measured with these recommendations.

It is however difficult to measure the high side signals due to the fact that the VCC2 potential of the high side is moving with the switching node (high and fast common mode shifts). Measuring these signals without adequate protection might destroy the measuring equipment! Even when using equipment that fulfills the requirements, a measurement with clean signals will probably not be possible due to the fast common mode shifts.

It is therefore recommended that the characterization of the components should be done by measuring only signals on the low side of the half-bridge.

6 Clamping diode

As clamping diodes Infineon Technologies BAS16-03W are mounted. These diodes are used in the Direct Drive Topology[7] to pull the JFET gate low during reverse startup or if a power supply failure occurs. They are connected between the MOSFET drain and JFET gate. In this design a BAS16 diode is used because the ringing over the diode does not exceed the blocking voltage of 80 V. When choosing a diode for a different design the ringing which is created by fast current changes in the parasitic inductances in the switching path between JFET source and MOSFET drain needs to be checked and a diode with a fitting blocking capability has to be chosen.

A 20 Ω resistor is placed in series with the diode to protect the diode by limiting the current through the diode. The size of the resistor is chosen so the maximum current through the diode cannot be exceeded.

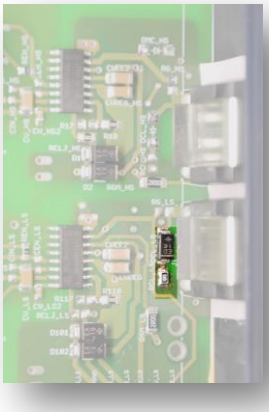


Figure 21 – Position of external LS clamp diode and resistor

[7] Please refer to the 1EDI30J12Cx datasheet and Application Note for more information about the Direct Drive Topology and safety measures.

7 Mounted power inductor

The mounted power inductor has an inductance of 360 µH (±10%, see Figure 22).

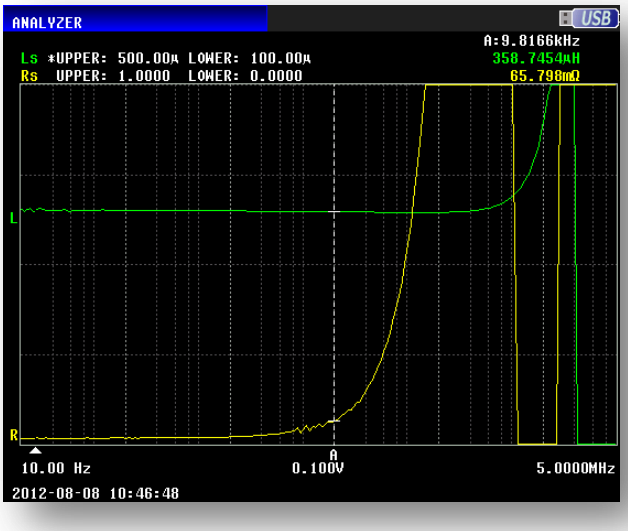


Figure 22 - Power inductor measurement

As cores two Magnetics Kool Mµ® 0077442A7 with a permeability of 90 µ are used. 30 windings with an enameled copper wire (2 mm diameter) are placed around the cores.

REMARK: During high power tests it is recommended to control the temperature of the power inductor while operating the board.

8 Getting started: first steps in operating the evaluation board

Before applying high voltage to the board it is recommended to familiarize oneself with the board first. These steps should help the operator to gain first impressions of the board without endangering anyone.

8.1 Auxiliary supply startup – setting up the low voltage domain of the system

1. Check that all jumpers are placed at their correct positions (refer to chapter 3.2)
2. Set the auxiliary power supply (LV power supply) to 12 V with a current limitation of 1 A.

   In the initial startup phase the board's TRACOs draw ~1 A to quickly settle the -24 V at their output pins. (Setup shown in Figure 23)
3. Set up the Arbitrary Frequency Generator (AFG) to a PWM signal with 25 kHz, 20 % duty cycle with a high impedance output. The termination resistor on the board is 4.7 kΩ. The AFG should therefore be set to high-Z output mode. The HIGH value of the signal should be 5 V, the LOW value 0 V.

   These parameters can be changed by the operator, however these values are recommended on a first startup to get to know the board. (See Figure 24)
4. Connect LV power supply to plugs *VDDH* (+) and *GND* (-) (see Figure 23)
5. Connect AFG to *NOC_IN* with a SMA cable

6. Turn on the low voltage power supply and check current consumption. After a brief spike to several hundred mA it should settle at about 90-110 mA in the standard assembly
7. If everything is working properly: start AFG signal pulses
8. Check if the following signals are correct: *IN_LS* and *IN_HS* (IN signal for the drivers). The oscilloscope probes can be hocked to the jumpers at *IN_LS_SEL* and *IN_HS_SEL*.

   The dead-time between the signals should be ~100 ns. If the value deviates severely the jumpers at *NOC_LS* and *NOC_HS* have to be checked. (Refer to chapter 3.4, Figure 14 & Figure 15)

   The reference potential of the signals is *GND*!
9. Check if the voltage level of *VReg* and *MDrv* is -19 V

   The reference potential for this signal is *VCC2* (please refer to the 1EDI30J12CL datasheet as well as to Figure 26). Disconnect all previously used probes from the board since they have used GND as reference potential.
10. Check if JFDrv is switching according to the signal of the AFG. The signal should be -19 V when the IN signal is 0 V.

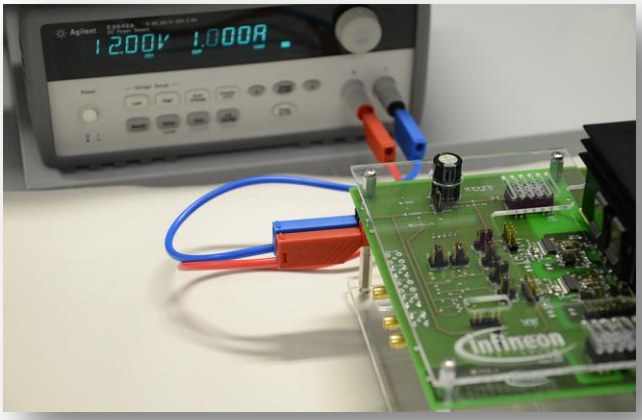


Figure 23 Connections LV domain

Figure 24 Control signal settings

8.2 DC link startup – setting up the high voltage domain

Attention – High Voltage

This section must only be executed by experienced engineers that are aware of the danger of high voltage systems and are properly trained!

1. Auxiliary supply setup must be working but disabled (Section 8.1)
2. Disconnect oscilloscope probes from the board
3. DC link startup (following auxiliary startup)
    a. Setup supplies
        i. Set up DC link supply to ~40 V
        ii. Connect DC link supply to *VIN* (+) and *PGND* (-) (see Figure 25 – red & black)
        iii. Connect a voltmeter between *VOUT* (+) and *PGND* (-)(see Figure 25 – yellow & blue)
        iv. Connect oscilloscope probes to JFDrv, MDrv, VReg (see Figure 26 & Figure 27)
        The reference potential for these signals is VCC2 (refer to 1EDI30J12CL datasheet).
        v. Connect current probe to enameled wire loop
    b. Turn on the auxiliary power supply (according to Section 8.1) as well as the control signal
    c. Turn on DC link supply
    d. Check voltmeter if the output voltage is correct
    If VIN=40 V and the duty cycle is 50% the output voltage VOUT should be ~20 V
4. Check JFDrv signals with oscilloscope for abnormalities
5. If the system is running correctly the voltage of the DC link can be changed to the desired value.
6. End test:
    a. Turn off DC link supply
    b. Turn off auxiliary supply

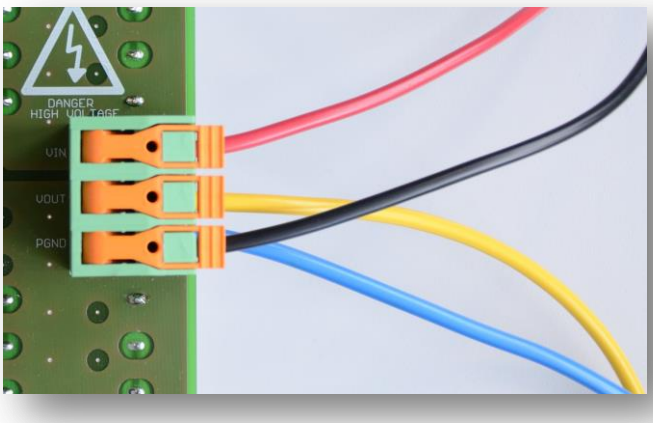


Figure 25 Connections HV domain - buck converter

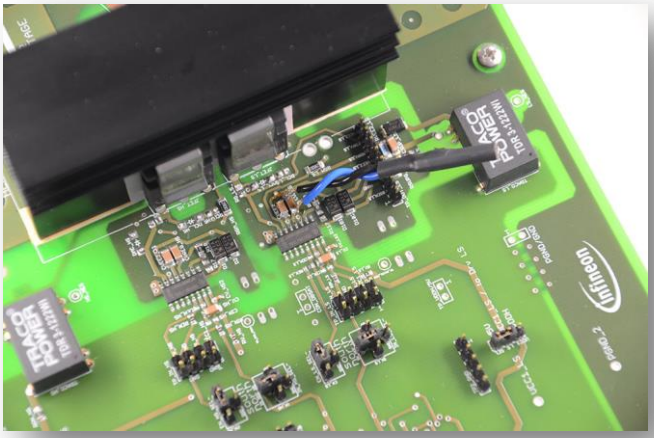


Figure 26 Probe holder at V_{Reg} capacitor

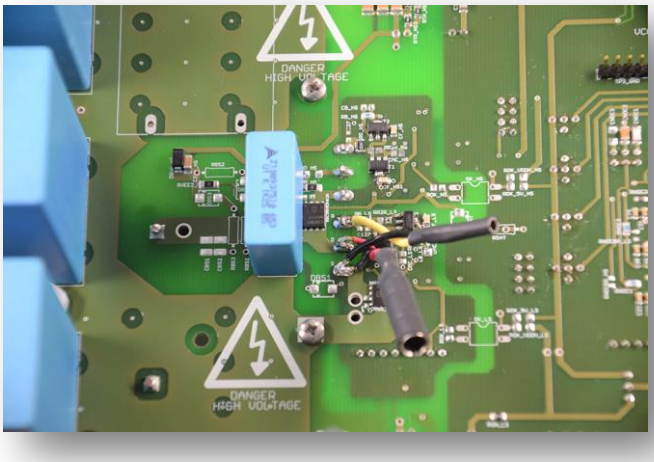


Figure 27 Probe holder at JFDrv and JFET V_{gs}

Figure 28 Connection of the current probe

If the setup is working stable a DC load can be connected to *VOUT* (+) and *PGND* (-)(see Figure 25 – yellow & blue). Please keep in mind that when running the system with a DC load a shutdown procedure without a huge load step is recommended:

1. Reduce load to <1 A
2. Stop the DC link supply
3. Switch off DC load

Make sure that functionality of the board is fully understood before high voltage is used!

9 Possible Test Topologies

Several topologies can be tested with this evaluation board. In each of them the test emphasis is on the CoolSiC™ JFET itself since it is defining the performance of the Direct Drive JFET Topology.

9.1 Synchronous Buck Converter

Figure 29 shows the application schematic when using the board as an synchronous buck converter.

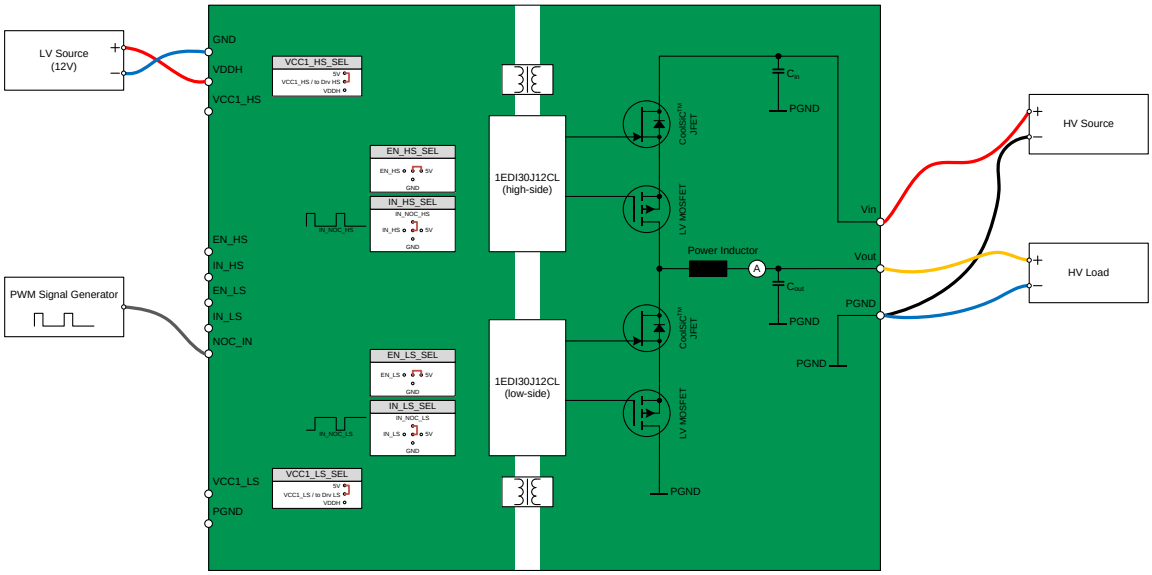


Figure 29 Simplified application drawing for a synchronous buck converter

9.1.1 Connections

A low-voltage domain and the signal generator should be set up as described in chapter 8.1.

The high-voltage source is connected to *Vin* and *PGND*. The high-voltage load is connected to *Vout* and *PGND*.

9.1.2 Jumper settings

The low voltage supply of the drivers (*VCC1_LS_SEL*, *VCC1_HS_SEL*) can be left in the standard position between 5 V and the middle connection point that is connected to the driver.

Both drivers should be permanently enabled. This is done by connecting the *EN_LS_SEL* and *EN_HS_SEL* to 5 V (*EAST*, std. assembly).

As *IN* signal the NOC signals can be used (see chapter 3.4). To use these signals connect *IN_LS_SEL* to *IN_NOC_LS* (*NORTH*) and *IN_HS_SEL* to *IN_NOC_HS* (*NORTH*).

These settings can be used for a first try but can of course be adapted to the desired test conditions.

9.1.3 Measurements

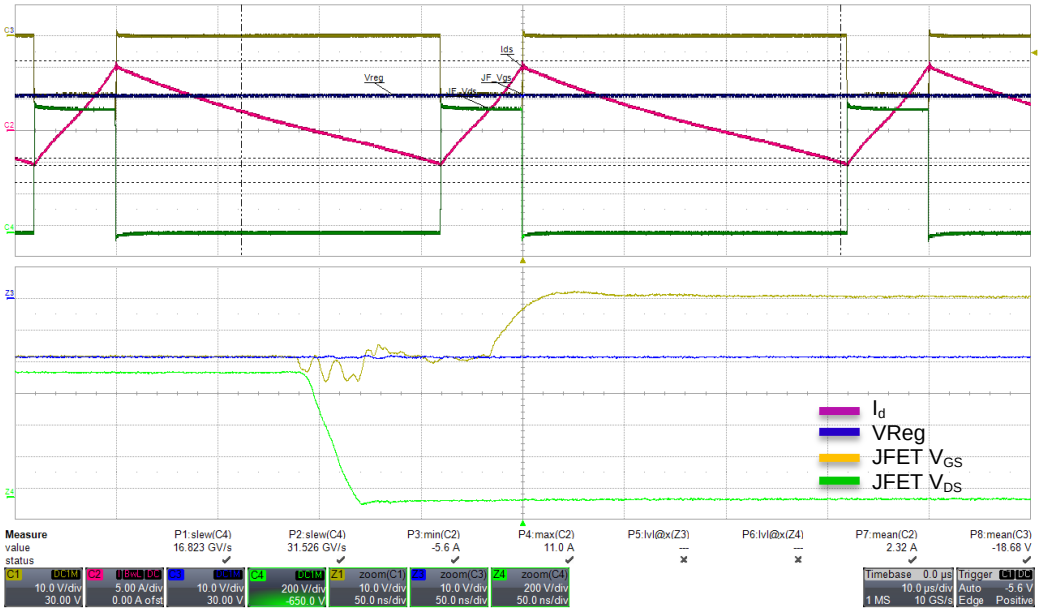


Figure 30 Measurement - sync. buck converter - 800V, 3A - turn on

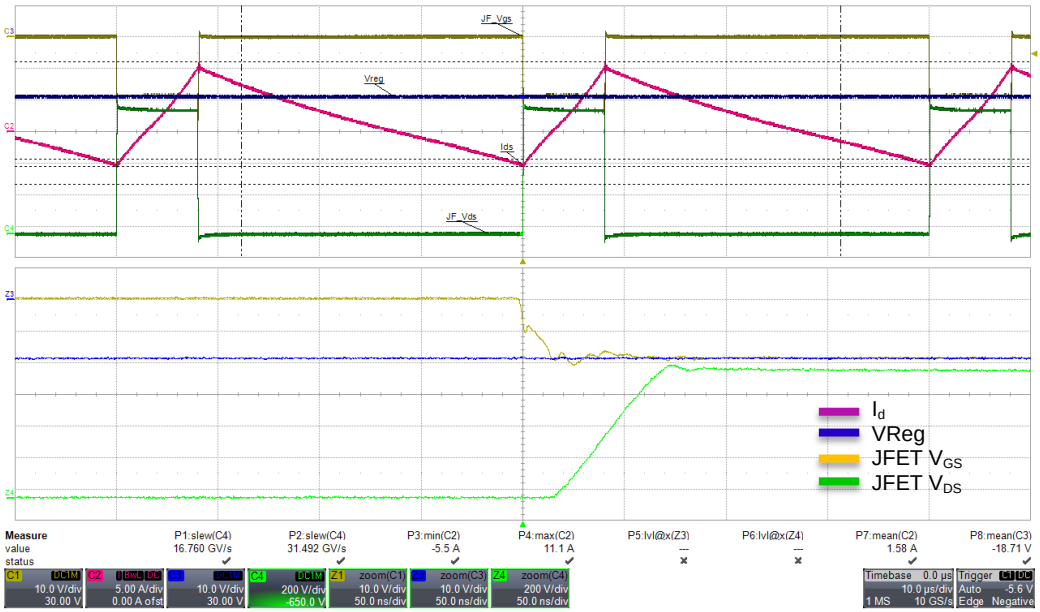


Figure 31 Measurement - sync. buck converter - 800V, 3A - turn off

Figure 30 and Figure 31 show exemplary measurements of the board using it as a synchronous buck converter at 800 V DC link voltage and 3 A DC load.

9.2 Synchronous Boost Converter

The board can easily be modified to be functioning as a synchronous boost converter (see Figure 32).

This topology has to be handled carefully to make sure that the output voltage does not exceed any maximum voltage of any connected component.

This topology has not been tested by Infineon Technologies to its full output voltage potential.

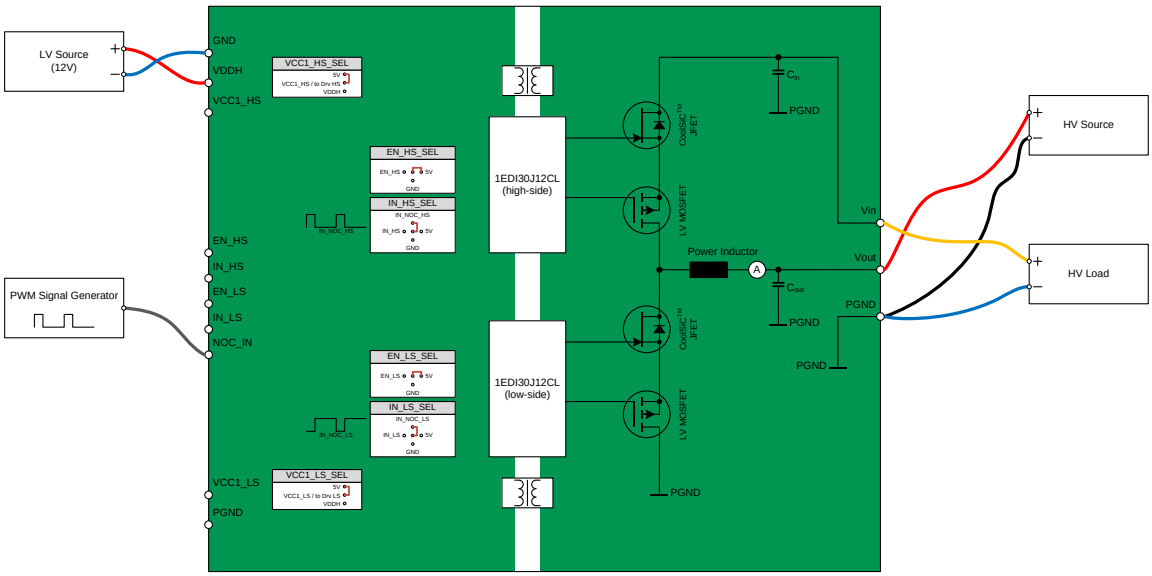


Figure 32 Simplified application drawing for a synchronous boost converter

9.2.1 Connections

For this measurement the connections of the high-voltage load and source are switched so that the load is connected to the plug *Vin* and the source is connected to the plug *Vout*. Both devices are again referred and connected to *PGND*. A simplified schematic of this setup can be seen in Figure 32.

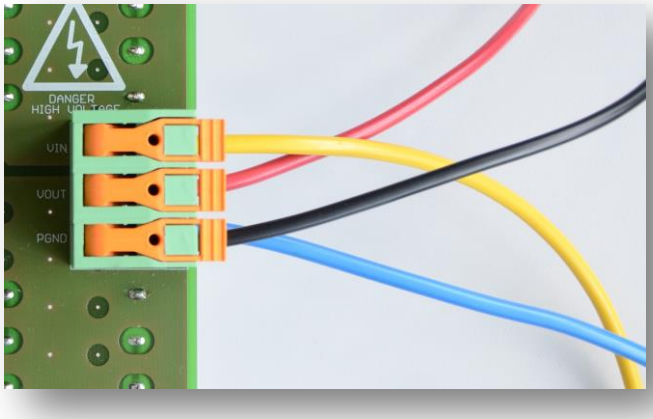


Figure 33 Connections HV domain - boost converter

9.2.2 Jumper settings

For a first try the jumper settings should be the same as for the buck converter. (see chapter 9.1.2.)

9.3 High-Side Buck Converter

This application is primarily used to look at the behavior of the JFET itself. By disabling the high-side stage and commutating against the internal body diode the switching event of the low-side switch can be looked at.

Figure 34 shows how the board has to be connected to test this configuration.

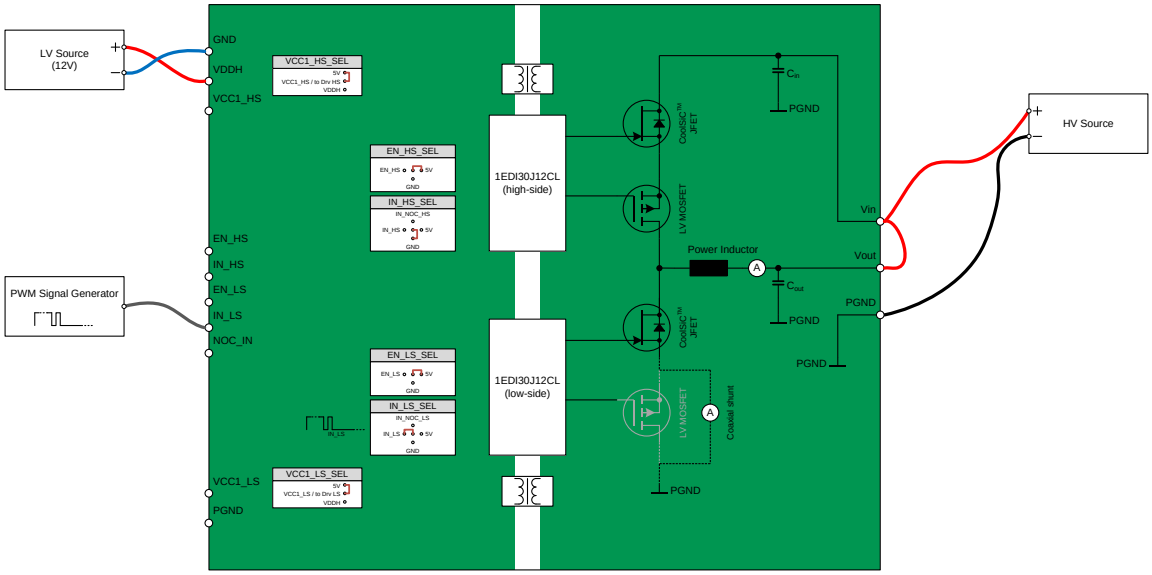


Figure 34 Simplified application drawing for a high-side buck converter

The low-voltage domain is set up as previously described.

The high-voltage source is connected to *Vin* and *PGND*. *Vout* is shorted with *Vin* for this test. In this test no high-voltage load is required.

The signal generator is connected to *IN_LS* and is sending out a double pulse. This double pulse has the same high and low voltage settings as in the other two tests. The double pulse itself can be triggered manually or it can also be repetitive (up to several pulses per second). The first pulse is used to energize the inductor to a desired current. The turn-off behavior of the JFET can be looked at the end of this first pulse. After a brief pause (~300 ns – 600 ns) a second pulse is sent. This pulse is used to look at the turn-on behavior of the JFET at the given load current. (See Figure 36 and Figure 37)

It is also possible to measure the exact current through the JFET. For this measurement the low-side p-channel MOSFET has to be desoldered and a coaxial shunt is placed on the board (see chapter 5.1)

Since the low-voltage MOSFET is constantly turned on during normal operation of the Direct Drive JFET Topology it is not significantly influencing the normal switching behavior of the driver stage. Therefore the coaxial shunt's placement is parallel to the MOSFET on the board and is meant to replace the MOSFET during this test.

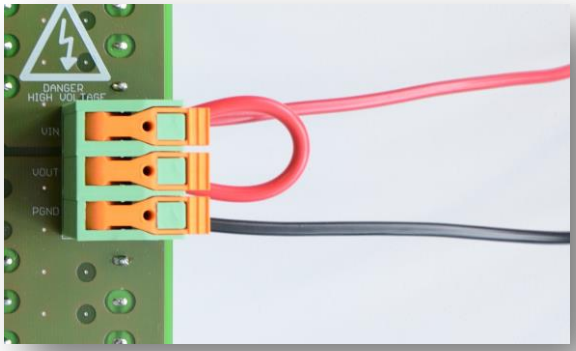


Figure 35 Connections HV domain - highside buck converter

9.3.1 Jumper settings

The high-side JFET is turned off by the driver and the current commutates against the body diode of the high-side JFET.

The *IN_HS_SEL* jumper-cross is connected to *GND* (*SOUTH*) to send a constant off signal. The *IN_LS_SEL* jumper is connected to *IN_LS* (*WEST*; the connection to the SMA plug IN_LS).

Both *EN* signals are kept at 5 V (*EN_HS_SEL* and *EN_LS_SEL* to *EAST*).

9.3.2 Measurements

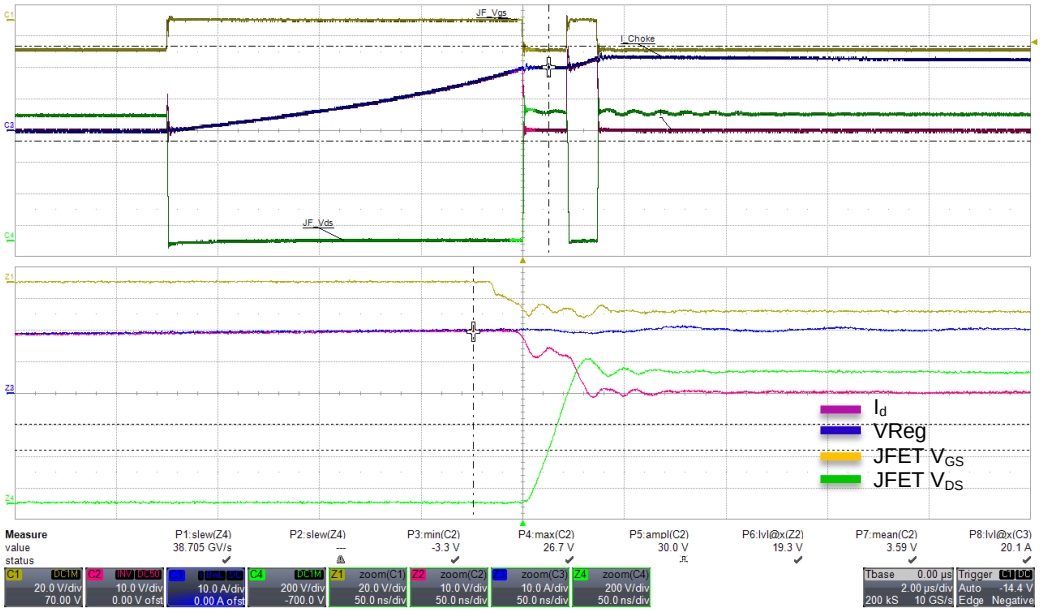


Figure 36 Measurement - double pulse - 800V 20A - turn off

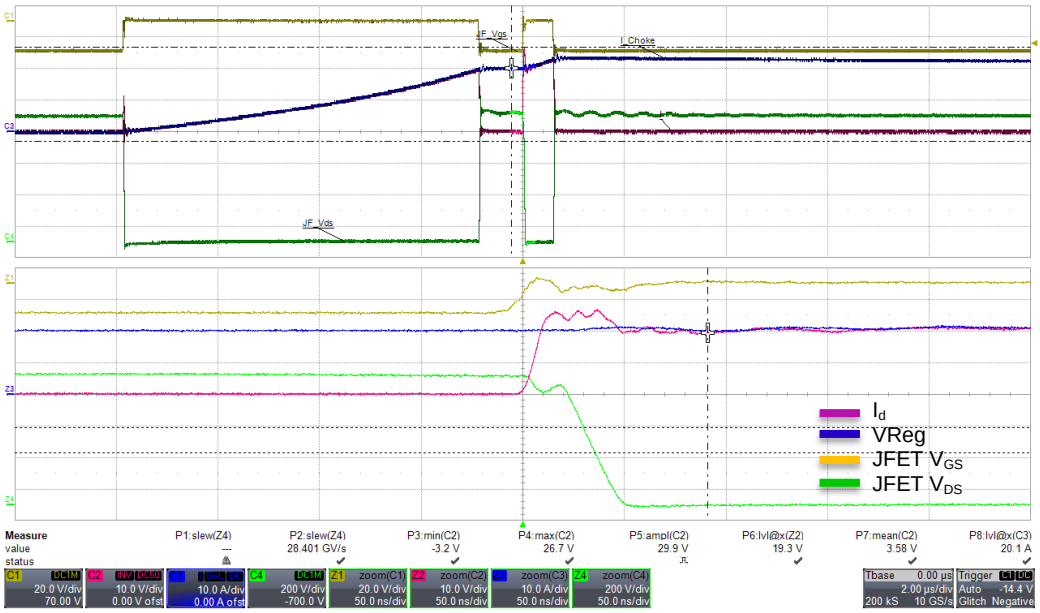


Figure 37 Measurement - double pulse - 800V 20A - turn on

10 Possible Gate Control Circuits

With this board it is possible to test several ways of controlling the JFET gate. When changing the gate drive circuit any other gate driving circuit variant has to be desoldered.

The best topology to view the switching behavior of the CoolSiC™ JFET is the High-side Buck configuration. In this topology both the switching on and off signals can be viewed directly at the low-side switch. The board configuration for this topology can be seen in chapter 9.3.

10.1 Emitter follower as booster (standard assembly)

The standard assembly has an emitter follower between the driver output pin and JFET gate. This booster stage is used to enable the best switching behavior by reducing the dynamical switching losses. To ensure a low-parasitic and space efficient layout it is placed on the bottom of the evaluation board with a low-ohmic short connection to the JFET.

A booster stage is typically used when driving a JFET with a low-ohmic $R_{DS(on)}$ (70 mΩ) or when driving parallelized JFETs.

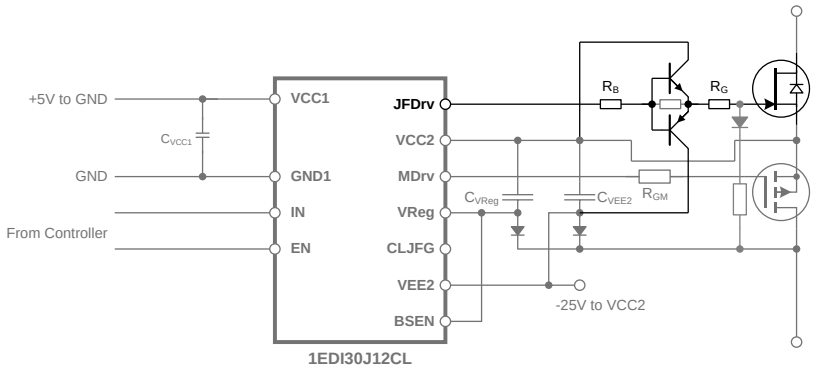


Figure 38 Principle schematic - gatecircuit with booster

This booster stage is built up from two bipolar transistors: ZXTN2010Z and ZXTP2012Z in a SOT89 package. The base resistors (RB_LS, RB_HS) are 2 Ω. A 2 Ω gate resistor (RG_LS, RG_HS) is placed between the booster stage and the JFET. To realize a rail-to-rail amplifier a resistor (39 Ω, RR2R_LS, RR2R_HS) is placed between the bases and emitters of the two bipolar transistors.

The resistor values can be changed according to the desired switching speeds of the boost transistors and the JFET itself. The mounted values are representing a balanced starting point.

Additionally a capacitor can be placed in parallel to the base resistor (CB_LS, CB_HS) to create a filter at the bases.

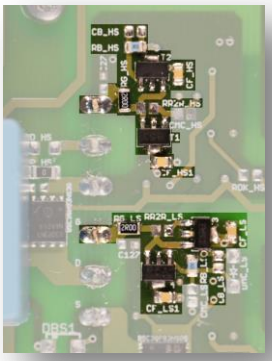


Figure 39 Board assembly - gatecircuit with booster (bottom side)

It is recommended to use a base resistor of at least 1 Ω to safeguard the driver by limiting any transients that might come back from the switches.

10.2 Gate resistor

The simplest way of driving the CoolSiC™ JFET is to only use a gate resistor in the gate circuit. Best switching results can be reached by using a low-ohmic resistor in the range of 1 – 2 Ω. It is recommended to drive the JFET with at least a 1 Ω resistor to protect the driver against any kickback coming from the switch.

A higher resistor value can be used if a lower dv/dt of the drain-source voltage is desired.

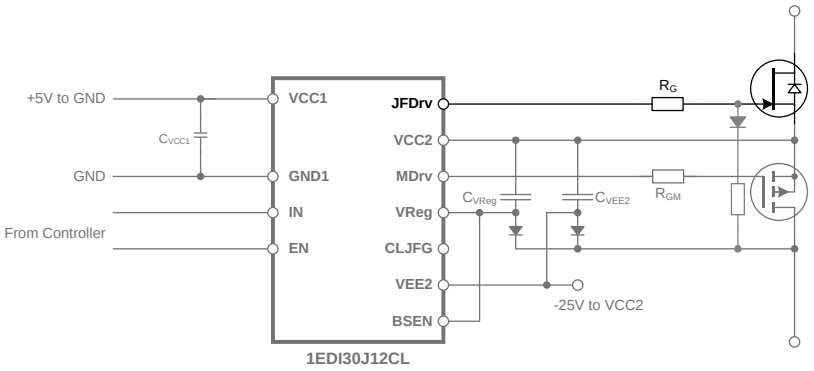


Figure 40 Principle schematic – gate circuit with R_g

The principle schematic of a driverstage with a gate resistor can be seen in Figure 40. The corresponding board assembly can be seen in Figure 41.

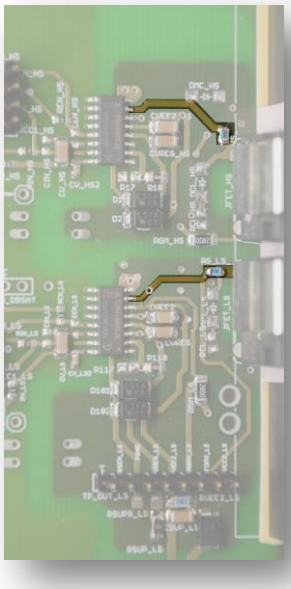


Figure 41 Board assembly - gatecircuit with R_g

When using this circuit the booster stage and the accompanying resistors (see chapter 10.1) have to be desoldered.

10.3 Gate resistor with Miller Clamp circuit

In high inductive designs a Miller Clamp circuit might be beneficial to clamp the gate to -19 V. A possible circuit can be seen in Figure 42.

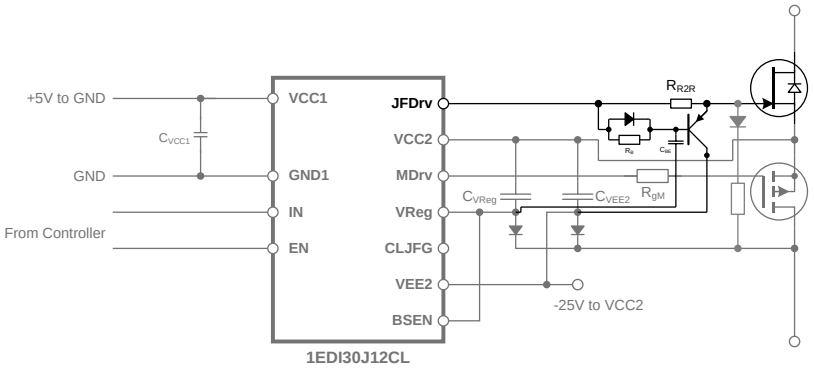


Figure 42 Principle schematic – gate circuit with Miller Clamp

This circuit can also be realized on the evaluation board. A picture showing the assembly can be seen in Figure 43 and Figure 44.

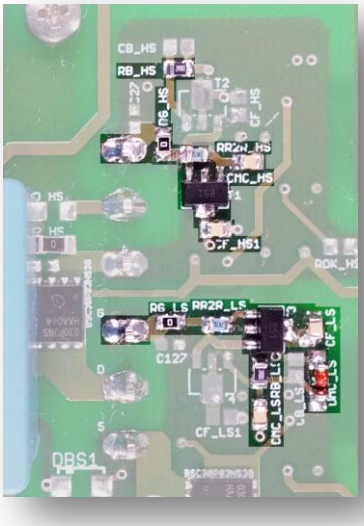


Figure 43 Board assembly - gate circuit with Miller Clamp (bottom side)

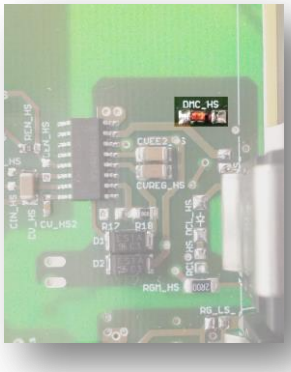


Figure 44 Board assembly - gate circuit with Miller Clamp (top side)

References

1. 1EDI30J12Cx Datasheet
2. 1EDI30J12Cx Application Note AN2013-17
3. 1200V Evaluation Board documents
    - Appendix A Full schematic
    - Appendix B Schematic - Standard Assembly
    - Appendix C Bootstrap schematic
    - Appendix D Board layout
    - Appendix E Bill of Material – Full Schematic
    - Appendix F Bill of Material – Standard Assembly
    - Appendix G Bill of Material – Bootstrapping

Appendix: schematics and layout

Appendix A Full schematic

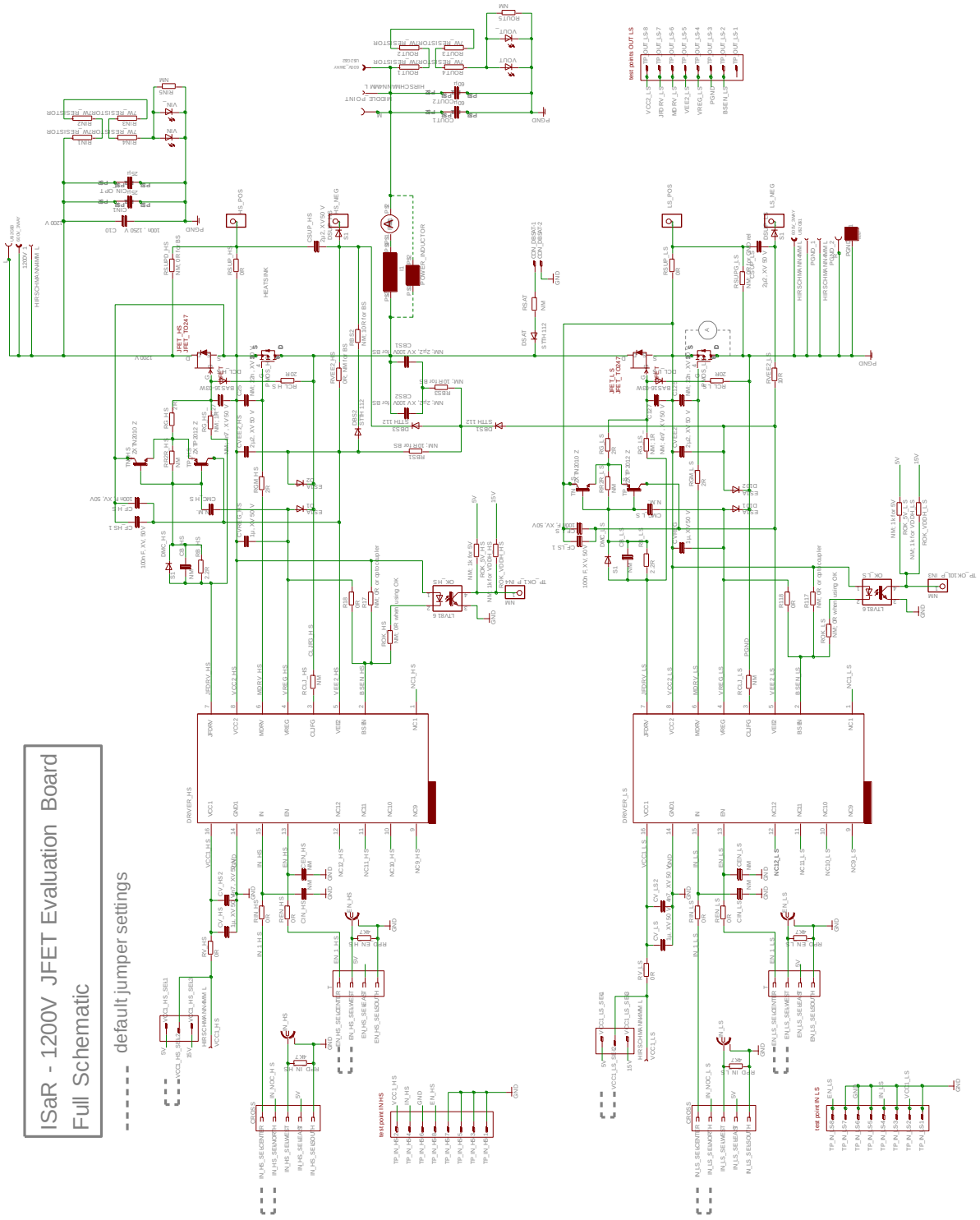


Figure 45 Full Schematic - part 1

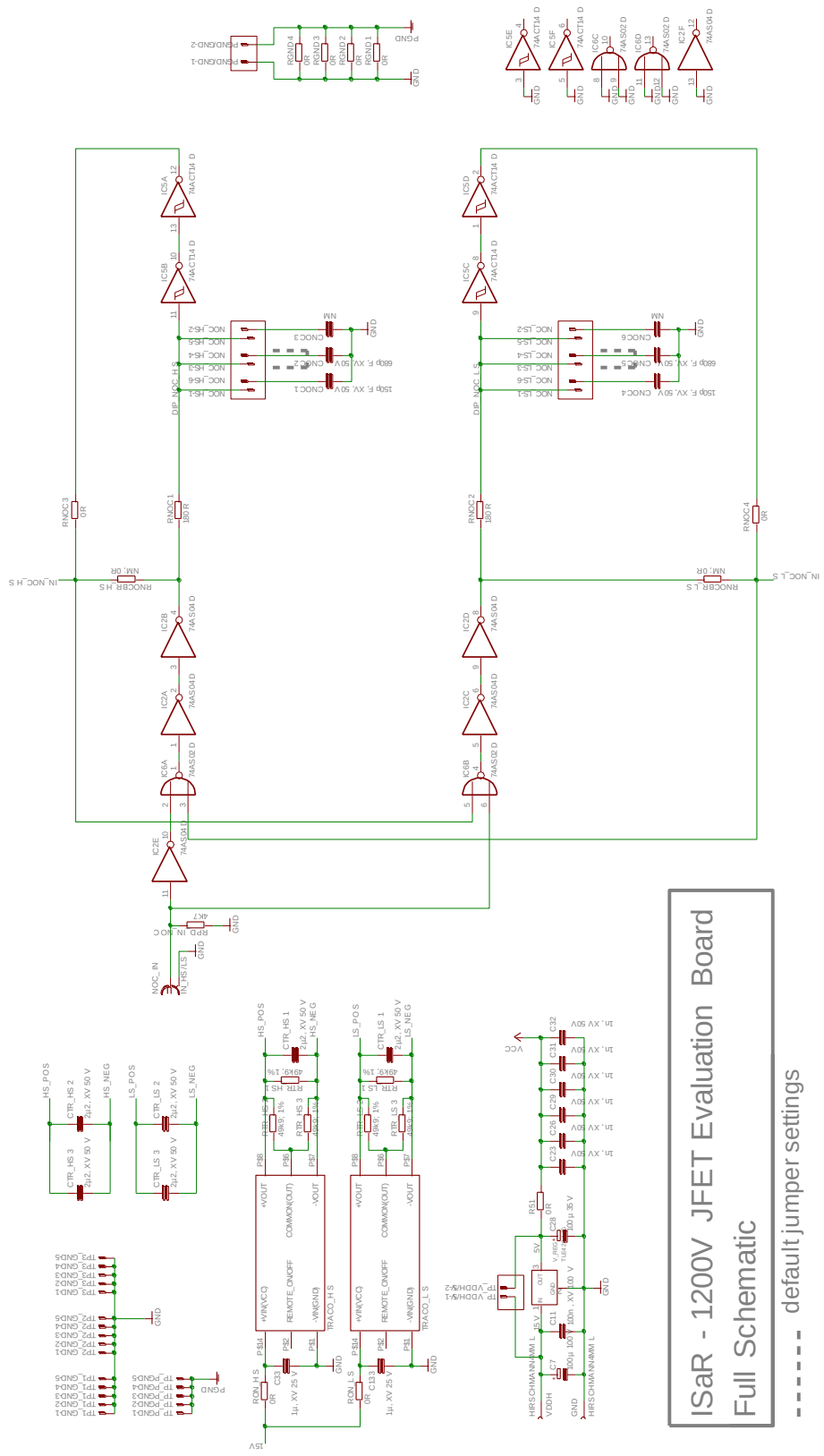


Figure 46 Full Schematic - part 2

Appendix B Schematic - Standard Assembly

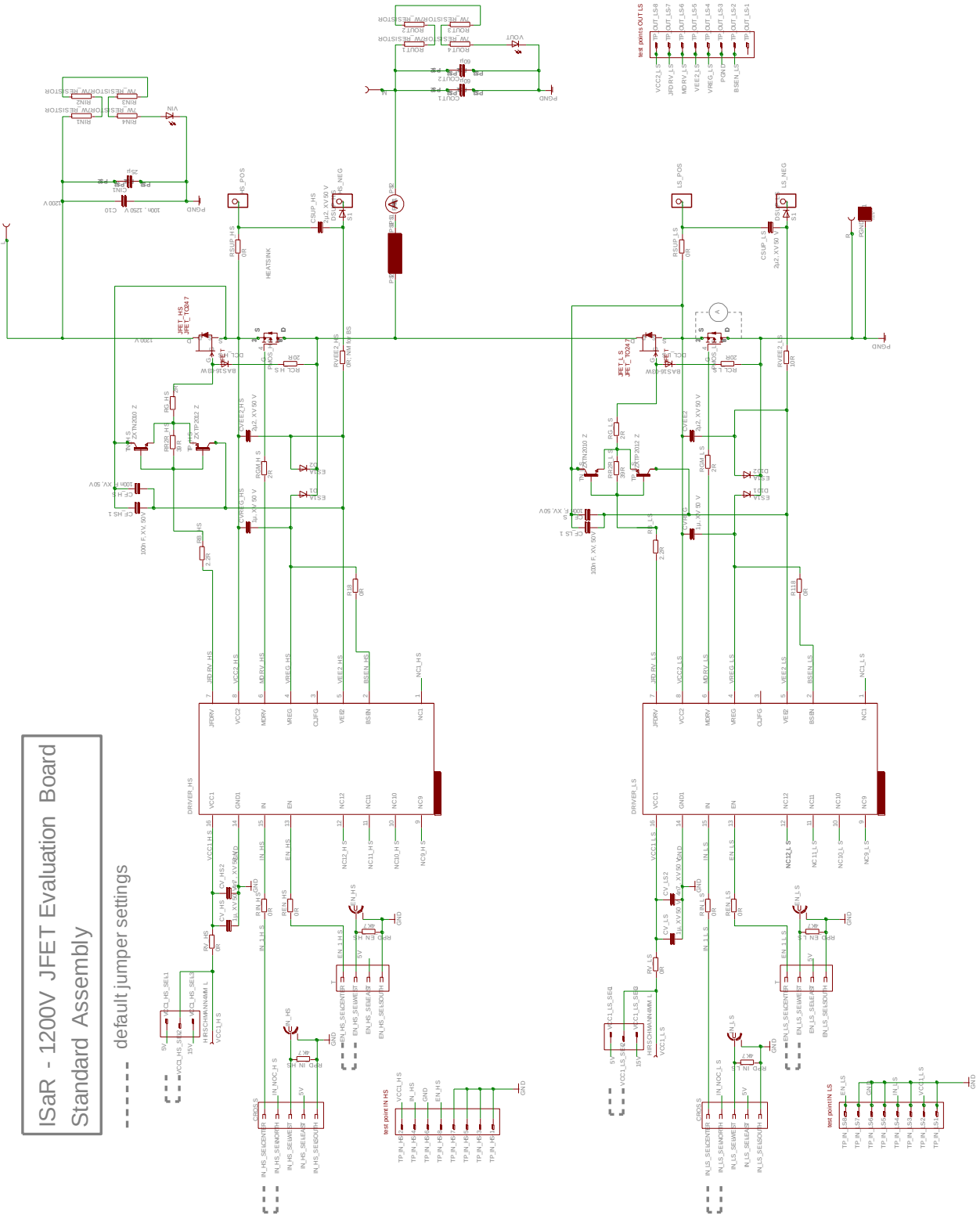


Figure 47 Schematic - Standard Assembly - part 1

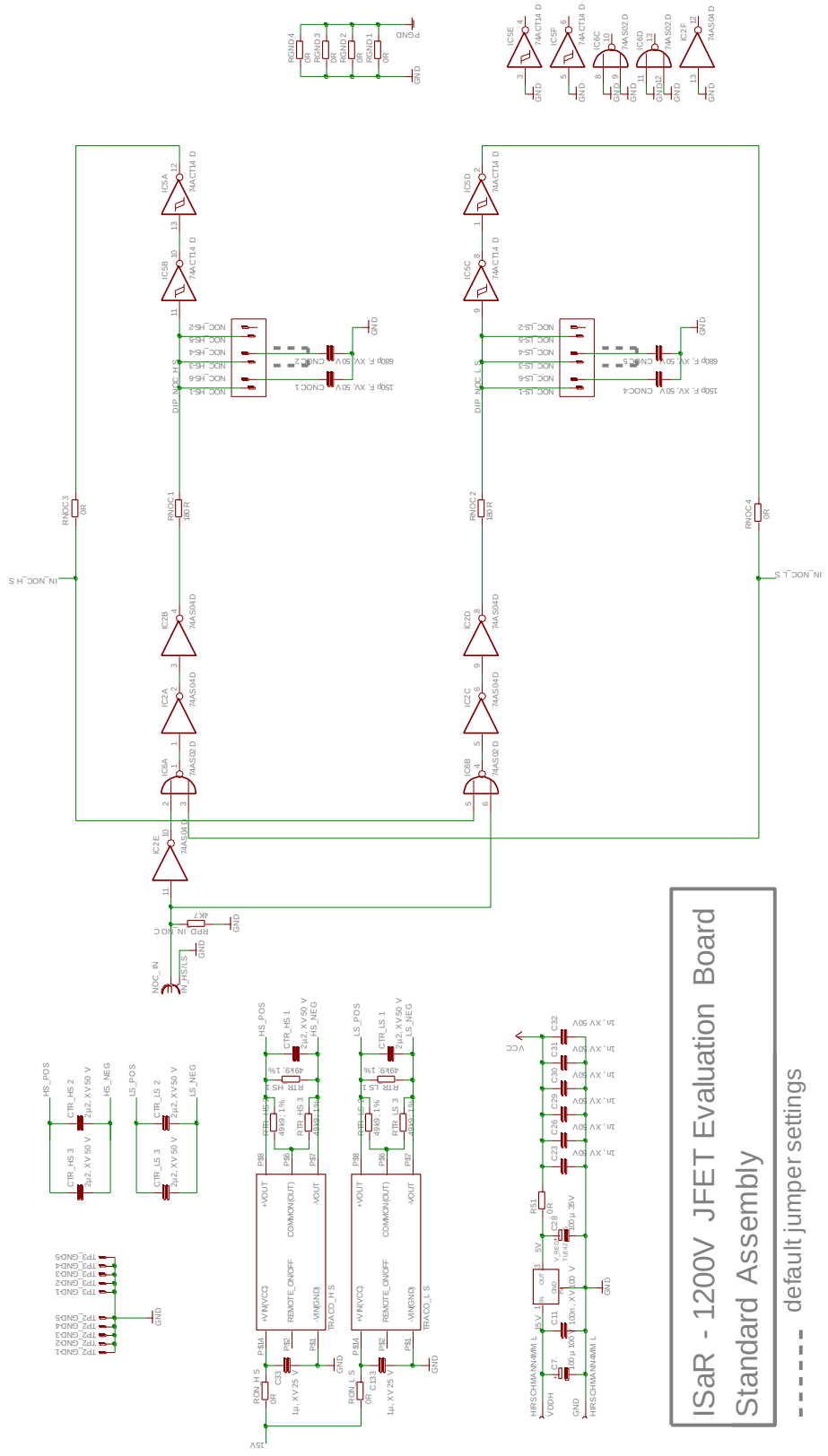


Figure 48 Schematic - Standard Assembly - part 2

Appendix C Bootstrap schematic

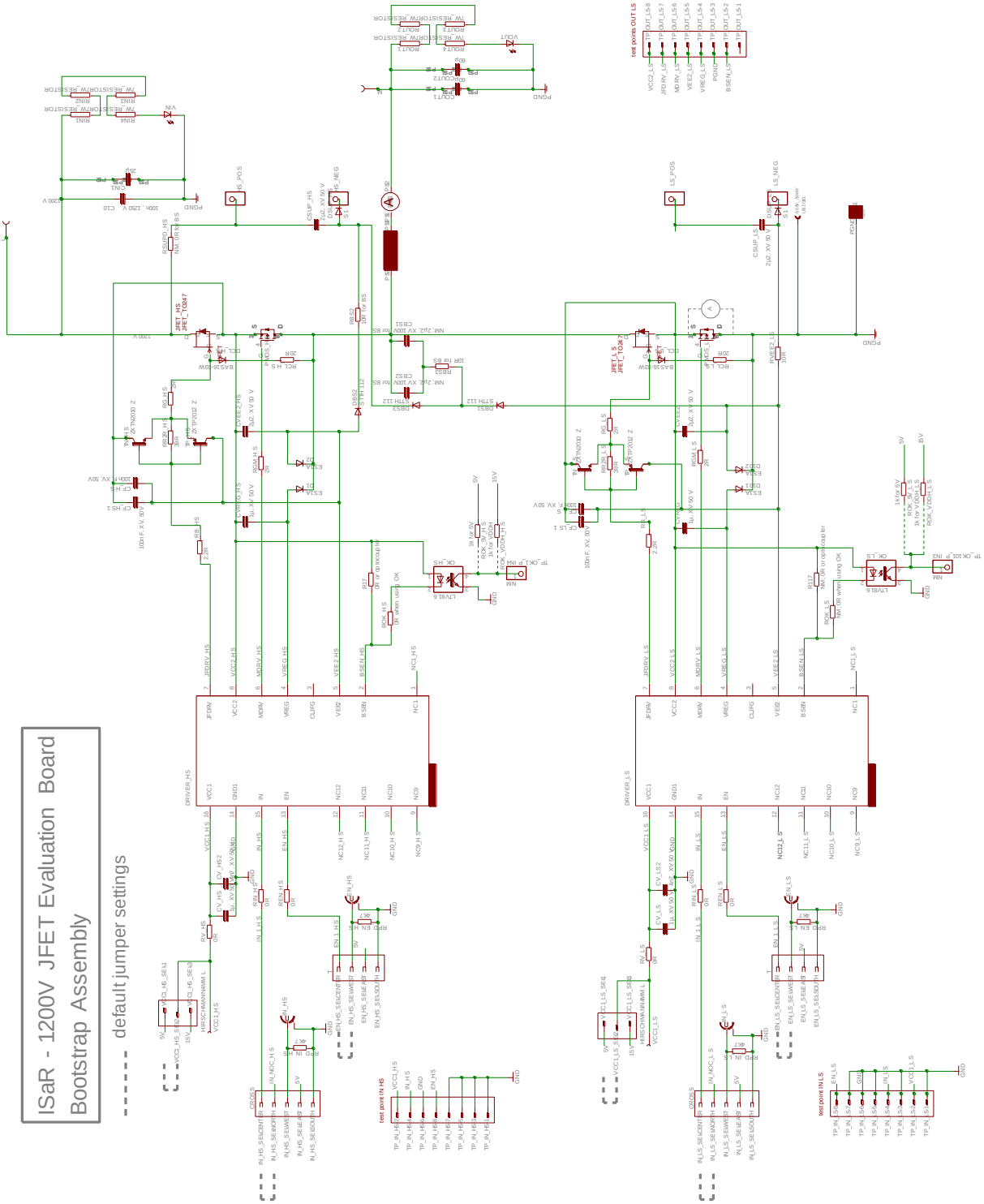


Figure 49 Schematic - Bootstrapping - part 1

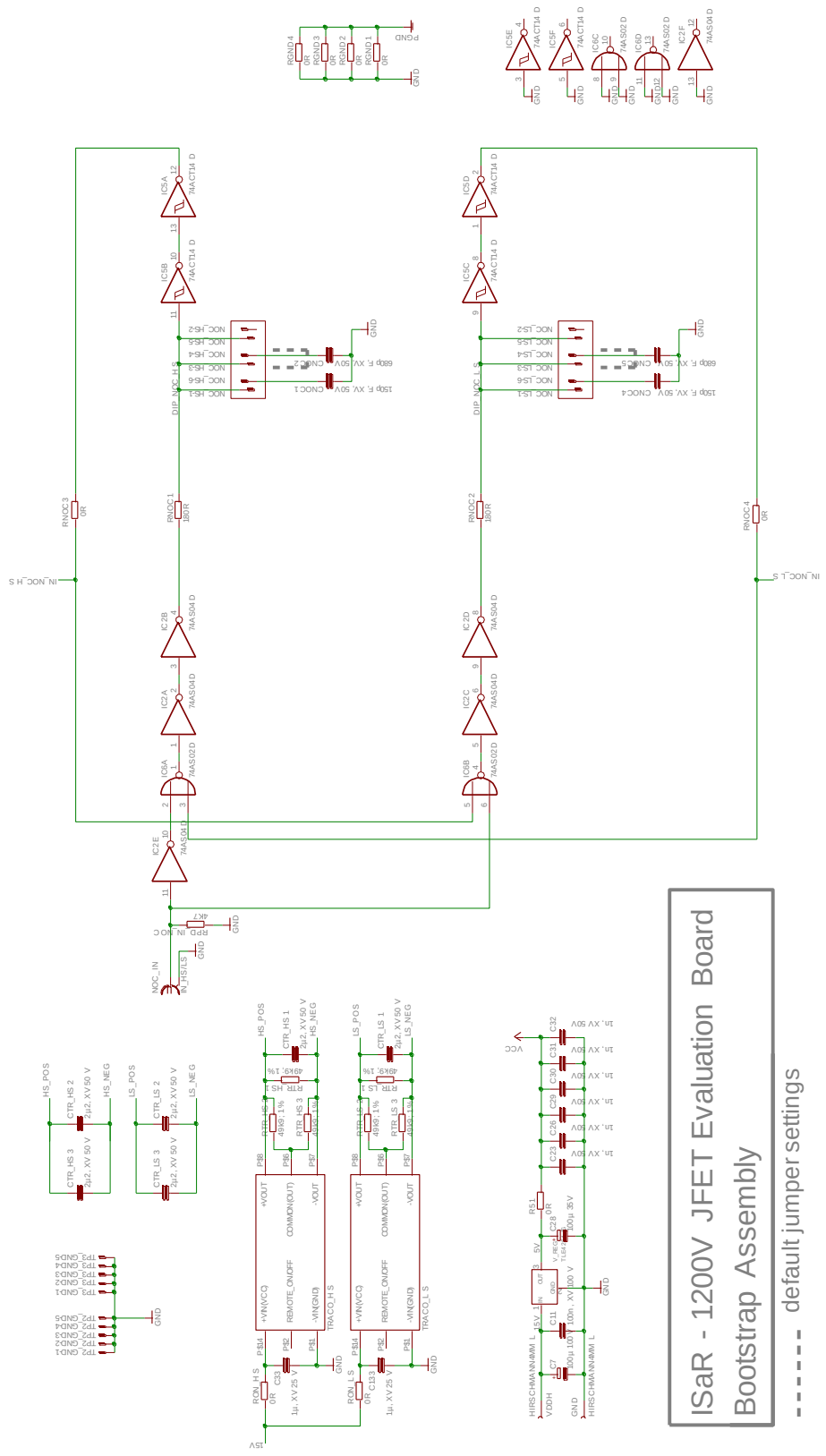


Figure 50 Schematic - Bootstrapping - part 2

Appendix D Board layout

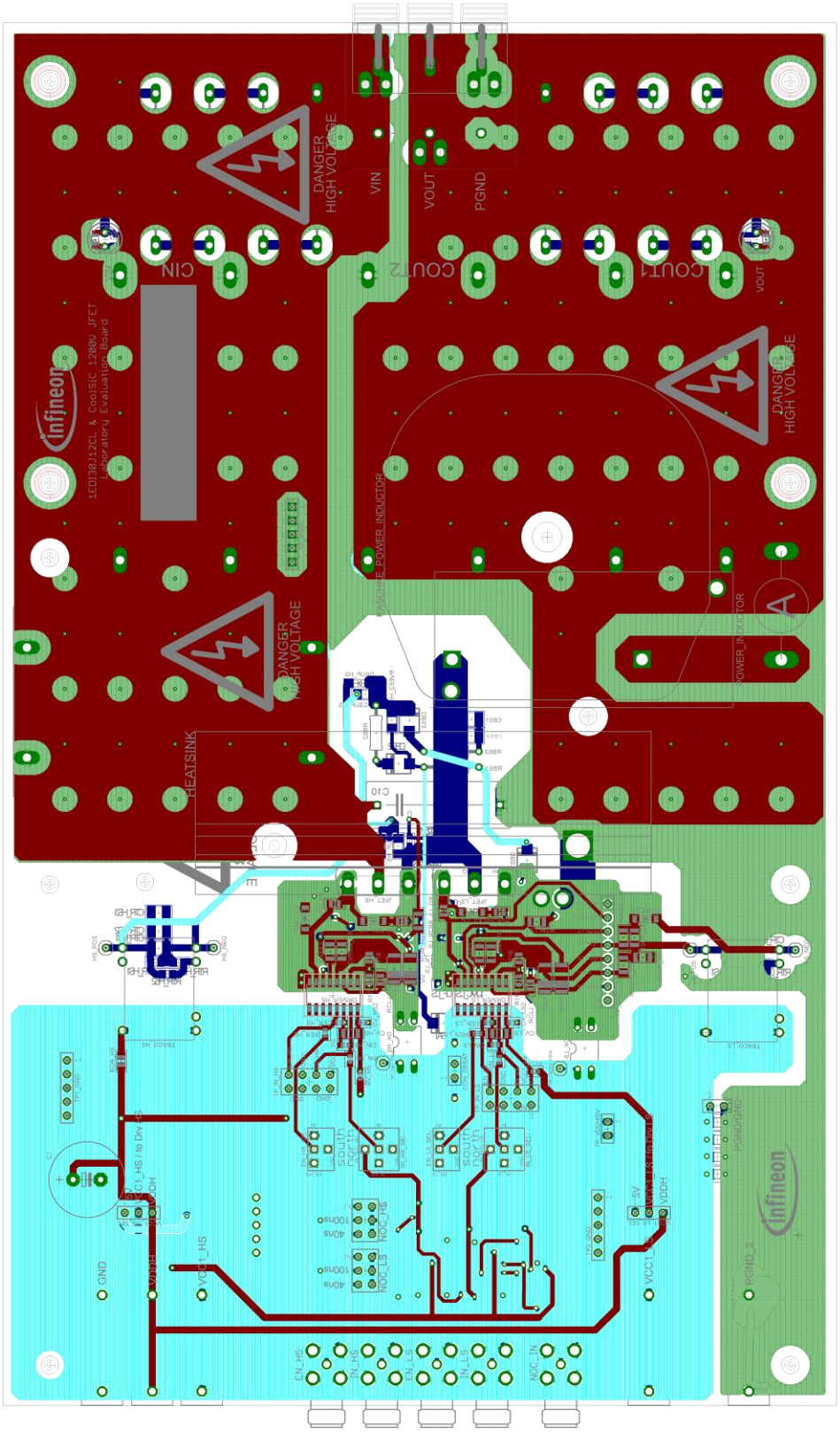


Figure 51 Board Layout - all layers

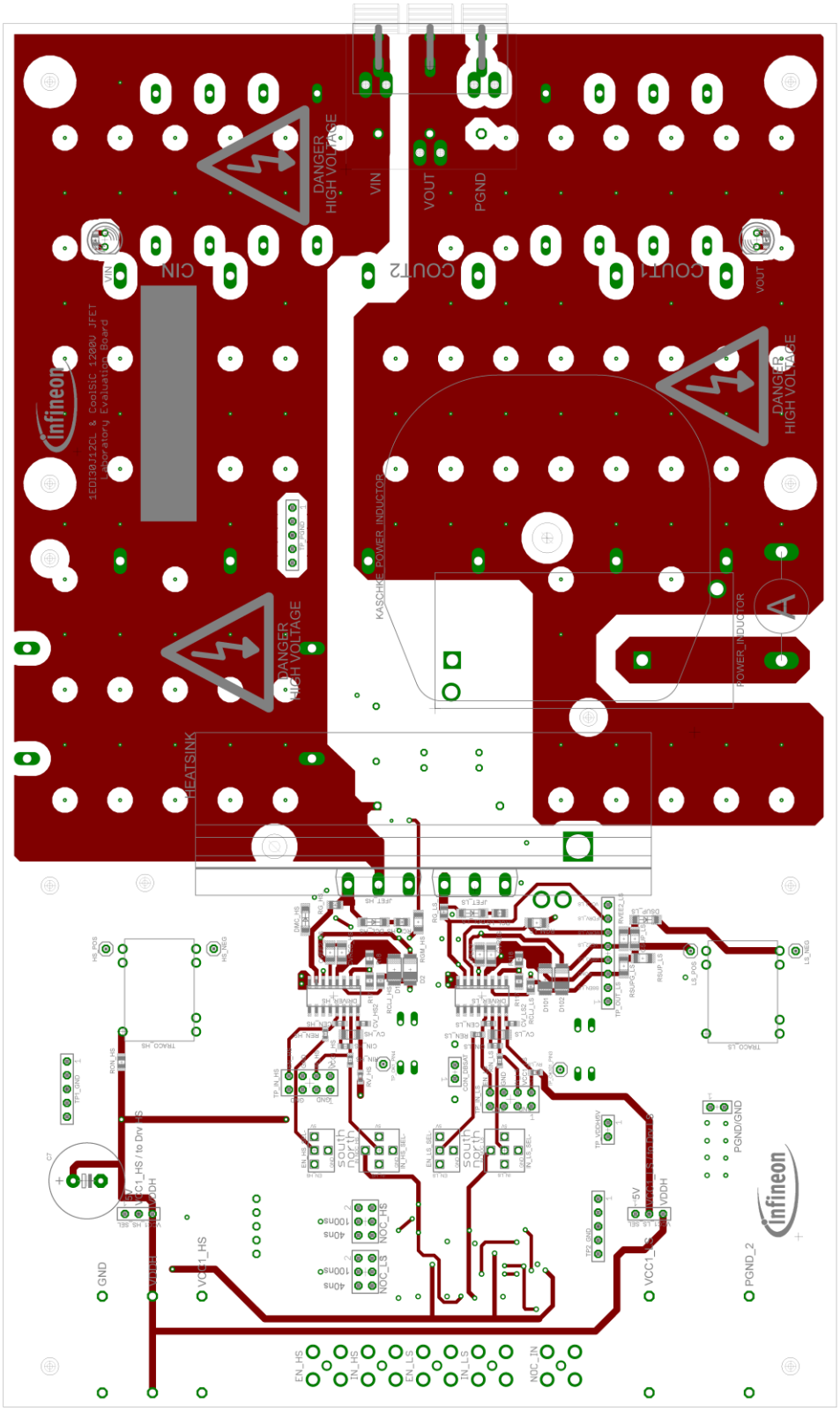


Figure 52 Board Layout - layer 1

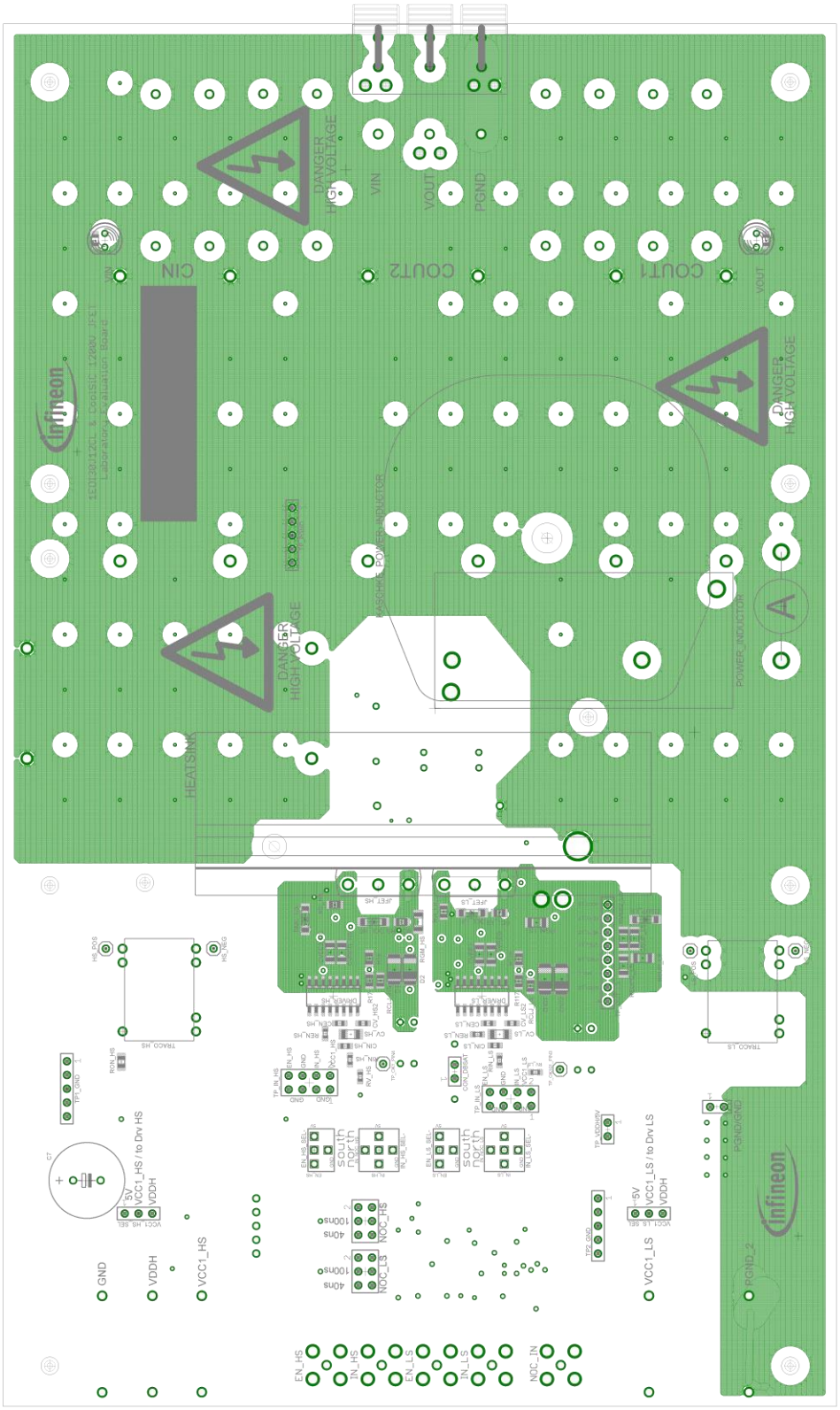


Figure 53 Board Layout - layer 2

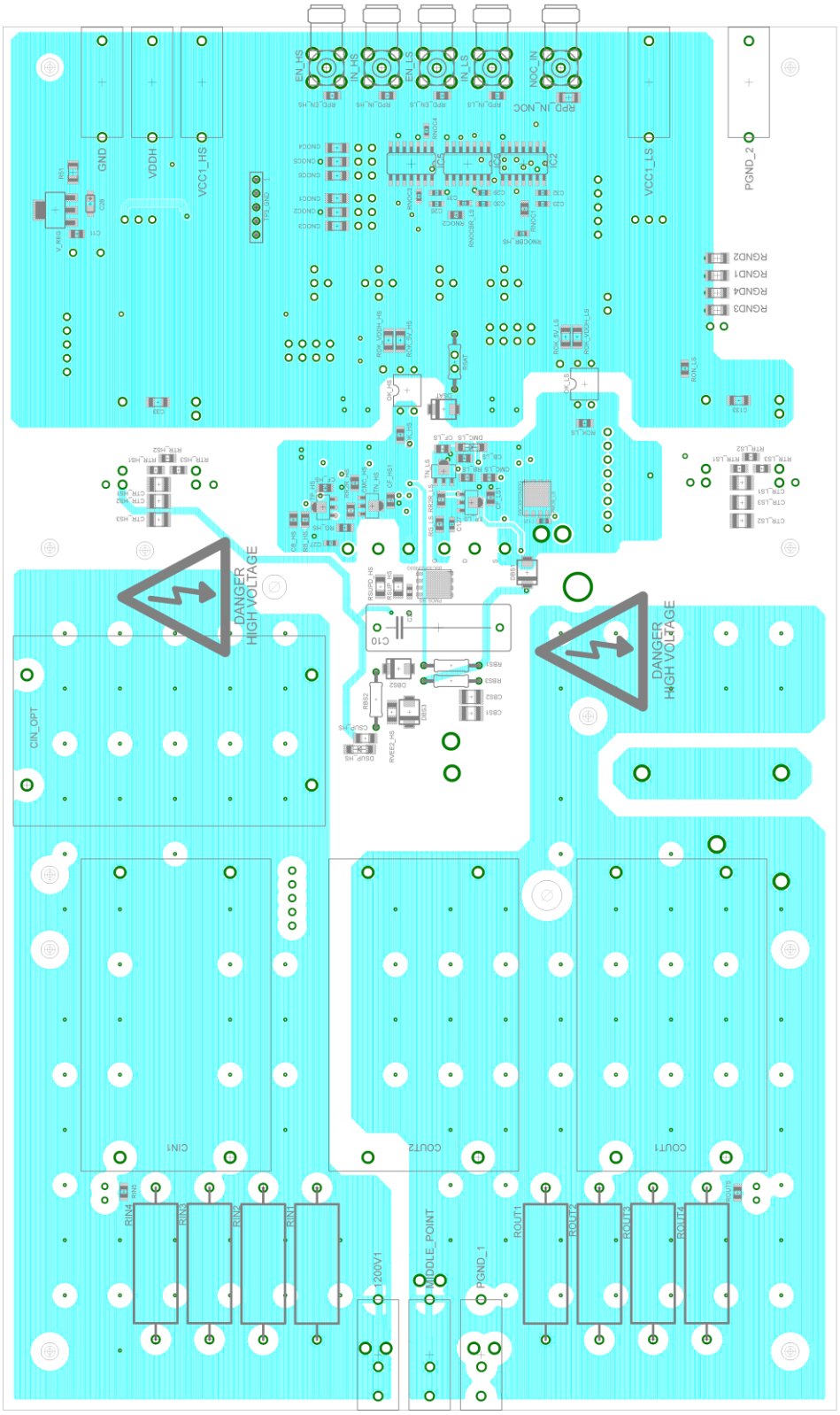


Figure 54 Board Layout - layer 3

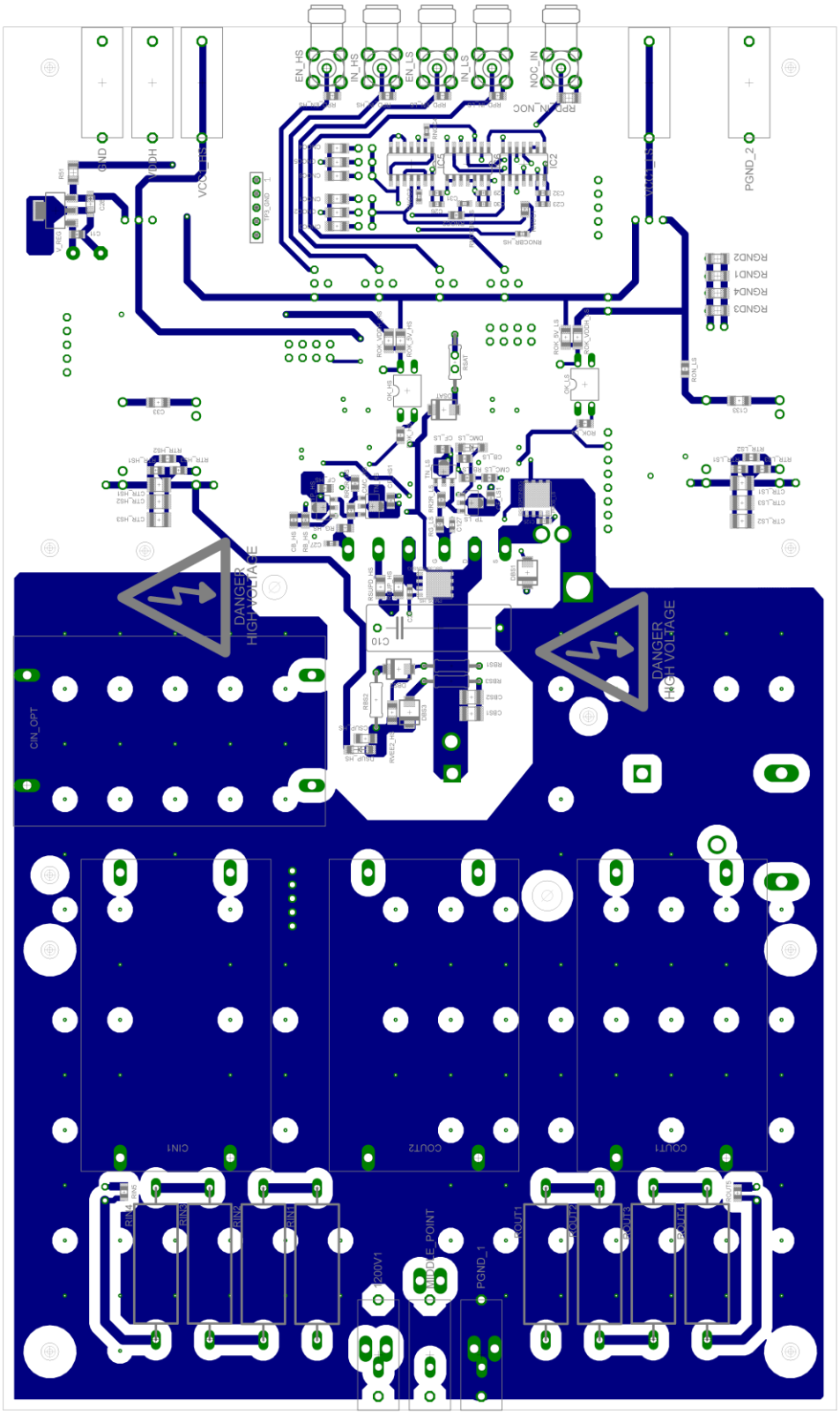


Figure 55 Board Layout - layer 4

Appendix E Bill of Material – Full Schematic

Qty	Value	Device	Parts
5	0R	R-EU_M1206	R51, RGND1, RGND2, RGND3, RGND4
8	0R	R-EU_R0603	REN_HS, REN_LS, RIN_HS, RIN_LS, RNOC3, RNOC4, RV_HS, RV_LS
6	0R	R-EU_R0805	R18, R118, RON_HS, RON_LS
2	0R	R-EU_R1206	RSUP_HS, RSUP_LS
1	0R; NM for BS	R-EU_R1206	RVEE2_HS
2	1µ, XV 25 V	C-EUC1206	C33, C133
4	1µ, XV 50 V	C-EUC1206	CVREG, CVREG_HS, CV_HS, CV_LS
1	100µ 100V	CPOL-EUE5-13	C7
1	100µ 35V	CPOL-EUCT3216	C28
1	100n, 1250V	C-EU225-087X268	C10
1	100n, XV 100 V	C-EUC0805	C11
4	100nF, XV, 50V	C-EUC0805	CF_HS, CF_HS1, CF_LS, CF_LS1
1	10R	R-EU_R1206	RVEE2_LS
2	150pF, XV, 50V	C-EUC1206	CNOC1, CNOC4
2	180R	R-EU_R0805	RNOC1, RNOC2
2	1EDI30J12CL	1EDI30J12CL	DRIVER_HS, DRIVER_LS
6	1n, XV 50V	C-EUC0603	C23, C26, C29, C30, C31, C32
2	2.2R	R-EU_R0805	RB_HS, RB_LS
4	2µ2, XV 50 V	C-EUC1206	CSUP_HS, CSUP_LS, CVEE2, CVEE2_HS
6	2µ2, XV 50 V	C-EUC1210	CTR_HS1, CTR_HS2, CTR_HS3, CTR_LS1, CTR_LS2, CTR_LS3
2	25µ, 1200V	C_4PIN	CIN1, CIN_OPT
2	2R	R-EU_R0805	RG_HS, RG_LS
2	2R	R-EU_R1206	RGM_HS, RGM_LS
2	20R	R-EU_R0805	RCL_HS, RCL_LS
1	360µH	KASCHKE_SDR20-0.15	KASCHKE_POWER_INDUCTOR
6	49k9; 1%	R-EU_R0805	RTR_HS1, RTR_HS2, RTR_HS3, RTR_LS1, RTR_LS2, RTR_LS3
1	4K7	R-EU_M1206	RPD_IN_NOC
4	4K7	R-EU_R0805	RPD_EN_HS, RPD_EN_LS, RPD_IN_HS, RPD_IN_LS
2	4n7, XV 50 V	C-EUC0603	CV_HS2, CV_LS2
2	60µ, 800V	C_4PIN	COUT1, COUT2
1	600V_3WAY	600V_3WAY	U$2
2	680pF, XV, 50V	C-EUC1206	CNOC2, CNOC5
1	74ACT14D	74ACT14D	IC5
1	74AS02D	74AS02D	IC6
1	74AS04D	74AS04D	IC2
8	82K	3W_RESISTOR	RIN1, RIN2, RIN3, RIN4, ROUT1, ROUT2, ROUT3, ROUT4
2	amber	LEDCHIP-LED0805	VIN_, VOUT_
2	BAS16-03W	D-SOD323	DCL_HS, DCL_LS
2	BSC030P03NS3G	BSC030P03NS3G	PMOS_HS, PMOS_LS
4	BU-SMA-H	BU-SMA-H	EN_HS, EN_LS, IN_HS, IN_LS
2	CROSS	Pin Header	IN_HS_SEL-, IN_LS_SEL-
4	ES1A	DIODE-DO-214AC	D1, D2, D101, D102

8	HIRSCHMANN4MML	HIRSCHMANN4MML	1200V1, GND, MIDDLE_POINT, PGND_1, PGND_2, VCC1_HS, VCC1_LS, VDDH
2	IJW120R100T1	JFET_TO247	JFET_HS, JFET_LS
1	IN_HS/LS	BU-SMA-H	NOC_IN
1	IPROBE	IPROBE	U$7
2	LTV816	LTV816	OK_HS, OK_LS
2	N.M.	C-EUC0805	CMC_HS, CMC_LS
4	NM	C-EUC0603	CEN_HS, CEN_LS, CIN_HS, CIN_LS
2	NM	C-EUC0805	CB_HS, CB_LS
2	NM	C-EUC1206	CNOC3, CNOC6
1	NM	R-EU_0207/10	RSAT
6	NM	R-EU_R0805	RIN5, ROUT5, RCLJ_HS, RCLJ_LS, RR2R_HS, RR2R_LS
2	NM; 0R	R-EU_R0603	RNOCBR_HS, RNOCBR_LS
1	NM; 0R for BS	R-EU_R1206	RSUPD_HS
1	NM; 0R for GND rel	R-EU_R1206	RSUPG_LS
2	NM; 0R or optocoupler	R-EU_R0805	R17, R117
2	NM; 0R when using OK	R-EU_R0805	ROK_HS, ROK_LS
3	NM; 10R for BS	R-EU_0207/10	RBS1, RBS2, RBS3
2	NM; 1k for 5V	R-EU_R1206	ROK_5V_HS, ROK_5V_LS
1	NM; 1k for VDDH_HS	R-EU_R1206	ROK_VDDH_HS
1	NM; 1k for VDDH_LS	R-EU_R1206	ROK_VDDH_LS
2	NM; 1R	R-EU_R0805	RG_HS_, RG_LS_
2	NM; 2µ2, XV 100V for BS	C-EUC1210	CBS1, CBS2
2	NM; 22n, XV 50 V	C-EUC0603	C25, C125
2	NM; 4n7, XV 50 V	C-EUC0603	C27, C127
2	NM; PINHD-1x1	Pin Header	TP_OK1_PIN4, TP_OK101_PIN3
1	PHOENIX_PHL-16_3-10-ZF	PHOENIX_PHL-16_3-10-ZF	U$3
4	PINHD 1X1	Pin Header	HS_NEG, HS_POS, LS_NEG, LS_POS
3	PINHD 1x2	Pin Header	CON_DBSAT, PGND/GND, TP_VDDH/5V
2	PINHD 1x3	Pin Header	VCC1_HS_SEL, VCC1_LS_SEL
4	PINHD 1x5	Pin Header	TP1_GND, TP2_GND, TP3_GND, TP_PGND
1	PINHD 1x8	Pin Header	TP_OUT_LS
2	PINHD 2x3	Pin Header	NOC_HS, NOC_LS
2	PINHD 2x4	Pin Header	TP_IN_HS, TP_IN_LS
1	POWER_INDUCTOR	POWER_INDUCTOR	I1
2	rot	LED5MM	VIN, VOUT
4	S1	S1	DMC_HS, DMC_LS, DSUP_HS, DSUP_LS
1	SK481-84	Fischer SK481	U$4
4	STTH112	STTH112	DBS1, DBS2, DBS3, DSAT
2	T	Pin Header	EN_HS_SEL-, EN_LS_SEL-
2	TDR 3-1222 WI	TRACO_TDR3_DUAL	TRACO_HS, TRACO_LS
1	TLE4264-2G	TLE4264-2G	V_REG

Appendix F Bill of Material – Standard Assembly

Qty	Value	Device	Parts
5	0R	R-EU_M1206	R51, RGND1, RGND2, RGND3, RGND4
8	0R	R-EU_R0603	REN_HS, REN_LS, RIN_HS, RIN_LS, RNOC3, RNOC4, RV_HS, RV_LS
4	0R	R-EU_R0805	R18, R118, RON_HS, RON_LS
2	0R	R-EU_R1206	RSUP_HS, RSUP_LS
1	0R; NM for BS	R-EU_R1206	RVEE2_HS
2	1µ, XV 25 V	C-EUC1206	C33, C133
4	1µ, XV 50 V	C-EUC1206	CVREG, CVREG_HS, CV_HS, CV_LS
1	100µ 100V	CPOL-EUE5-13	C7
1	100µ 35V	CPOL-EUCT3216	C28
1	100n, 1250V	C-EU225-087X268	C10
1	100n, XV 100 V	C-EUC0805	C11
4	100nF, XV, 50V	C-EUC0805	CF_HS, CF_HS1, CF_LS, CF_LS1
1	10R	R-EU_R1206	RVEE2_LS
2	150pF, XV, 50V	C-EUC1206	CNOC1, CNOC4
2	180R	R-EU_R0805	RNOC1, RNOC2
2	1EDI30J12CL	1EDI30J12CL	DRIVER_HS, DRIVER_LS
6	1n, XV 50V	C-EUC0603	C23, C26, C29, C30, C31, C32
2	2.2R	R-EU_R0805	RB_HS, RB_LS
4	2µ2, XV 50 V	C-EUC1206	CSUP_HS, CSUP_LS, CVEE2, CVEE2_HS
6	2µ2, XV 50 V	C-EUC1210	CTR_HS1, CTR_HS2, CTR_HS3, CTR_LS1, CTR_LS2, CTR_LS3
1	25µ, 1200V	C_4PIN	CIN1
2	2R	R-EU_R0805	RG_HS, RG_LS
2	2R	R-EU_R1206	RGM_HS, RGM_LS
2	20R	R-EU_R0805	RCL_HS, RCL_LS
1	360µH	KASCHKE_SDR20-0.15	KASCHKE_POWER_INDUCTOR
2	39R	R-EU_R0805	RR2R_HS, RR2R_LS
6	49k9; 1%	R-EU_R0805	RTR_HS1, RTR_HS2, RTR_HS3, RTR_LS1, RTR_LS2, RTR_LS3
1	4K7	R-EU_M1206	RPD_IN_NOC
4	4K7	R-EU_R0805	RPD_EN_HS, RPD_EN_LS, RPD_IN_HS, RPD_IN_LS
2	4n7, XV 50 V	C-EUC0603	CV_HS2, CV_LS2
2	60µ, 800V	C_4PIN	COUT1, COUT2
2	680pF, XV, 50V	C-EUC1206	CNOC2, CNOC5
1	74ACT14D	74ACT14D	IC5
1	74AS02D	74AS02D	IC6
1	74AS04D	74AS04D	IC2
8	82K	3W_RESISTOR	RIN1, RIN2, RIN3, RIN4, ROUT1, ROUT2, ROUT3, ROUT4
2	BAS16-03W	D-SOD323	DCL_HS, DCL_LS
2	BSC030P03NS3G	BSC030P03NS3G	PMOS_HS, PMOS_LS
4	BU-SMA-H	BU-SMA-H	EN_HS, EN_LS, IN_HS, IN_LS
2	CROSS	Pin Header	IN_HS_SEL-, IN_LS_SEL-
4	ES1A	DIODE-DO-214AC	D1, D2, D101, D102
4	HIRSCHMANN4MML	HIRSCHMANN4MML	GND, VCC1_HS, VCC1_LS, VDDH

2	IJW120R070T1	JFET_TO247	JFET_HS, JFET_LS
1	IN_HS/LS	BU-SMA-H	NOC_IN
1	IPROBE	IPROBE	U$7
1	PHOENIX_PHL-16_3-10-ZF	PHOENIX_PHL-16_3-10-ZF	U$3
4	PINHD 1X1	Pin Header	HS_NEG, HS_POS, LS_NEG, LS_POS
2	PINHD 1x3	Pin Header	VCC1_HS_SEL, VCC1_LS_SEL
2	PINHD 1x5	Pin Header	TP2_GND, TP3_GND
1	PINHD 1x8	Pin Header	TP_OUT_LS
2	PINHD 2x3	Pin Header	NOC_HS, NOC_LS
2	PINHD 2x4	Pin Header	TP_IN_HS, TP_IN_LS
2	rot	LED5MM	VIN, VOUT
2	S1	S1	DSUP_HS, DSUP_LS
1	SK481-84	Fischer SK481	U$4
2	T	Pin Header	EN_HS_SEL-, EN_LS_SEL-
2	TDR 3-1222 WI	TRACO_TDR3_DUAL	TRACO_HS, TRACO_LS
1	TLE4264-2G	TLE4264-2G	V_REG
2	ZXTN2010Z	ZXTN2010Z	TN_HS, TN_LS
2	ZXTP2012Z	ZXTP2012Z	TP_HS, TP_LS

Appendix G Bill of Material – Bootstrapping

Qty	Value	Device	Parts
2	0R	R-EU_R0805	RON_HS, RON_LS
5	0R	R-EU_M1206	R51, RGND1, RGND2, RGND3, RGND4
8	0R	R-EU_R0603	REN_HS, REN_LS, RIN_HS, RIN_LS, RNOC3, RNOC4, RV_HS, RV_LS
1	0R for BS	R-EU_R1206	RSUPD_HS
1	0R or optocoupler	R-EU_R0805	R17
1	0R or optocoupler	R-EU_R0805	R117
1	0R when using OK	R-EU_R0805	ROK_HS
1	0R when using OK	R-EU_R0805	ROK_LS
2	1µ, XV 25 V	C-EUC1206	C33, C133
4	1µ, XV 50 V	C-EUC1206	CVREG, CVREG_HS, CV_HS, CV_LS
1	100µ 100V	CPOL-EUE5-13	C7
1	100µ 35V	CPOL-EUCT3216	C28
1	100n, 1250V	C-EU225-087X268	C10
1	100n, XV 100 V	C-EUC0805	C11
4	100nF, XV, 50V	C-EUC0805	CF_HS, CF_HS1, CF_LS, CF_LS1
1	10R	R-EU_R1206	RVEE2_LS
2	10R for BS	R-EU_0207/10	RBS2, RBS3
2	150pF, XV, 50V	C-EUC1206	CNOC1, CNOC4
2	180R	R-EU_R0805	RNOC1, RNOC2
2	1EDI30J12CL	1EDI30J12CL	DRIVER_HS, DRIVER_LS
2	1k for 5V	R-EU_R1206	ROK_5V_HS, ROK_5V_LS
1	1k for VDDH	R-EU_R1206	ROK_VDDH_HS
1	1k for VDDH_LS	R-EU_R1206	ROK_VDDH_LS
6	1n, XV 50V	C-EUC0603	C23, C26, C29, C30, C31, C32
2	2.2R	R-EU_R0805	RB_HS, RB_LS
2	2µ2, XV 100V for BS	C-EUC1210	CBS1, CBS2
4	2µ2, XV 50 V	C-EUC1206	CSUP_HS, CSUP_LS, CVEE2, CVEE2_HS
6	2µ2, XV 50 V	C-EUC1210	CTR_HS1, CTR_HS2, CTR_HS3, CTR_LS1, CTR_LS2, CTR_LS3
1	25µ, 1200V	C_4PIN	CIN1
2	2R	R-EU_R0805	RG_HS, RG_LS
2	2R	R-EU_R1206	RGM_HS, RGM_LS
2	20R	R-EU_R0805	RCL_HS, RCL_LS
1	360µH	KASCHKE_SDR20-0.15	KASCHKE_POWER_INDUCTOR
2	39R	R-EU_R0805	RR2R_HS, RR2R_LS
6	49k9; 1%	R-EU_R0805	RTR_HS1, RTR_HS2, RTR_HS3, RTR_LS1, RTR_LS2, RTR_LS3
1	4K7	R-EU_M1206	RPD_IN_NOC
4	4K7	R-EU_R0805	RPD_EN_HS, RPD_EN_LS, RPD_IN_HS, RPD_IN_LS
2	4n7, XV 50 V	C-EUC0603	CV_HS2, CV_LS2
2	60µ, 800V	C_4PIN	COUT1, COUT2
1	600V_3WAY	600V_3WAY	U$2
2	680pF, XV, 50V	C-EUC1206	CNOC2, CNOC5
1	74ACT14D	74ACT14D	IC5

1	74AS02D	74AS02D	IC6
1	74AS04D	74AS04D	IC2
8	82K	3W_RESISTOR	RIN1, RIN2, RIN3, RIN4, ROUT1, ROUT2, ROUT3, ROUT4
2	BAS16-03W	D-SOD323	DCL_HS, DCL_LS
2	BSC030P03NS3G	BSC030P03NS3G	PMOS_HS, PMOS_LS
4	BU-SMA-H	BU-SMA-H	EN_HS, EN_LS, IN_HS, IN_LS
2	CROSS	Pin Header	IN_HS_SEL-, IN_LS_SEL-
4	ES1A	DIODE-DO-214AC	D1, D2, D101, D102
4	HIRSCHMANN4MML	HIRSCHMANN4MML	GND, VCC1_HS, VCC1_LS, VDDH
2	IJW120R070T1	JFET_TO247	JFET_HS, JFET_LS
1	IN_HS/LS	BU-SMA-H	NOC_IN
1	IPROBE	IPROBE	U$7
2	LTV816	LTV816	OK_HS, OK_LS
1	PHOENIX_PHL-16_3-10-ZF	PHOENIX_PHL-16_3-10-ZF	U$3
2	PINHD 1X1	Pin Header	TP_OK1_PIN4, TP_OK101_PIN3
4	PINHD 1X1	Pin Header	HS_NEG, HS_POS, LS_NEG, LS_POS
2	PINHD 1x3	Pin Header	VCC1_HS_SEL, VCC1_LS_SEL
2	PINHD 1x5	Pin Header	TP2_GND, TP3_GND
1	PINHD 1x8	Pin Header	TP_OUT_LS
2	PINHD 2x3	Pin Header	NOC_HS, NOC_LS
2	PINHD 2x4	Pin Header	TP_IN_HS, TP_IN_LS
2	rot	LED5MM	VIN, VOUT
2	S1	S1	DSUP_HS, DSUP_LS
1	SK481-84	Fischer SK481	U$4
3	STTH112	STTH112	DBS1, DBS2, DBS3
2	T	Pin Header	EN_HS_SEL-, EN_LS_SEL-
2	TDR 3-1222 WI	TRACO_TDR3_DUAL	TRACO_HS, TRACO_LS
1	TLE4264-2G	TLE4264-2G	V_REG
2	ZXTN2010Z	ZXTN2010Z	TN_HS, TN_LS
2	ZXTP2012Z	ZXTP2012Z	TP_HS, TP_LS