AN201081

S29JL064J Package Routing Guide

AN201081 provides a general routing guide for packages (substrate/leadframe) designed with S29JL064J die.

1 Introduction

This document is meant to provide a general routing guide for packages (substrate/leadframe) designed with S29JL064J die.

This document does not eliminate the need for customer signal integrity/power delivery simulations. Customer should use Cypress® provided IBIS models for signal timing/crosstalk analysis.

2 Signal Descriptions

The following table describes various pads utilized in S29JL064J die.

Signal/Supply pad name	Description
A21-A0	Address inputs
DQ15-DQ0	Data I/O
CE#	Chip Enable Input
OE#	Output Enable Input
WE#	Write Enable Input
WP#/ACC	Program Acceleration input/Hardware Write Protect input
RY/BY#	Ready/Busy output (open sink)
BYTE#	Selects 8-bit or 16-bit mode
RESET#	Hardware Reset input
VCCQ	I/O Power supply (2.7V-3.6V)
VCC	Core power supply (2.7V-3.6V)
VSS	Core ground
VSSQ	I/O ground

3 Signal Groupings

The following table describes various signal/supply groupings to assist in package routing/signal integrity simulations.

Signal/Supply group	Description
A21-A0	Address inputs
DQ15-DQ0	Data I/O
CE#, OE#, WE#	Control signals
WP#/ACC, RY/BY#, /BYTE#, RESET#	Miscellaneous
VCCQ, VCC, VSS, VSSQ	Supply

4 Supply Routing Guidelines

Customers are recommended to meet or beat below supply routing recommendations.

1. Provide a dedicated V_{CC} ball/pin for the V_{CC} pad and a dedicated $V_{CC}Q$ ball/pin for the $V_{CC}Q$ pad.
2. Provide at least two dedicated V_{SS} balls/pins for flash. The two V_{SS} balls/pins should be shorted together in the substrate. It is ok to short V_{SS} and $V_{SS}Q$ in the substrate.
   In case of a leadframe design, shorting all $V_{SS}/V_{SS}Q$ pads in the leadframe maybe improbable. It is recommended in that case to short pads 27 and 28 to a pin/ball and to short pads 48 and 49 to a pin/ball.
3. Maintain a low inductance/resistance path from each supply pad (V_{CC}, V_{SS} or $V_{CC}Q$) to solder ball/pin.
4. It is recommended to keep path inductance for each of the supply nets (from each supply pad to its solder ball/pin) ≤ 3.5 nH.
5. It is recommended to keep path resistance for each of the supply nets (from each supply pad to its solder ball/pin) ≤ 150 mΩ.
6. Except for necking/bondfinger breakout region, please maintain supply ($V_{CC}/V_{CC}Q/V_{SS}$) trace width ≥ 100 µm (wider the better).
7. Route V_{CC} and/or $V_{CC}Q$ close to V_{SS} trace (regardless of the bondwire location) to maintain V_{CC}-V_{SS} and $V_{CC}Q$-V_{SS} inductance loop constant. In general a 50 µm separation between V_{CC}/V_{SS} supply traces is ideal whenever possible.
8. Select V_{CC} and V_{SS} solder ball location next to each other on the ball map (Same comment applies for $V_{CC}Q$ and V_{SS}).
9. While doing layer transitions in a BGA substrate use dual vias as much as possible to reduce via current crowding.

5 Signal Routing Guidelines

Customers are recommended to meet or beat below signal routing recommendations.

1. Maintain all DQ routing within ± 1 nH of each other. Limit DQ routing to ≤ 5 nH.
2. Maintain all address routing within ± 1 nH of each other. Limit address routing to ≤ 6.5 nH.
3. Keep all DQ routing within ± 1 nH of /WE. Maintain all address routing within ± 2 nH of WE#.
4. CE# and OE# routing should be limited to ≤ 5.5 nH.
5. Route all other signal as short as possible (≤ 8 nH).
6. As much as possible, maintain via count on all signals within a signal group (DQ and address only) similar.
7. RY/BY# pin should be connected to a 6.2 kΩ resistor to V_{CC} on the system board.

6 Multi-Chip Package Routing

If S29JL064J die is used along with other (non-flash) dies in a single MCP, following routing recommendations should be followed in addition to those in Section 4 and Section 5

1. It is recommended to keep flash $V_{CC}/V_{CC}Q/V_{SS}$ separate from other die/interface $V_{CC}/V_{CC}Q/V_{SS}$ (routing as well as solderball/pin allocations).
2. It maybe possible to share V_{SS} between Cypress flash and PSRAM die (if present) provided PSRAM speed doesn't exceed flash speed. Controller V_{SS} can only be shared if it pertains to flash interface only. Do not share V_{SS} between different interfaces (e.g. DDR and flash).
3. Provide V_{SS} shielding between flash traces/supplies and other interface supply/signal traces (150 µm minimum trade width).
4. If signals are shared with another die such as PSRAM/controller the following general routing rules should be used;
   a. All address/inputs should be routed in Y configuration. Maintain the overall inductance from pad to ball within guidelines specified in Section 4 and Section 5 However the fork lengths going to both

dies should be electrically matched (provided both dies have similar input capacitance. If they have different input capacitances, IBIS simulations need to be performed to determine fork lengths).

b. All DQ topologies need to be simulated to provide adequate topology (daisy chain or Y). However it is recommended that flash path inductance from signal pad to ball/pin follows guidelines specified in Section 4 and Section 5

Document History Page

Document Title: AN201081 - S29JL064J Package Routing Guide Document Number: 002-01081				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	01/19/2011	Initial version
*A	4992578	MSWI	10/28/2015	Updated in Cypress template
*B	5870072	AESATMP8	09/01/2017	Updated logo and Copyright.

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at Cypress Locations.

Products

ARM® Cortex® Microcontrollers	cypress.com/arm
Automotive	cypress.com/automotive
Clocks & Buffers	cypress.com/clocks
Interface	cypress.com/interface
Internet of Things	cypress.com/iot
Memory	cypress.com/memory
Microcontrollers	cypress.com/mcu
PSoC	cypress.com/psoc
Power Management ICs	cypress.com/pmic
Touch Sensing	cypress.com/touch
USB Controllers	cypress.com/usb
Wireless Connectivity	cypress.com/wireless

PSoC® Solutions

PSoC 1 | PSoC 3 | PSoC 4 | PSoC 5LP | PSoC 6

Cypress Developer Community

Forums | WICED IOT Forums | Projects | Video | Blogs | Training | Components

Technical Support

cypress.com/support

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709