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Spec No: 002-00973

Spec Title: AN200973 - INTERFACING CYPRESS FLASH TO TI OMAP PROCESSORS

Replaced by: NONE

AN200973

Interfacing Cypress Flash to TI OMAP Processors

AN200973 discusses how to interface a Cypress flash device with the Texas Instruments OMAP3503 processor(OMAP3503/3515/3525/3530).

1 Introduction

This application note assumes that the reader is familiar with asynchronous, page, and synchronous flash memory timings. The Texas Instrument OMAP3503 processor is used as example in this application note. OMAP3503/3515/3525/3530 are TI's OMAP families.

General-purpose memory controllers (GPMC) are used for the basic memory controller. NOR flash/NAND flash / SDRAM are all controlled by general-purpose memory controller (GPMC).

The following flash are covered in this file:

Family	Technology	I/O Voltage	Address and Data Interface
S29VS-R	65 nm MirrorBit® Technology	Single 1.8V	Address and Data Multiplexed (ADM)
S29WS-P	90 nm MirrorBit Technology	Single 1.8V	Address Data Parallel (ADP) Interface
S29GL-P	90 nm MirrorBit Technology	Versatile I/O Feature	Address Data Parallel (ADP)
S29GL-S	65 nm MirrorBit Technology	Versatile I/O Feature	Address Data Parallel (ADP) Interface

The S29GL-P and S29GL-S families are both asynchronous mode. The S29VS-R and S29WS-P families can support synchronous mode.

The current OMAP™ processor supports GPMC connection to address/data multiplexed-memory, address/data non-multiplexed memory with limited address (2 kbytes), and a NAND device:

The S29VS-R can be connected directly to OMAP3503, but S29WSP, S29GL-S, and S29GL-P need special logic glue to OMAP3503 since they support ADP interface.

The maximum density per chip-select is 1-Gbit NOR flash.

The interface width is 16 bits. Both the S29GL-P and S29GL-S support a 16-bit bus.

The OMAP I/O voltage 1.8V LVCMOS and Versatile I/O features are both supported. For the S29GL-P and S29GL-S to meet this requirement needs a Wide I/O voltage range (V_{IO}): 1.65V to V_{CC}.

Additionally, the signals required to interface to the Cypress flash, the configuration required for the interface, the registers in both the OMAP processor and the flash that need to be programmed, and the interface timing are described below.

2 Interface Signals

The general-purpose memory controller (GPMC) is the OMAP™2 unified memory controller (UMC) dedicated to interfacing external memory devices.

The GPMC supports up to 8 chip-select regions of programmable size, and programmable base addresses in a total address space of 1 Gbyte.

Table 1 describes the processor's flash signals.

Table 1. Flash Signals

Signal Name	I/O	Description
gpmc_clk	I/O	External clock provided to the external device for synchronous operations
gpmc_a[10: 1]	O	Address a[26:17]
gpmc_d[15: 0]	I/O	Data-multiplexed with addresses A[16:1] on memory side
gpmc_ncs[7:0]	O	Chip-select
gpmc_nadv_ale	O	Address Valid or Address Latch
gpmc_noe_nre	O	Output enable (read access only)
gpmc_nwe	O	Write enable (write access only)
gpmc_wait[3:0]	I	Ready signal from memory device. Indicates when valid burst data is ready to be read
gpmc_nbe0_cle	O	Lower Byte Enable. Also used for Command Latch Enable.
gpmc_nbe1	O	Upper Byte Enable
gpmc_nwp	O	Flash Write Protect
gpmc_wait[3:0]	I	External indication of wait

Reset values of the timing control parameters are defined to cope with direct boot on address and data multiplexed NOR flash devices, on non-multiplexed NOR flash devices, or on any asynchronous device with large timing margins assuming a low GPMC_FCLK frequency (for example, 19.2 MHz) at boot time.

3 Configuration Overview

The GPMC is the OMAP2 16-bit external memory controller. The GPMC data access engine provides a flexible programming model for communication with all standard memories. The GPMC supports various accesses.

The GPMC supports the following interface protocols when communicating with external Nor flash memory:

- Asynchronous read/write access
- Synchronous read/burst read
- Synchronous read burst access without wrap capability (4-8-16 Word16)
- Synchronous read burst access with wrap capability (4-8-16 Word16)

3.1 GPMC I/O Configuration Setting

The address/data non-multiplexed device, which is limited to a 2 kbyte address range:

- GPMC.GPMC_CONFIG1_i[11:10] DEVICETYPE field = 0x00
- GPMC.GPMC_CONFIG1_i[9] MUXADDDATA bit = 0
- GPMC.GPMC_CONFIG[1] LIMITEDADDRESS bit = 1

To select the address/data-multiplexed device, program the following register fields:

- GPMC.GPMC_CONFIG1_i[11:10] DEVICETYPE field = 0b00
- GPMC.GPMC_CONFIG1_i[9] MUXADDDATA bit = 1

3.2 Asynchronous and Synchronous Access

Read access can be specified as either asynchronous or synchronous access:

- GPMC.GPMC_CONFIG1_i[29] READTYPE bit (i = 0 to 7)

3.3 Page and Burst Support

Read accesses can be configured through the GPMC_CONFIG1_i[30] READMULTIPLE

The maximum length that can be issued is defined per CS by the GPMC.GPMC_CONFIG1_i[24:23] ATTACHEDDEVICEPAGELENGTH field (i= 0 to7).

16 Word16-length-wrapping burst capability (critical word access first), the ATTACHEDDEVICEPAGELENGTH parameter must be set to 16 words and the GPMC.GPMC_CONFIG1_i[31] WRAPBURST bit (i = 0 to 7) must be set to 1.

4 Asynchronous Access Example

In asynchronous operations:

- GPMC_CLK is not provided outside the GPMC
- GPMC_CLK is kept low

Page mode is only available in non-muxed mode. The non-muxed mode is very limited (address space limited to 2 kbytes). So only muxed mode are covered here.

4.1 Asynchronous Single Read

Asynchronous single read operation on an address/data-multiplexed device.

When the GPMC generates a read access to an address/data-multiplexed device, it drives the address bus until nOE assertion time.

- GPMC.GPMC_CONFIG1_i register settings (i = 0 to 7):
  - READMULTIPLE bit at 0 (read single access)
  - READTYPE bit at 0 (read asynchronous)
  - MUXADDDATA bit at 1 (address/data-multiplexed device)

Address bits ([16:1] from a GPMC perspective, [15:0] from an external device perspective) are placed on the address/data bus, and the remaining address bits [25:16] are placed on the address bus. The address phase ends at nOE assertion, when the DIR signal goes from OUT to IN.

- Chip-select signal nCS:
  - nCS assertion time is controlled by the GPMC_CONFIG2_i[3:0] CSOnTime field. It controls the address setup time to nCS assertion.
  - nCS deassertion time is controlled by the GPMC_CONFIG2_i[12:8] CSRdOffTime field. It controls the address hold time from nCS deassertion.
- Address valid signal nADV:
  - nADV assertion time is controlled by the GPMC_CONFIG3_i[3:0] ADVOnTime field.
  - nADV deassertion time is controlled by the GPMC_CONFIG3_i[12:8] ADVRdOffTime field.
- Output enable signal nOE:
  - nOE assertion indicates a read cycle.
  - nOE assertion time is controlled by the GPMC_CONFIG4_i[3:0] OEOnTime field.
  - nOE deassertion time is controlled by the GPMC_CONFIG4_i[12:8] OEOffTime field.
- Read data is latched when RdAccessTime completes. Access time is defined in the GPMC.GPMC_CONFIG5_i[20:16] RdAcessTime field.
- The end of the access is defined by the RdCycleTime parameter. The read cycle time is defined in the GPMC.GPMC_CONFIG5_i[4:0] RdCycleTime field.
- Direction signal DIR: DIR goes from OUT to IN at the same time that nOE is asserted.

4.2 Asynchronous Single Write

Asynchronous single write operation on an address/data-multiplexed device.

When the GPMC generates a write access to an address/data-multiplexed device, it drives the address on the address/data muxed bus until WRDATAONADMUXBUS time, and then it drives the data.

- GPMC.GPMC_CONFIG1_i register settings (i = 0 to 7):
  - WRITEMULTIPLE bit at 0 (write single access)
  - WRITETYPE bit at 0 (write asynchronous)
  - MUXADDDATA bit at 1 (address/data-multiplexed device)

Address bits [16:1] are placed on the address/data bus at the start of cycle time, and the remaining address bits [26:17] are placed on the address bus.

- Chip-select signal nCS:
  - nCS assertion time is controlled by the GPMC.GPMC_CONFIG2_i[3:0] CSOnTime field and ensures address setup time to nCS assertion.
  - nCS deassertion time is controlled by the GPMC.GPMC_CONFIG2_i[20:16] CSWrOffTime field and ensures address hold time to nCS deassertion.
- Address valid signal nADV:
  - nADV assertion time is controlled by the GPMC.GPMC_CONFIG3_i[3:0] ADVOnTime field.
  - nADV deassertion time is controlled by the GPMC.GPMC_CONFIG3_i[20:16] ADVWrOffTime field.

Address and data are driven on their corresponding buses at start-of-cycle time.

- Write enable signal nWE:
  - nWE assertion indicates a write cycle.
  - nWE assertion time is controlled by the GPMC.GPMC_CONFIG4_i[19:16] WEOnTime field.
  - nWE deassertion time is controlled by the GPMC.GPMC_CONFIG4_i[28:24] WEOffTime field.
- Direction signal DIR:

DIR signal is OUT during the entire access.

- The end of the access is defined by the WRCYCLETIME parameter. This write-cycle time is defined in the GPMC.GPMC_CONFIG5_i[12:8] WrCycleTimefield.

5 Synchronous Access Example

In synchronous operations:

- The GPMC_CLK clock is provided outside the GPMC when accessing the memory device.
- The GPMC_CLK clock is derived from the GPMC_FCLK clock using the GPMC.GPMC_CONFIG1_i[1:0] GpmcFCLKDivider field (where i = 0 to 7).
- The GPMC.GPMC_CONFIG1_i[26:25] ClkActivationTime field specifies that the GPMC_CLK is provided outside the GPMC 0, 1, or 2 GPMC_FCLK cycles after start access time until CycleTime completes.
- When the GPMC is configured for synchronous mode, the GPMC_CLK signal (which is an output) must also be set as an input (CONTROL.CONTROL_PADCONF_GPMC_NCS7[24] INPUTENABLE1 =1). GPMC_CLK is looped back through the output and input buffers of the corresponding GPMC_CLK pad at OMAP boundary. The looped-back clock is used to synchronize the sampling of the memory signals.

5.1 Register Setting for S29VS-R

Table 2. Configuration Register

CR Bit	Function	Settings (Binary)
CR.15	Device Read Mode	0 = Synchronous Read Mode 1 = Asynchronous Read Mode (Default)
CR.14 CR.13 CR.12 CR.11	Programmable Read Wait States	0000 = Reserved 0001 = Initial data is valid on the 3rd rising CLK edge after addresses are latched 0010 = 4th 0011 = 5th ⋮ ⋮ 1011 = 13th (Default) 1100 = Reserved 1101 = Reserved 1110 = Reserved 1111 = Reserved
CR.10	RDY Polarity	0 = RDY signal is active low 1 = RDY signal is active high (Default)
CR.9	Reserved	0 = Reserved 1 = Reserved (Default)
CR.8	RDY Timing	0 = RDY active one clock cycle before data 1 = RDY active with data (Default)
CR.7	Output Drive Strength	0 = Full Drive= Current Driver Strength (Default) 1 = Half Drive
CR.6	Reserved	0 = Reserved 1 = Reserved (Default)
CR.5	Reserved	0 = Reserved (Default) 1 = Reserved
CR.4	Reserved	0 = Reserved (Default) 1 = Reserved
CR.3	Reserved	0 = Reserved 1 = Reserved (Default)
CR.2 CR.1 CR.0	Burst Length	000 = Continuous (Default) 010 = 8-word (16-byte) Linear Burst with wrap around 011 = 16-word (32-byte) Linear Burst with wrap around (All other bit settings are reserved)

5.2 Synchronous Multiple Read (Burst)

Synchronous multiple read operation with GpmcFCLKDivider equal to 0 and 1, respectively.

- GPMC.GPMC_CONFIG1_i register settings:
  - READMULTIPLE bit at 1 (read multiple access)
  - READTYPE bit at 1 (read synchronous)
  - MUXADDDATA bit at 0 (nonaddress/data-multiplexed device)

When RDACCESSTIME completes, control-signal timings are frozen during the multiple data transactions, corresponding to PageBurstAccessTime multiplied by the number of remaining data transactions.

- Chip-select signal nCS:

  - nCS assertion time is controlled by the GPMC.GPMC_CONFIG2_i[3:0] CSOnTime field and ensures address setup time to nCS assertion.
  - nCS deassertion time is controlled by the GPMC.GPMC_CONFIG2_i[12:8] CSRdOffTime field and ensures address hold time to nCS deassertion.
- Address valid signal nADV:
  - nADV assertion time is controlled by the GPMC.GPMC_CONFIG3_i[3:0] ADVOnTime field.
  - nADV deassertion time is controlled by the GPMC.GPMC_CONFIG3_i[12:8] ADVRdOffTime field.
- Output enable signal nOE:
  - nOE assertion indicates a read cycle.
  - nOE assertion time is controlled by the GPMC.GPMC_CONFIG4_i[3:0] OEOnTime field.
  - nOE deassertion time is controlled by the GPMC.GPMC_CONFIG4_i[12:8] OEOffTime field.
- Initial latency for the first read data is controlled by GPMC.GPMC_CONFIG5_i[20:16] RdAccessTime or by monitoring the WAIT signal.
- Successive read data are provided by the memory device each one or two GPMC_CLK cycles. The PageBurstAccessTime parameter must be set accordingly with GpmcFCLKDivider and the memory-device internal configuration.

Depending on the device page length, the GPMC can control device page crossing during a new burst request and purposely insert initial latency.

- Total access time (RdCycleTime) corresponds to RdAccessTime plus the address hold time from nCS deassertion, plus the time from RdAccessTime to CSRdOffTime.
  - RdCycleTime is defined in the GPMC.GPMC_CONFIG5_i register.
- Direction signal DIR:

DIR goes from OUT to IN at the same time as nOE assertion. After a read operation, if no other access (read or write) is pending, the data bus is driven with the previous read value.

- Burst wraparound

The GPMC.GPMC_CONFIG1_i[31] WRAPBURST bit allows a 4-, 8-, or 16-word16 linear burst access to wrap within its burst-length boundary.

6 Reference

- OMAP3515/03 Applications Processor data sheet

  SPRS505F–FEBRUARY 2008–REVISED SEPTEMBER 2009
- OMAP3530/25 Applications Processor data sheet

  SPRS507F–FEBRUARY 2008–REVISED OCTOBER 2009
- OMAP35x Applications Processor Technical Reference Manual

  SPRUF98M–April 2010–Revised December 2010
- S29VS/XS-R MirrorBit Flash Family data sheet

  Publication Number S29VS_XS-R_00 Revision 04 Issue Date March 10, 2009
- S29GL-P MirrorBit Flash Family data sheet

  Publication Number S29GL-P_00 Revision A Amendment 8 Issue Date November 28, 2007
- S29GL-S MirrorBit Eclipse Flash Family data sheet

  Publication Number S29GL_128S_01GS_00 Revision 01 Issue Date February 11, 2011
- S29WS-P MirrorBit Flash Family data sheet

  Publication Number S29WS-P_00 Revision A Amendment 12 Issue Date January 28, 2008

OMAP35x devices integrate the Cortex™-A8 core and TI's C64x+ DSP into four applications processors: OMAP3503, OMAP3515, OMAP3525, and OMAP3530.

Document History Page

Document Title: AN200973 - Interfacing Cypress Flash to TI OMAP Processors Document Number: 002-00973				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	–	–	07/05/2005 to 05/26/2011	Initial version
*A	5005480	MSWI	11/06/2015	Updated in Cypress template
*B	5824692	AESATMP8	07/19/2017	Updated logo and Copyright.
*C	6142191	ZHFE	04/17/2018	Obsolete this document, as TI OMAP processors have been EOLed in 2012 and the design is no longer needed.

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