AN200810 provides a general routing guide for packages (substrate/leadframe) designed with Cypress S25FL-P (32 Mb or 64 Mb) die.

1 Introduction
This document provides a general routing guide for packages (substrate/leadframe) designed with Cypress S25FL-P (32 Mb or 64 Mb) die.

This document does not eliminate the need for customer signal integrity/power delivery simulations. Customers should use Cypress provided IBIS models for timing/crosstalk analysis.

2 Signal Descriptions
The following table describes various pads used in the S25FL-P die.

<table>
<thead>
<tr>
<th>Signal/Supply Pad Name</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SCK</td>
<td>Serial Clock input.</td>
</tr>
<tr>
<td>CS#</td>
<td>Chip Select input.</td>
</tr>
<tr>
<td>SI/IO0</td>
<td>Serial Data Input. Functions as an output pin in Dual and Quad IO mode.</td>
</tr>
<tr>
<td>W#/ACC/IO2</td>
<td>Write Protect. Functions as an output in Quad IO mode.</td>
</tr>
<tr>
<td>SO/IO1</td>
<td>Serial Data Output.</td>
</tr>
<tr>
<td>HOLD#/IO3</td>
<td>Hold input pin. Functions as an output in Quad IO mode.</td>
</tr>
<tr>
<td>VCC</td>
<td>Power supply (2.7-3.6V).</td>
</tr>
<tr>
<td>VSS</td>
<td>Device ground.</td>
</tr>
</tbody>
</table>

3 Signal Groupings
The following table describes various signal/supply groupings to assist in package routing and signal integrity simulations.

<table>
<thead>
<tr>
<th>Signal/Supply Group</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>SI/IO0, SO/IO1, W#/ACC/IO2, HOLD#/IO3</td>
<td>Data I/O</td>
</tr>
<tr>
<td>SCK, CS#</td>
<td>Control signals</td>
</tr>
<tr>
<td>VCC, VSS</td>
<td>Supply</td>
</tr>
</tbody>
</table>

4 Supply Routing Guidelines
Cypress recommends meeting or beating the supply routing recommendations below.

1. Provide a dedicated VCC ball/pin to which the VCC pad is routed to.
2. Provide a dedicated VSS ball/pin to which the VCC pad is routed to.
3. Maintain a low inductance/resistance path from supply pad (VCC, VSS) to solder ball/pin.
4. Keep path inductance for each of the supply nets (from each supply pad to its solder ball/pin) \( \leq 3.0 \text{ nH} \).
5. Keep path resistance from each supply pad to its solder ball ≤ 100 mΩ.
6. Except for necking/bondfinger breakout region, maintain supply (V\text{CC}/V\text{SS}) trace width ≥ 100 µm (wider the better).
7. Route V\text{CC} close to V\text{SS} trace (regardless of the bondwire location) to maintain V\text{CC}-V\text{SS} inductance loop constant. In general a 50 µm separation between V\text{CC}/V\text{SS} supply traces is ideal, whenever possible.
8. Select V\text{CC} and V\text{SS} solder ball location next to each other on the ball map.
9. While doing layer transitions in a BGA substrate, use dual vias as much as possible to reduce via current crowding.

5 Signal Routing Guidelines

Cypress recommends meeting or beating the signal routing recommendations below.

1. Maintain data IO signal routing to within ± 1 nH of each other. Limit DQ routing to ≤ 5 nH.
2. Maintain all DQ routing within +/- 1 nH of SCK.
3. Route control traces (SCK and CS#) ≤ 4 nH.
4. As much as possible, maintain similar via count on all signals within data I/O group.
5. Route flash traces away from other interface high speed signals to avoid crosstalk.
6. Avoid long plating traces for SCK (will cause reflections and impact timing).

6 Multi-Chip Package Routing

If S25FL-P die is used along with other (non-flash) dies in a single MCP, the following routing recommendations should be followed in addition to those in Section 4 and Section 5.

1. Keep flash V\text{CC}/V\text{SS} separate from other die/interface V\text{CC}/V\text{SS} (routing as well as solderball/pin allocations).
2. It may be possible to share V\text{SS} between Cypress flash and PSRAM die (if present) provided PSRAM speed doesn't exceed flash speed. Controller V\text{SS} can only be shared if it pertains to flash interface only. Do not share V\text{SS} between different interfaces (e.g. DDR and flash).
3. Provide V\text{SS} shielding between flash traces/supplies and other interface supply/signal traces (150 µm min. trace width).
4. If signals are shared with another die (e.g. PSRAM) the following general rules should be used:
   - All control signals should be routed in Y configuration. Maintain the overall inductance from pad to ball within guidelines specified in Section 4 and Section 5. However, the fork lengths going to both dies should be electrically matched (provided both dies have similar input capacitance. If they have different input capacitances, IBIS simulations need to be performed to determine fork lengths).
   - All Data I/O topologies need to be simulated to provide adequate topology (daisy chain or Y). However, it is recommended that flash path inductance from signal pad to ball/pin follows guidelines specified in Section 4 and Section 5.
## Document History Page

<table>
<thead>
<tr>
<th></th>
<th>Rev.</th>
<th>ECN No.</th>
<th>Orig. of Change</th>
<th>Submission Date</th>
<th>Description of Change</th>
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<td>MSWI</td>
<td>10/29/2015</td>
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<td>*B</td>
<td>5846477</td>
<td>AESATMP8</td>
<td>08/08/2017</td>
<td>Updated logo and Copyright.</td>
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