AN200291

Migrating from I²C nvSRAM to I²C F-RAM™

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Associated Part Family: I²C F-RAM

Associated Code Examples: None

Related Application Notes: AN96578

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AN200291 provides guidelines for migrating from I²C nvSRAM to I²C F-RAM™. It recommends equivalent F-RAM devices, describes package and feature differences, and discusses the hardware and firmware modifications that need to be made for a successful migration.

Contents

1 Introduction

F-RAM (ferroelectric random access memory) is a nonvolatile memory that uses a ferroelectric capacitor to store data. The data written in F-RAM is nonvolatile instantaneously. Unlike EEPROM and flash, F-RAM writes data to nonvolatile memory at bus speed.

nvSRAM is a SRAM memory with a nonvolatile element embedded in each memory cell. The embedded nonvolatile elements incorporate SONOS Quantum Trap technology. The SRAM provides infinite read and write cycles, while the Quantum Trap cells offer highly reliable nonvolatile storage of data. Data transfers from the SRAM to the nonvolatile elements (STORE operation) take place automatically at power down. On power up, data is restored to the SRAM from the nonvolatile memory (RECALL operation).

Cypress has made three nvSRAM devices that are not recommended for new design (NRND): CY14MB064J2A, CY14ME064J2A, and CY14B101J2. Cypress provides replacement options for these devices through its F-RAM products. This application note provides details on migrating from I²C nvSRAM to I²C F-RAM. It discusses the differences in package, features, and timing, and the modifications required in hardware and firmware to make the migration successful.

For the nvSRAM devices that are NRND, Table 1 lists the suggested F-RAM replacement parts.

Table 1. Migration Options

SI No.	nvSRAM (or Original) Part Number	F-RAM (or Replacement) Part Number	Description
1	CY14MB064J2A	FM24CL64B	64-Kb, 3.0-V I^2C Device
2	CY14ME064J2A	FM24C64B	64-Kb, 5.0-V I^2C Device
3	CY14B101J2	FM24V10 / FM24VN10	1-Mb, 3.0-V I^2C Device

These suggested F-RAM parts are similar to the nvSRAM parts in read/write protocol (I^2C) and density, but they are not identical. You need to be aware of the differences when replacing the nvSRAM parts. The following sections discuss the similarities and differences.

2 Overview

2.1 Package Compatibility

All nvSRAM package options are supported in F-RAM, as shown in Table 2. In addition, the 3.0-V, 64-Kb F-RAM device is also offered in an 8-pin DFN package.

Table 2. Package Comparison

Package	Migration Options					
	1		2		3	
	CY14MB064J2A	FM24CL64B	CY14ME064J2A	FM24C64B	CY14B101J2	FM24V10/ FM24VN10
8-pin SOIC	Available	Available	Available	Available	Available	Available
8-pin DFN	Not Available	Available	Not Available	Not Available	Not Available	Not Available

2.2 Pin Compatibility

Between nvSRAM and F-RAM, all the I/O pins except pin 1 match, as described in Table 3. Pin 1 is device select pin A0 in F-RAM. Since A0 has an internal pull-down in F-RAM, it can be left floating when migrating to F-RAM.

Table 3. Pin Differences

SI No.	Part Numbers	Pin Description
1	CY14MB064J2A versus FM24CL64B	All the pins are compatible except pin 1. Pin 1 is V_{CAP} in CY14MB064J2A, while it is A0 in FM24CL64B. Since FM24CL64B does not need the V_{CAP} pin, it provides an extra device select pin, A0, through which a maximum of eight F-RAM devices can be hooked into the same I^2C bus. Using the A0 pin will require a firmware change in existing applications. Bit 1 in the memory slave ID was “don’t care” in nvSRAM, but it should be 0 in F-RAM (assuming the A0 pin will be left unconnected or connected to VSS in F-RAM).
2	CY14ME064J2A versus FM24C64B	All the pins are compatible except pin 1. Pin 1 is V_{CAP} in CY14ME064J2A, while it is A0 in FM24C64B. Since FM24C64B does not need the V_{CAP} pin, it provides an extra device select pin, A0, through which a maximum of eight F-RAM devices can be hooked onto the same I^2C bus. Using the A0 pin will require a firmware change in existing applications. Bit 1 in the memory slave ID was “don’t care” in nvSRAM, but it should be 0 in F-RAM (assuming the A0 pin will be left unconnected or connected to VSS in F-RAM).
3	CY14B101J2 versus FM24V10 / FM24VN10	All the pins are compatible. Since F-RAM does not require V_{CAP}, pin 1 is NC (no connect).

2.3 Instruction/Feature Set

Table 4 compares all the features of nvSRAM with F-RAM. The highlighted cells show that the feature is inferior in F-RAM compared to nvSRAM.

Table 4. Feature Set Comparison

Feature Set	Migration Options						Comments
	1		2		3		
	CY14MB064J2A	FM24CL64B	CY14ME064J2A	FM24C64B	CY14B101J2	FM24V10/ FM24VN10	
Single-Byte Write	Available	Available	Available	Available	Available	Available	
Multi-Byte Write	Available	Available	Available	Available	Available	Available	
Hs-mode Single-Byte Write	Available	Not Available	Available	Not Available	Available	Available	I^2C Hs-mode is not supported in 64-Kb F-RAM.
Hs-mode Multi-Byte Write	Available	Not Available	Available	Not Available	Available	Available	I^2C Hs-mode is not supported in 64-Kb F-RAM.
Current Address Single-Byte Read	Available	Available	Available	Available	Available	Available	
Current Address Multi-Byte Read	Available	Available	Available	Available	Available	Available	
Hs-mode Current Address Single-Byte Read	Available	Not Available	Available	Not Available	Available	Available	I^2C Hs-mode is not supported in 64-Kb F-RAM.
Hs-mode Current Address Multi-Byte Read	Available	Not Available	Available	Not Available	Available	Available	I^2C Hs-mode is not supported in 64-Kb F-RAM.
Selective (Random) Single-Byte Read	Available	Available	Available	Available	Available	Available	
Selective (Random) Multi-Byte Read	Available	Available	Available	Available	Available	Available	
Sleep Mode	Available	Not Available	Available	Not Available	Available	Available	64-Kb F-RAM consumes very low standby current; hence, sleep mode is not supported.
Device ID	Available	Not Available	Available	Not Available	Available	Available	Device ID is not supported in 64-Kb F-RAM.
Serial Number	Available	Not Available	Available	Not Available	Available	Available in FM24VN10	Serial number is not supported in 64-Kb F-RAM.
AutoStore	Available	–	Available	–	Available	–	AutoStore is not applicable to F-RAM, since nonvolatile write is instantaneous.
Software STORE	Available	–	Available	–	Available	–	Software STORE is not applicable to F-RAM, since nonvolatile write is instantaneous.

Feature Set	Migration Options						Comments
	1		2		3		
	CY14MB064J2A	FM24CL64B	CY14ME064J2A	FM24C64B	CY14B101J2	FM24V10/ FM24VN10	
AutoStore Enable and Disable	Available	–	Available	–	Available	–	AutoStore is not applicable to F-RAM.
Software RECALL	Available	–	Available	–	Available	–	Software RECALL is not applicable to F-RAM, since there are no separate NV memory cells.
Status Register/ Block Protect	Available	Not Available	Available	Not Available	Available	Not Available	Status register or block protect is not available in F-RAM.
Speed	3.4 MHz, 1 MHz, 400 kHz	1 MHz, 400 kHz	3.4 MHz, 1 MHz, 400 kHz	1 MHz, 400 kHz	3.4 MHz, 1 MHz, 400 kHz	3.4 MHz, 1 MHz, 400 kHz	High-speed mode is not supported in 64-Kb F-RAM.
Endurance	10^6 Nonvolatile Cycles	10^{14}	10^6 Nonvolatile Cycles	10^{14}	10^6 Nonvolatile Cycles	10^{14}	Endurance is virtually unlimited for all practical purposes for both nvSRAM and F-RAM.
Data Retention (at 85 °C)	20 Years	10 Years	20 Years	10 Years	20 Years	10 Years	F-RAM data retention is lower than that of nvSRAM.

2.4 Parameters

Table 5 provides the DC and AC parameter comparisons between 64-Kb nvSRAM and F-RAM. Except for high-speed mode, the parameters are compatible. The highlighted cells show that the feature is inferior in F-RAM compared to nvSRAM.

Table 5. Parameter Comparison of 64-Kb nvSRAM and F-RAM

Parameter	Description		CY14MB064J2A/ CY14ME064J2A		FM24CL64B / FM24C64B		Unit
			Min	Max	Min	Max	
DC Parameters							
V_{CC}/V_{DD}	Power supply	3 V Typical	2.7	3.6	2.7	3.65	V
		5 V Typical	4.5	5.5	4.5	5.5	
I_{CC1}	Average V_{cc} current	f_{SCL} = 3.4 MHz	–	1	Not Supported		mA
		f_{SCL} = 1 MHz	–	400	–	300 (FM24CL64B)	µA
						400 (FM24C64B)	
I_{CC2}	Average V_{cc} current during STORE		–	3	N/A		mA
I_{CC4}	Average V_{VCAP} current during AutoStore cycle		–	3	N/A		mA
I_{SB}	V_{cc} standby current		–	120 (CY14MB064J2A)	-	6 (FM24CL64B)	µA

Parameter	Description		CY14MB064J2A/ CY14ME064J2A		FM24CL64B / FM24C64B		Unit
			Min	Max	Min	Max	
				150 (CY14ME064J2A)		10 (FM24C64B)	
I_{ZZ}	Sleep mode current		–	8	Not Supported		µA
I_{IX}	Input current on I/O pin		–1	+1	–1	+1	µA
I_{OZ}	Output leakage current		–1	+1	–1	+1	µA
Ci / C_O	Output pin capacitance		–	7	–	8	pF
Ci / C_I	Input pin capacitance		–	7	–	6	pF
V_{IH}	Input HIGH voltage		0.7 x V_{CC}	V_{CC} + 0.5	0.7 x V_{CC}	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage		–0.5	0.3 x V_{CC}	–0.3	0.3 x V_{CC}	V
V_{OL}	Output LOW voltage	I_{OL} = 3 mA	–	0.4	–	0.4	V
		I_{OL} = 6 mA	–	0.6	Not Supported		V
Rin	V_{IN} = $V_{IL(Max)}$		50	–	40	–	kΩ
	V_{IN} = $V_{IH(Min)}$		1	–	1	–	MΩ
Vhys	Hysteresis of Schmitt trigger inputs		0.05 x V_{CC}	–	0.05 x V_{CC}	–	V
V_{CAP}	Storage capacitor		42	180	N/A		µF
V_{VCAP}	Maximum voltage driven on V_{CAP} pin by the device		–	V_{CC}	N/A		V
Clock Frequency							
f_{SCL}	Clock frequency, SCL		–	3.4	Not Supported		MHz
			–	1	–	1	MHz
			–	400	–	400	kHz
AC Switching Parameters at f_{SCL} = 1 MHz							
$t_{SU; STA}$	Setup time for repeated START condition		250	–	250	–	ns
$t_{HD;STA}$	Hold time for START condition		250	–	250	–	ns
t_{LOW}	LOW period of the SCL		500	–	600	–	ns
t_{HIGH}	HIGH period of the SCL		260	–	400	–	ns
$t_{SU;DATA}$	Data in setup time		100	–	100	–	ns
$t_{HD;DATA}$	Data hold time (in/out)		0	–	0	–	ns
t_{DH}	Data out hold time		0	–	0	–	ns
t_r	Rise time of SDA and SCL		–	120	–	300	ns
t_f	Fall time of SDA and SCL		–	120	–	100	ns
$t_{SU;STO}$	Setup time for STOP condition		250	–	250	–	ns
$t_{VD;DATA}$	Data output valid time		–	400	–	550	ns
$t_{VD;ACK}$	ACK output valid time		–	400	Not Specified		ns
t_{OF}	Output fall time from $V_{IH(min)}$ to $V_{IL(max)}$		–	120	Not Specified		ns

Parameter	Description	CY14MB064J2A/ CY14ME064J2A		FM24CL64B / FM24C64B		Unit
		Min	Max	Min	Max	
t_{BUF}	Bus free time between STOP and next START condition	500	–	500	–	ns
t_{SP}	Pulse width of spikes that must be suppressed by input filter	–	50	–	50	ns
Timing						
t_{FA} (t_{PU})	Power up to first access	20	–	1 (FM24CL64B) 10 (FM24C64B)	–	ms
$t_{VCCRISE}$ (t_{VR})	V_{CC} power-up ramp rate	50	–	30	–	µs/V
t_{VF}	V_{CC} power-down ramp rate	Not Specified		30	–	µs/V
t_{SLEEP}	Time to enter low-power mode after issuing SLEEP instruction	–	8	Not Applicable		ms
t_{WAKE} (t_{REC})	Time for wakeup from sleep mode	–	20	Not Applicable		ms
t_{SB}	Time to enter standby mode after issuing STOP condition	–	100	Not Specified		µs

Table 6 provides the DC and AC parameter comparisons between 1-Mb nvSRAM and F-RAM. All the parameters are compatible. The highlighted cells show that the feature is inferior in F-RAM compared to nvSRAM.

Table 6. Parameter Comparison of 1-Mb nvSRAM and F-RAM

Parameter	Description		CY14B101J2		FM24V10 / FM24VN10		Unit
			Min	Max	Min	Max	
DC Parameters							
V_{CC}/V_{DD}	Power supply		2.7	3.6	2.0	3.6	V
I_{CC1}	Average V_{cc} current	f_{SCL} = 3.4 MHz	–	1	1		mA
		f_{SCL} = 1 MHz	–	400	–	400	µA
I_{CC2}	Average V_{cc} current during STORE		–	3	Not Applicable		mA
I_{CC4}	Average V_{VCAP} current during AutoStore cycle		–	3	Not Applicable		mA
I_{SB}	V_{cc} standby current		–	150	–	150	µA
I_{ZZ}	Sleep mode current		–	8	–	8	µA
I_{IX}	Input current on I/O pin		–1	+1	–1	+1	µA
I_{OZ}	Output leakage current		–1	+1	–1	+1	µA
Ci	Capacitance for each I/O pin		–	7	–	–	pF
C_O	Output pin capacitance (SDA)		–	–	–	8	pF
C_I	Input pin capacitance		–	–	–	6	pF
V_{IH}	Input HIGH voltage		0.7 x V_{CC}	V_{CC} + 0.5	0.7 x V_{CC}	V_{CC} + 0.3	V
V_{IL}	Input LOW voltage		–0.5	0.3 x V_{CC}	–0.3	0.3 x V_{CC}	V
V_{OL}	Output LOW	I_{OL} = 3 mA	–	0.4	–	0.4	V

Parameter	Description		CY14B101J2		FM24V10 / FM24VN10		Unit
			Min	Max	Min	Max	
	voltage	I_{OL} = 6 mA	–	0.6	Not Specified		V
Rin	$V_{IN} = V_{IL(Max)}$		50	–	50	–	kΩ
	$V_{IN} = V_{IH(Min)}$		1	–	1	–	MΩ
Vhys	Hysteresis of Schmitt trigger inputs		0.05 x V_{CC}	–	0.05 x V_{CC}	–	V
V_{CAP}	Storage capacitor		42	180	Not Applicable		µF
V_{VCAP}	Maximum voltage driven on V_{CAP} pin by the device		–	V_{CC}	Not Applicable		V
Clock Frequency							
f_{SCL}	Clock frequency, SCL		–	3.4	–	3.4	MHz
			–	1	–	1	MHz
			–	400	–	400	kHz
AC Switching Parameters at f_{SCL} = 1 MHz							
$t_{SU;STA}$	Setup time for repeated START condition		250	–	260	–	ns
$t_{HD;STA}$	Hold time for START condition		250	–	260	–	ns
t_{LOW}	LOW period of the SCL		500	–	500	–	ns
t_{HIGH}	HIGH period of the SCL		260	–	260	–	ns
$t_{SU;DATA}$	Data in setup time		100	–	50	–	ns
$t_{HD;DATA}$	Data hold time (in/out)		0	–	0	–	ns
t_{DH}	Data out hold time		0	–	0	–	ns
t_r	Rise time of SDA and SCL		–	120	–	120	ns
t_f	Fall time of SDA and SCL		–	120	–	120	ns
$t_{SU;STO}$	Setup time for STOP condition		250	–	260	–	ns
$t_{VD;DATA}$	Data output valid time		–	400	–	450	ns
$t_{VD;ACK}$	ACK output valid time		–	400	Not Specified		ns
t_{OF}	Output fall time from $V_{IH(min)}$ to $V_{IL(max)}$		–	120	Not Specified		ns
t_{BUF}	Bus free time between STOP and next START condition		500	–	500	–	ns
t_{SP}	Pulse width of spikes that must be suppressed by input filter		–	50	–	50	ns
Timing							
t_{FA} (t_{PU})	Power up to first access		20	–	0.25	–	ms
$t_{VCCRISE}$ (t_{VR})	V_{CC} power-up ramp rate		50	–	50	–	µs/V
t_{VF}	V_{CC} power-down ramp rate		No Restriction		100	–	µs/V
t_{SLEEP}	Time to enter low-power mode after issuing SLEEP instruction		–	8	Not Specified		ms
t_{WAKE} (t_{REC})	Time for wakeup from sleep mode		–	20	–	0.4	ms

Parameter	Description	CY14B101J2		FM24V10 / FM24VN10		Unit
		Min	Max	Min	Max	
t_{SB}	Time to enter standby mode after issuing STOP condition	–	100	Not Specified		µs

3 Critical Considerations

Table 7 summarizes the critical considerations for each option that need to be accommodated when migrating from nvSRAM to F-RAM.

Table 7. Summary of Critical Considerations

Sl No.	Part Numbers	Key Differences
1	CY14MB064J2A versus FM24CL64B	**Pin:** Pin 1 is V_{CAP} in nvSRAM and A0 in F-RAM. **Speed:** 3.4 MHz is not supported in F-RAM. F-RAM supports 1 MHz, 400 kHz, and 100 kHz. **Features not required:** AutoStore, software STORE, software RECALL, AutoStore Enable, and AutoStore Disable are not applicable to F-RAM. **Features not supported:** Sleep mode, device ID, serial number, block protect, and status register are not supported in F-RAM.
2	CY14ME064J2A versus FM24C64B	**Pin**: Pin 1 is V_{CAP} in nvSRAM and A0 in F-RAM. **Speed:** 3.4 MHz is not supported in F-RAM. F-RAM supports 1 MHz, 400 kHz, and 100 kHz. **Features not required:** AutoStore, software STORE, software RECALL, AutoStore Enable, and Autostore Disable are not applicable to F-RAM. **Features not supported:** Sleep mode, device ID, serial number, block protect, and status register are not supported in F-RAM.
3	CY14B101J2 versus FM24V10/ FM24VN10	**Pin**: Pin 1 is V_{CAP} in nvSRAM and A0 in F-RAM. **Features not required:** AutoStore, software STORE, software RECALL, AutoStore Enable, and AutoStore Disable are not applicable to F-RAM. **Features not supported:** Block protect and status register are not supported in F-RAM. **Features with different implementation:** Sleep mode, Device ID and serial number are supported, but instructions are different between nvSRAM and F-RAM.

3.1 Pin Difference

Pin 1 in nvSRAM is V_{CAP}. In 64-Kb F-RAM, it is A0 and in 1-Mb F-RAM, it is NC, as shown in Figure 1 and Figure 2. Hence when migrating from nvSRAM to F-RAM, leave pin 1 floating. F-RAM has an internal pull-down to keep pin A0 LOW.

Figure 1. Package Comparison of 64-Kb nvSRAM and F-RAM

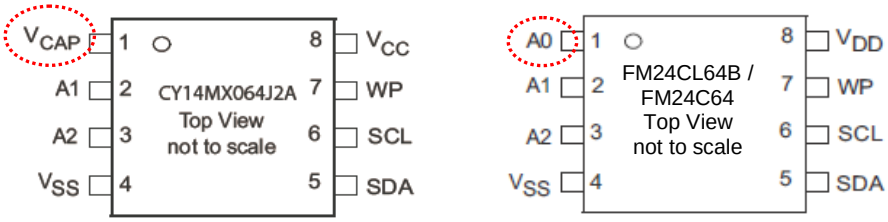
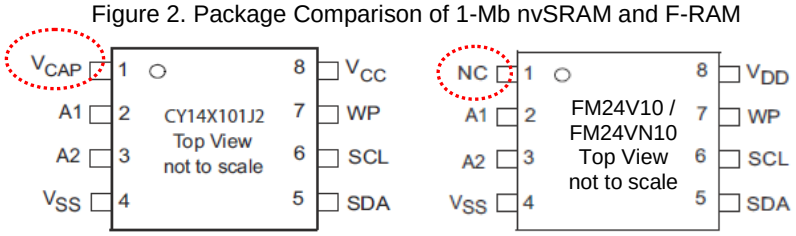


Figure 2. Package Comparison of 1-Mb nvSRAM and F-RAM



3.2 I²C Speed

I²C Hs-mode is supported only in higher density (128 Kb or higher) F-RAM. Therefore, I²C speed is not an issue when migrating from 1-Mb nvSRAM to 1-Mb F-RAM.

I²C speed is also not an issue when migrating from 64-Kb nvSRAM (CY14MB064J2A) to 64-Kb F-RAM (FM24CL64B) for a 1-MHz or lower I²C access. However, if Hs-mode access is a necessity, then CY14MB064J2A can migrate to a higher density F-RAM (128 Kb, FM24V01) that supports Hs-mode in the same footprint. CY14ME064J2A (5-V nvSRAM) has no replacement for Hs-mode in F-RAM.

3.3 nvSRAM Special Features

The nvSRAM special features such as AutoStore, AutoStore Enable, AutoStore Disable, software STORE, and software RECALL are not applicable to F-RAM. In nvSRAM, data is first written to SRAM and then transferred to nonvolatile cells during AutoStore or software STORE. In F-RAM, data is nonvolatile instantaneously; hence, these features are not relevant.

3.4 Sleep Mode

On lower density F-RAM devices (FM24CL64B and FM24C64B), the standby current is equivalent to the sleep mode currents of the nvSRAM. Hence, sleep mode is not required in low-density F-RAM. In the 1-Mb F-RAM FM24V10/FM24VN10, sleep mode is supported similar to the nvSRAM CY14B101J2. However, the sleep mode entry instructions are different, as shown in Figure 3 and Figure 4.

Figure 3. Sleep Mode in nvSRAM (CY14B101J2)

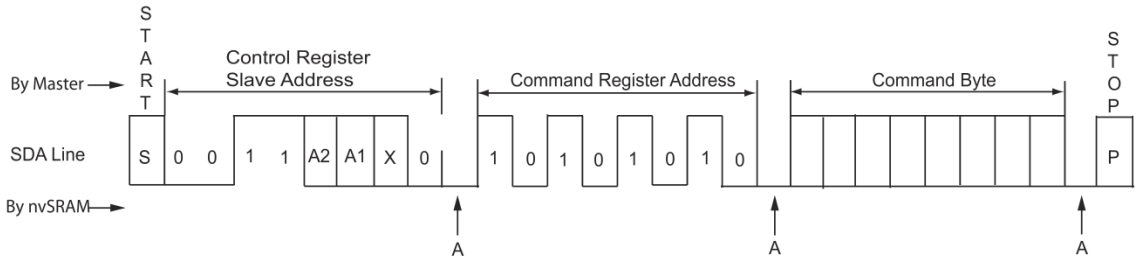
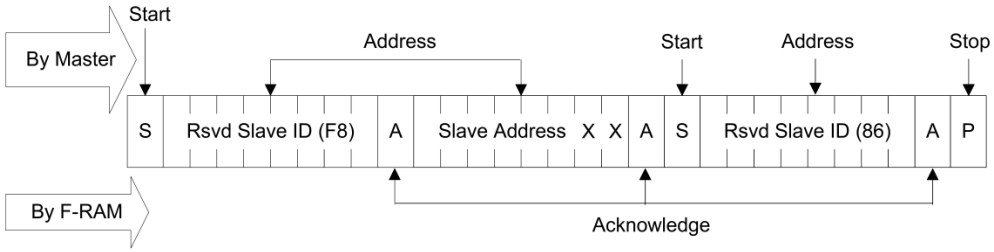


Figure 4. Sleep Mode in F-RAM (FM24V10)



3.5 Device ID

Unlike nvSRAM, a device ID is not available in all F-RAM devices. FM24V10/FM24VN10 has a device ID similar to that in the nvSRAM counterpart, CY14B101J2. However, the instructions to read the device ID are different, as shown in Figure 5 and Figure 6. On lower density F-RAM devices (FM24CL64B and FM24C64B), a device ID is not available. However, FM24CL64B can migrate to a higher density F-RAM (128-Kb FM24V01) if a device ID is a necessity.

Figure 5. Device ID Read in nvSRAM (CY14B101J2)

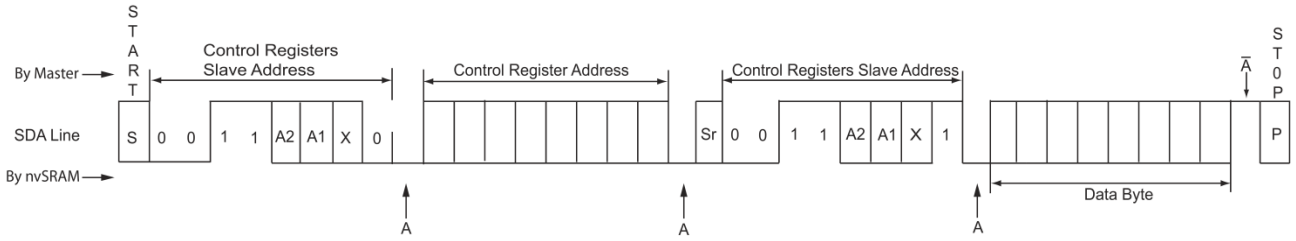
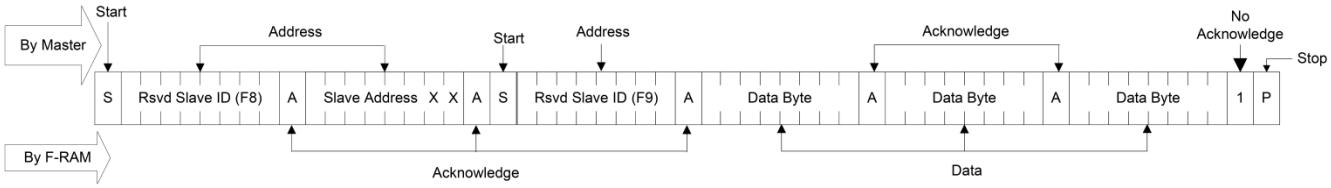


Figure 6. Device ID Read in F-RAM (FM24V10)



3.6 Serial Number

Unlike nvSRAM, a serial number is available only in the 1-Mb F-RAM device. While the standard 1-Mb FM24V10 does not have a serial number, another F-RAM part, FM24VN10, has a serial number. The serial number in nvSRAM is user configurable, but in F-RAM, it is a factory-programmed read-only number. Also, the instructions to read the serial number are different between the two, as shown in Figure 7 and Figure 8. On lower density F-RAM devices (FM24CL64B and FM24C64B), a serial number is not available.

Figure 7. Serial Number Read in nvSRAM (CY14B101J2)

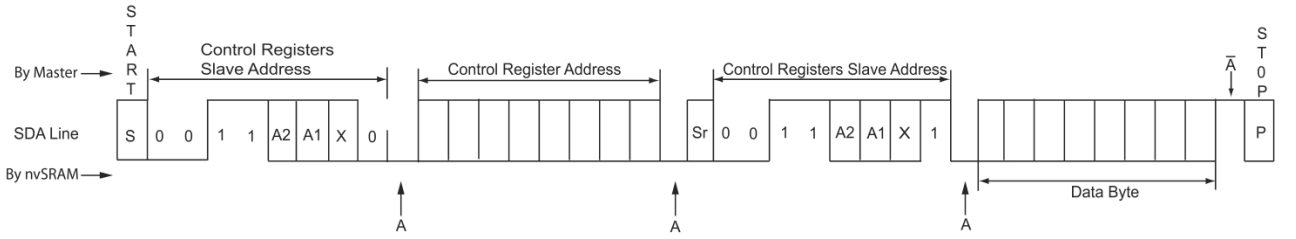
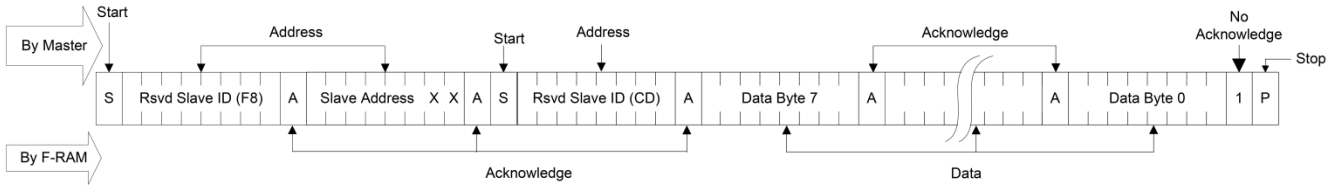


Figure 8. Serial Number Read in F-RAM (FM24VN10)



3.7 Status Register and Block Protect

Unlike nvSRAM, F-RAM does not have a status register. Hence, the block protect feature is also not supported. If you are using the block protect feature in nvSRAM, it is not available when migrating to F-RAM. However, the Write Protect (WP) pin functionality, which protects the entire memory, is the same for both nvSRAM and F-RAM.

3.8 Timing Parameters

The AC parameters, tLOW and tHIGH, represent the SCL clock LOW and HIGH timing. They are the same for 1-Mb CY14B101J2 and FM24V10. For 64-Kb nvSRAM and F-RAM, they are the same except at 1 MHz. If your application is running at 1 MHz, ensure that tLOW is minimum, 600 ns, and tHIGH is minimum, 400 ns, when migrating to F-RAM.

The fall time of the SDA and SCL line, t_f, is 120 ns (max) for 64-Kb nvSRAM, while is it 100 ns (max) for 64-Kb F-RAM.

The setup timing for repeat START ($t_{SU;STA}$) and STOP ($t_{SU;STO}$) and hold timing ($t_{HD;STA}$) for START is slightly different. It is 260 ns for 1-Mb FM24V10 and 250 ns for CY14B101J2.

The rest of the F-RAM specifications are either better than or the same as those of nvSRAM. Refer to Table 5 and Table 6 for a comparison.

3.9 V_{cc} Ramp Rate

F-RAM has the same or a better V_{cc} power-up ramp rate specification than the nvSRAM. However, the power-down ramp rate specification is added in F-RAM. Ensure that the power-down ramp rates are slower than 30 µs/V in your system.

3.10 Firmware Changes

The firmware for nvSRAM may contain extra logic due to nvSRAM-specific features such as AutoStore, software STORE, software RECALL, AutoStore Enable, and AutoStore Disable. This logic can be removed for F-RAM. The sleep mode, device ID, and serial number instructions are different in F-RAM; hence, the firmware needs to be modified.

The power up to first access time, sleep mode entry time, and wakeup time are less in F-RAM. Hence, the firmware can be updated to reduce the wait time. Refer to Table 5 and Table 6 for more details.

4 Summary

This application note discussed the options for migrating from I^2C nvSRAM to I^2C F-RAM devices. There are a few differences between them that need to be considered in terms of package, features, and parameters. The majority of designs that use the specified nvSRAM devices can migrate to F-RAM with minimal changes.

Document History

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**	5009385	MEDU	11/10/2015	New application note.
*A	5857687	HARA	08/18/2017	Updated logo and copyright.

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