AN15979

Soft Errors in nvSRAM

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Associated Part Family: nvSRAM
Related Application Notes: None

AN15979 describes the causes of soft error in memories and how the nvSRAM architecture, features, and packaging techniques act to reduce these soft errors.

1 Introduction

The Soft Error Rate (SER) of advanced CMOS devices is higher than all other reliability mechanisms combined together. So it becomes necessary for the high-speed memory architectures to counter the effect of soft errors. The Cypress nvSRAM with its unique architecture and special features such as Software STORE and Software RECALL can correct soft errors on the fly. This capability combined with Cypress's intense SER test methodology makes nvSRAM one of the most reliable memory devices against the soft errors.

2 Soft Errors and their Causes

The Soft Errors (caused by radiations) refer to random, non-recurring change of state or transient in microelectronic circuits due to energetic nuclear particles interacting with the silicon. No physical defect is associated with the failing circuit and the device's normal operation is restored by a simple reset/rewrite operation as opposed to hard fails, which cause permanent damage to the device. Soft error rate determines the probability of the device failure caused by radiations.

The causes of Soft Errors are:

Alpha particles – They are produced due to the radioactive decay of elements, such as Th-232, U-238, Po-210, and so on. They also exist in packaging materials such as mold compounds, bumps, and so on. In Silicon, an alpha particle hit deposits a dense track of charge (e-h pairs) and has a range that depends on its energy (usually 2 MeV to 9 MeV).

High energy neutrons from cosmic rays – The origin of these cosmic rays striking the earth's atmosphere is either the sun (energies upto 1 GeV) or isotropic galactic particles (energies > 108 GeV). The flux of these particles depends on the altitude and the geographical location. These high energy neutrons create a burst of energy in the semiconductor substrate and form the most dominant soft error source.

Thermal neutrons – Thermal neutrons react with the boron isotope 10B in BPSG and produces two high energy particles (Li7 (0.84 MeV) and He4 (1.47 MeV)) that cause soft errors.

3 Failure Mechanisms in nvSRAM

The nvSRAM is basically a SRAM with a nonvolatile element embedded in every SRAM cell, which makes the nvSRAM a nonvolatile memory. During normal operation, only the SRAM portion of the nvSRAM is exposed to the read/write operation therefore, the radiations explained in soft errors and their causes can cause soft errors in the SRAM portion of the nvSRAM cell. The nonvolatile portion of the nvSRAM is not affected due to soft errors. The impact of soft errors in SRAM portion of nvSRAM cell is illustrated in Figure 1 and Figure 2.

Figure 1. SRAM Portion of nvSRAM

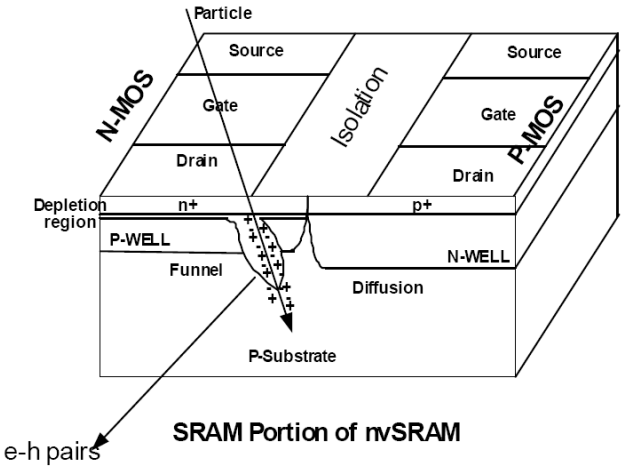
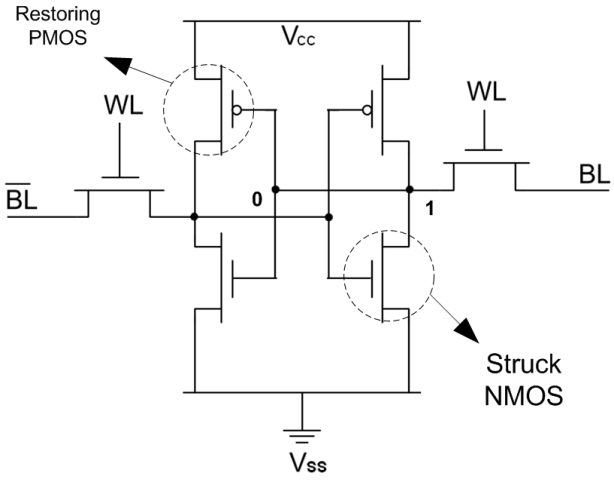


Figure 2. SRAM Cell in the nvSRAM



As shown in the reference, an incident particle generates an electron hole pairs directly (alpha-particle) or indirectly (high energy neutron causing burst of charge) in the SRAM portion of the nvSRAM and the following occurs: The electric field in the depletion region causes the charge to be collected by the junction, resulting in the current disturb of the struck MOS (NMOS). The restoring MOS (PMOS) tries to balance it but its finite current drive and the channel conductance induces a voltage disturb in its drain. If this transient voltage pulse overcomes the threshold charge of the cell, the stored data flips.

4 nvSRAM Failure Modes

The failure mechanisms explained above can result in the SRAM portion of the nvSRAM. The following failure modes can take place due to soft errors in nvSRAM:

4.1 Single Event Upset (SEU)

This type of radiation induced upset is identified when a flipped bit is physically isolated from other possible events and the physical separation from any other flipped bit is at least two memory cells. For Alpha particles, typically 99% of the upsets are single-bit. For Neutrons, typically 84% of the upsets are single-bit (and is decreasing with technology scaling).

4.2 Multi Bit Upset (MBU)

This type of radiation induced upset is identified when two or more flipped bits are physically adjacent or have a separation of at most one-failing bit. For alpha particles, typically 1% of the upsets are multi-bit. For neutrons, up to 16% of the upsets can be multi-bit (and is increasing with technology scaling).

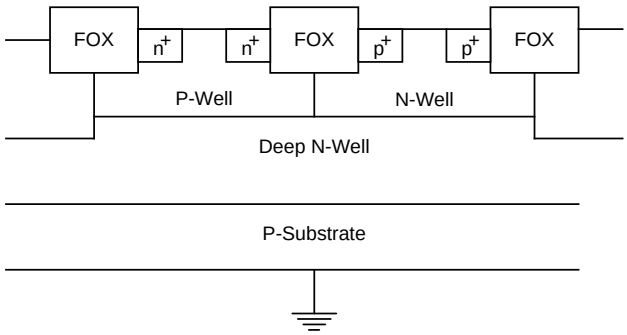
4.3 Single Event Latch-up (SEL)

This type of upset is potentially destructive condition involving parasitic circuit elements forming a silicon controlled rectifier (SCR). Normally this SCR is off and only conducting leakage current. However, if enough voltage (called a threshold voltage) is put across the SCR by some parasitic event, the SCR turns on and conducts current. This current remains until the SCR is completely powered off, which is why this condition is called latch-up. In traditional SEL, the SCR device current may destroy the device if not current limited and removed in time. A removal of power to the device is required in all non-catastrophic SEL conditions in order to recover device operations. Several mitigation options used for standard latch-up issues can also be applied for SEL issues.

4.4 SEL Solution in nvSRAM Application

The nvSRAM is well protected from SEL events by employing a triple well architecture underneath the memory core, which creates a low resistive V_{CC} collection layer for electrons, making it virtually impossible to accumulate enough isolated charge to create a voltage even approaching the threshold voltage required for latch-up.

Figure 3. Triple Well Architecture



Cypress has performed both alpha and neutron testing (the main cause of parasitic events in silicon) on our nvSRAM's to measure SEL. All tested samples of nvSRAM on S8 technology node successfully demonstrated Zero SEL events under extreme testing conditions.

5 Process Mitigation Techniques Used in nvSRAM

5.1 Alpha Particles

The semiconductor industry has focused very strongly in using low alpha mold compounds in packaging to reduce alpha particle related failures. The flux rate currently applied for nvSRAM is in the order of 0.001 to 0.002 alpha/cm^2/hr, which is at the lower end of the detection limit for the mold compound material. In addition thorough packaging supplier screening has ensured that low alpha emitting materials are employed.

5.2 Thermal Neutrons

The Borophosphosilicate glass (BPSG) layer, which causes the interaction with the thermal Neutrons, has been completely eliminated from Cypress Semiconductor process flows starting with the 0.16 µm technology node. The nvSRAM does not contain any BPSG, hence, there is no risk for thermal neutron related upsets.

6 System Level Solution against Soft Errors

The Cypress nvSRAM cell is unique and different from a normal SRAM cell, because it integrates the SRAM and NV memory cell together. The nvSRAM memory is architected in such a way that it is virtually impossible to get an MBU, as the bits are spread apart farther than area caused by the damage from the particle. Therefore, the nvSRAM is capable of producing only single bit upsets. No evidence of multi bit upset (MBU) has been recorded in the nvSRAM in all SER testing.

nvSRAM's are high performance nonvolatile memories designed to interface easily with embedded controllers with write and read access time as fast as 20 ns. Cypress's nvSRAM's can be accessed like any other standard SRAMs and can be integrated to any standard processor very easily. The transfer of data from the volatile SRAM memory to the nonvolatile element is done very quickly and automatically when power fails. This data can be retained for as long as 20 years without the use of a battery.

The STORE operation in nvSRAM's can be initiated by any of the following three methods:

- AutoStore™ on power down
- Software STORE
- Hardware STORE

Similarly, the RECALL operation from non volatile cells to SRAM cells can be initiated by any of the following two methods:

- AutoRecall™ on power up
- Software RECALL

The special features of nvSRAM such as Software STORE and RECALL can be utilized effectively at the system level to counter the effect of SER. Software STORE and RECALL are initiated by the controller by sending specific soft sequences as specified in the device datasheet. For example, in a 4 Mb nvSRAM, the Software STORE and RECALL are initiated by performing consecutive reads from the six specified memory address locations as below:

- Read Address 0x4E38 – Valid READ
- Read Address 0xB1C7 – Valid READ
- Read Address 0x83E0 – Valid READ
- Read Address 0x7C1F – Valid READ
- Read Address 0x703F – Valid READ
- Read Address 0x8FC0 – Valid READ; to initiate STORE Cycle

Or

- Read Address 0x4C63 – Valid READ; to initiate RECALL Cycle.

The Software STORE takes 8 ms and Software RECALL takes about 200 µs to complete.

The following schemes can be implemented in the system/controller in any application for the nvSRAM to counter the soft errors.

6.1 Software STORE after Every Critical Write

The controller accessing the nvSRAM can be programmed to perform a Software STORE every time it writes a critical data on to the nvSRAM. This ensures that the data is stored safely in the Quantum Trap, which is isolated from the SRAM portion of the nvSRAM during the power-on condition. This is equal to making a copy of the important data and keeping it in a safe place. In case of data corruption during power-on condition, the saved data can be retrieved by the controller performing a Software RECALL. However it should be noted that the number of writes to Quantum Trap is limited to 1,000,000 cycles and therefore the Software STORE should follow only the critical writes.

6.2 Parity Correction with Software RECALL (Against SEUs)

A parity bit can be added to the data that is stored on to the nvSRAM. Parity check can be performed by the controller interfacing with the nvSRAM during every write or read operation. If the error is detected, a Software RECALL can be performed to restore the correct data (Remember that every critical write should follow a software STORE to secure data in NV cell so that data can be recalled whenever data corruption happens due to soft error). This acts as an error correction scheme against single bit upsets.

6.3 Error Detecting Algorithms with a Software RECALL

Error detecting bits can be appended to the words stored in the nvSRAM with the detecting algorithm implemented in the controller interfacing to it. If an error is detected, a Software RECALL can be initiated to restore the correct value (under the assumption that a Software STORE has followed a critical write). This acts as an error correction scheme against MBUs. The number of recalls from the nonvolatile elements to the SRAM in the nvSRAM is infinite but the number of write cycles to the nonvolatile element is limited to one million in the Cypress devices. So the nonvolatile write in these schemes should be initiated only after the critical write to avoid unnecessary write to non volatile cells.

7 Cypress SER Test Methodologies

Cypress understands the importance and the criticality of SER in memory devices and the affect it can have on the customer's applications. It has the required infrastructure to carry out both the life testing methods and the accelerated testing methods for SER in memory devices.

In life testing methods, large memory banks are built and natural SER is tested without acceleration. This is a time consuming and expensive method that can span over months. This can also be used to confirm the results of accelerated testing methods.

Accelerated testing methods include exposing the chip to various types of radiation such as alpha test, neutron/proton test, system SER, and thermal neutron test to measure the SER value. The accelerated testing can be carried out at Cypress facility on request. Cypress has done accelerated testing on demand for Department of Defense (DoD) and Navy experiments.

8 Summary

Soft errors are inevitable in memory devices. The nvSRAM acts against these soft errors in every aspect with its architecture, packaging, and special features such as Software STORE/RECALL. These protection techniques along with Cypress's intense SER test methodologies and its leading SER capabilities make nvSRAM more reliable device in the customer's application than its competitors.

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10 Document History

Document Title: AN15979 - Soft Errors in nvSRAM

Document Number: 001-15979

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1210788	UHA	07/03/2007	New application note.
*A	3053056	ZSK	10/08/2010	Added SCR effect in Single Event Latch-up (SEL) description System Added a paragraph in “Level Solution against Soft Errors” describing nvSRAM is free from MBU. Software STORE time duration changed from 15 ms to 8 ms Software STORE time duration changed from 100 µs to 200 µs Non volatile endurance cycle changed from 200,000 to 1,000,000 cycles Ported to Cypress’s latest Application Note format.
*B	3590368	ZSK	04/18/2012	Fixed typo error on page 4 to remove the following line. “The style at the bottom of this page is Body Text manually set to 7.5 pt. The first section is right aligned manually.” Updated template according to current Cypress standards.
*C	3674395	ZSK	07/18/2012	Physical SBU percentage changed from 70% to 84%. Physical MBU percentage changed from 30% to 16%. Removed repeated paragraph from “Cypress SER Test Methodologies” section.
*D	4164904	ZSK	10/29/2013	Updated in new template. Completing Sunset Review.
*E	5520623	ZSK	11/14/2016	Updated to new template. Updated Copyright.
*F	5818274	AESATP12	07/20/2017	Updated logo and copyright.

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