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**Spec No**: 001-15652

**Spec Title**: Interfacing a Cypress MoBL-USB(TM) FX2LP18 with an Intel PXA27x Processor - AN15652

**Replaced by**: NONE

AN15652

# Interfacing a Cypress MoBL-USB™ FX2LP18 with an Intel PXA27x Processor

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**Associated Project: No**
**Associated Part Family: CY4625 - MoBL-USB™**
**Software Version: NA**

MoBL-USB™ FX2LP18 is a low-power, integrated USB 2.0 microcontroller. With the MoBL-USB bridge firmware, the MoBL-USB FX2LP18 can connect to any external master, such as standard microprocessors, DSPs, application-specific integrated circuits (ASICs), and FBGAs. This application note provides an example of interfacing the MoBL-USB FX2LP18 with the Intel® PXA27x processor.

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## Introduction

MoBL-USB FX2LP18 (CY7C68053) is a low-power, integrated USB 2.0 microcontroller. The USB 2.0 transceiver, serial interface engine (SIE), enhanced 8051 microcontroller, and a programmable peripheral interface are integrated in a single chip.

When interfacing with an external processor/DSP, use the CY4625 MoBL-USB bridge firmware, which executes on the MoBL-USB FX2LP18.

The MoBL-USB bridge firmware is designed to work with any external master, such as standard microprocessors, DSPs, ASICs, and FPGAs to enable USB 2.0 support for the peripheral design. The MoBL-USB FX2LP18 controller has two double-buffered, high-speed–capable endpoints that share a 2-KB FIFO space for maximum flexibility and throughput, and control endpoint 0. The bridge firmware exposes three FIFO address pins and a 16-bit data bus for both command and data input or output.

This application note assumes the use of the MoBL-USB bridge firmware.

By using the Intel PXA27x processor as a concrete example, this application note presents some of the important design considerations when interfacing the MoBL-USB FX2LP18 (with the bridge firmware) to a processor.

## Interface Signals: Cypress MoBL-USB FX2LP18

The peripheral interface of MoBL-USB FX2LP18 is designed for a simple connection using typical embedded processors with an SRAM-style interface. Consider the main MoBL-USB FX2LP18 signals when connecting to a PXA27x processor:

- IFCLK: This pin is not needed if asynchronous mode is used. The IFCLK pin can be configured as either an input (default) or an output interface clock.
- FD[15:0]: 16-bit data bus.
- FIFOADR[2:0]: These pins select which of the two FIFOs is connected to the FD [15:0] bus, or whether the command interface is selected.
- SLCS: Slave chip select.
- SLOE and SLRD: In synchronous mode, the FIFO pointer is incremented on each rising edge of IFCLK while SLRD is asserted. In asynchronous mode, the FIFO pointer is incremented on each asserted-to-deasserted transition of SLRD. SLOE is a data bus driver enable. When SLOE is asserted, the MoBL-USB bridge firmware drives the data bus.
- FLAGA/B: FLAGx pins report the status of the FIFO. They can be configured to be Full Flag, Empty Flag, or Programmable Flag.
- SLWR: In synchronous mode, data on the FD bus is written to the FIFO (and the FIFO pointer is incremented) on each rising edge of IFCLK while SLWR is asserted. In asynchronous mode, data on the FD bus is written to the FIFO (and the FIFO pointer is incremented) on each asserted-to-deasserted transition of SLWR.

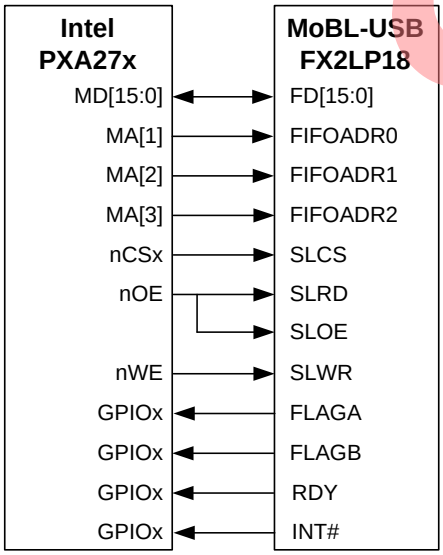
## Interface Signals: Intel PXA27x Processor

The PXA27x processor includes a memory interface that supports a variety of external memory types. The memory bus signals of the PXA27x to be considered when connecting to MoBL-USB FX2LP18 are:

- MD[31:0]: Bidirectional data for all memory types. During reads from 16-bit memory devices, the upper 16 data bits are internally pulled low.
- MA[25:0]: Output address to all memory types.
- nCSx: Active-low chip select. Though each of the PXA27x processor's six chip selects (nCS[5:0]) can be used, nCS0 is dedicated as a "bootable" memory chip select. Use any of the other five chip selects (nCS[5:1]).
- nOE and nWE: Common active low read and write control signals.
- External memory clock (CLK_MEM), SDCLK1: Note that this pin is not needed if the interface is asynchronous.

Figure 1 shows a connection example between the PXA27x processor and MoBL-USB FX2LP18 in asynchronous mode. For a more detailed sample schematic, see Appendix A. Sample Schematic. Timing analysis provided in this application note also pertains to asynchronous mode.

Figure 1. Interconnect Diagram




## FLAGS Configuration

Applications typically set FLAGA to fixed signaling of EP2 empty/not-empty status. Also, applications configure EP6 as an IN endpoint and typically set FLAGB to fixed signaling of EP6 full/not-full status. Typically, these flags are configured as active low.

This scenario means that FLAGA is low whenever the OUT endpoint is EMPTY, which tells the external processor not to attempt to read from the MoBL-USB FX2LP18. Similarly, FLAGB is low every time the IN endpoint is FULL, signaling the external processor not to attempt to write to the MoBL-USB FX2LP18.

The MoBL-USB FX2LP18 register setting required to achieve this functionality is PINFLAGSAB = 0xE8.

## Reduced Pin Configuration

Use the FLAG pins to achieve optimum throughput performance. However, a reduced pin configuration is possible by eliminating the use of the FLAG pins. The MoBL-USB bridge firmware provides the extended INNF and OUTNE interrupts.

Enable the extended interrupts, INNF and OUTNE, by setting or clearing the corresponding bit in the extended INTENABLE1 register.

OUTNE interrupt, when asserted, indicates EP2 OUT is not empty. INNF interrupt when asserted, indicates EP6 IN is not full.

For further details, refer to the *MoBL-USB Bridge Firmware Guide*.

The READY pin is used to determine when the bridge firmware is ready for a new command. The use of the READY pin signal can be replaced by the extended CMDRDY interrupt. When the CMDRDY is enabled in the INTENABLE register, a Command Ready interrupt is generated when the command interface is ready to receive a new command.

For further details, refer to the *MoBL-USB Bridge Firmware Guide*.

Figure 2 shows such a configuration.

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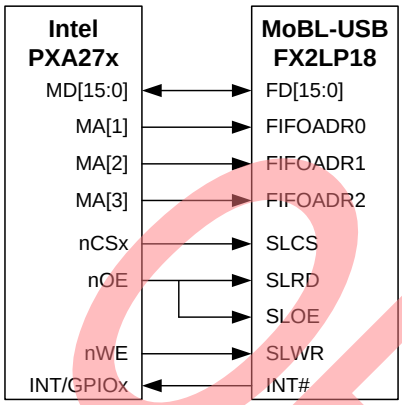
Figure 2. Reduced Pin Interconnect Diagram




## Voltage Compatibility

The MoBL-USB FX2LP18 device has a 1.8 V core operation and 1.8 V–3.3 V I/O operations. The Intel PXA27x processor supports 0.85 V to 1.55 V variable core, and 1.8 V, 2.5 V, 3.0 V, or 3.3 V memory I/O supply voltages. The two devices are compatible when voltages are set at the same levels.

## PXA27x Configurations

The MSCx registers of the PXA27x processor must be configured appropriately to interface to the MoBL-USB FX2LP18 device. The register configurations presented in this section assume:

- CLK_MEM of PXA27x is 78 MHz; that is, 12.82 ns time period. The same principle can applies if the CLK_MEM is set at a different frequency.
- RDN, RDF, and other timing parameters can be programmed in terms of CLK_MEM cycles.
- tCES equals two cycles and tCEH equals one cycle and cannot be lower than these values.
- tDSOH data setup time for read is less than or equal to 1.5 CLK_MEM. This is an internal specification for the PXA27x. If the requirement is more than 1.5 CLK_MEM, increase the read cycles accordingly.
- MSCx registers contain control information for configuring static memories connected to respective chip selects. Table 1 shows the recommended MSCx register setting for MoBL-USB FX2LP18.

Table 1. PXA27x MSCx Register Settings

| Field | Value | Description |
|---|---|---|
| RTx | 0b001 | Type of memory: SRAM |
| RBWx | 0b1 | Data bus width: 16 bits |
| RDFx | 0b0001 | Latency for read access: 1 x CLK_MEM |
| RDNx | 0b0100 | nWE low time during write: 4 x CLK_MEM |
| RRRx | 0b000 | nCS deassertion between accesses |
| RBUFFx | 0b0 | Fast/Slow device: Slow |

## Timing

This section provides a timing analysis summary of read and write operations between the PXA27x processor and MoBL-USB FX2LP18. This analysis uses the register configuration shown in the previous section.

Table 2 shows the timing parameter values required by the MoBL-USB FX2LP18 and that provided by the PXA27x processor with the register configuration described previously.

**Note** This is a theoretical timing analysis of the interface. This solution has not been simulated or tested. Actual results may vary.

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Table 2. Suggested Values for Timing Parameters

| PXA27x Symbol | Description | PXA27x Min | PXA27x Max | FX2LP18 Min (ns) | FX2LP18 Max (ns) | Recommended CLK_MEM Cycles |
|---|---|---|---|---|---|---|
| ***WRITE CYCLE PARAMETERS*** | | | | | | |
| tsramAS | Address setup to nCS assert | 1 CLK_MEM | | - | - | 1 cycle |
| | Write cycle chip select active | - | | 50 | - | 5 cycles |
| tsramASW | Address setup to nWE assert | 1 CLK_MEM | | 10 | | 1 cycles |
| tsramAH | Address hold from nWE deassert | 1 CLK_MEM | | 10 | | 1 cycles |
| tsramCES | nCS setup to nWE asserted | 2 CLK_MEM | | - | - | 2 cycles |
| tsramWL | nWE asserted time | RDN+1 CLK_MEM | | 50 | - | 5 cycles (RDN=4) |
| tsramCEH | nCS hold from nWE deasserted | 1 CLK_MEM | | 0 | - | 1 cycle |
| tsramDSWH | DATA setup to nWE deasserted | RDN+2 CLK_MEMs | | 10 | - | 6 cycles (RDN=4) |
| tsramDH | DATA hold from nWE deasserted | 1 CLK_MEM | | 10 | - | 1 cycle |
| | nWE deassert time | - | | 50 | | 5 cycles |
| ***READ CYCLE PARAMETERS*** | | | | | | |
| tromAS | Address setup to nCS asserted | 1 CLK_MEM | | - | - | 1 cycle |
| | Address to nOE setup time | - | | 10 | | 1 cycle |
| | nOE deassert to address hold time | - | | 10 | | 1 cycle |
| | nOE asserted time | - | | 50 | - | 5 cycles |
| | nOE assert to MD output propagation Delay | - | | | 15 | 2 cycles |
| | Address to FLAGS output propagation delay | - | | | 10.7 | 1 cycle |
| | nOE deassert time | - | | 50 | | 5 cycles |
| | Address to data valid (Address to nOE setup time + nOE assert to MD output propagation delay) | RDF+2 CLK_MEM | | 25 | | 3 cycles (RDF=1) |

## Summary

MoBL-USB FX2LP18 can be effectively interconnected with the Intel PXA27x processor. The timing analysis described in this application note confirms that single read and single write operations are supported. The timing analysis and recommended timing numbers for the PXA27x asynchronous SRAM interface for the single read and write are also described.

From the timing analysis, it can be concluded that:

- Read operations are performed in 13 CLK_MEM cycles equivalent to 167 ns in a 78 MHz clock. The resulting bandwidth on the peripheral interface of MoBL-USB FX2LP18 is (1/167ns) * 2 = 12 Mbytes/s.
- Write operations are performed in 11 CLK_MEM cycles equivalent to 141 ns in a 78 MHz clock. The resulting bandwidth on the peripheral interface of MoBL-USB FX2LP18 is (1/141ns) * 2 = 14 Mbytes/s.

Appendix A. Sample Schematic shows a sample schematic for the hardware connection.

Use this application note in conjunction with the *MoBL-USB Bridge Firmware Guide* for detailed information about the interface, programming the MoBL-USB FX2LP18 registers, and various system-level considerations.

## Additional Resources

For more information on FX2LP18, refer to the following documents available on the Cypress website:

- Technical Reference Manual for the MoBL-USB FX2LP18.
- CY3687 MoBL-USB FX2LP18 Development Kit
- CY4625 - MoBL-USB(TM) Bridge Reference Design

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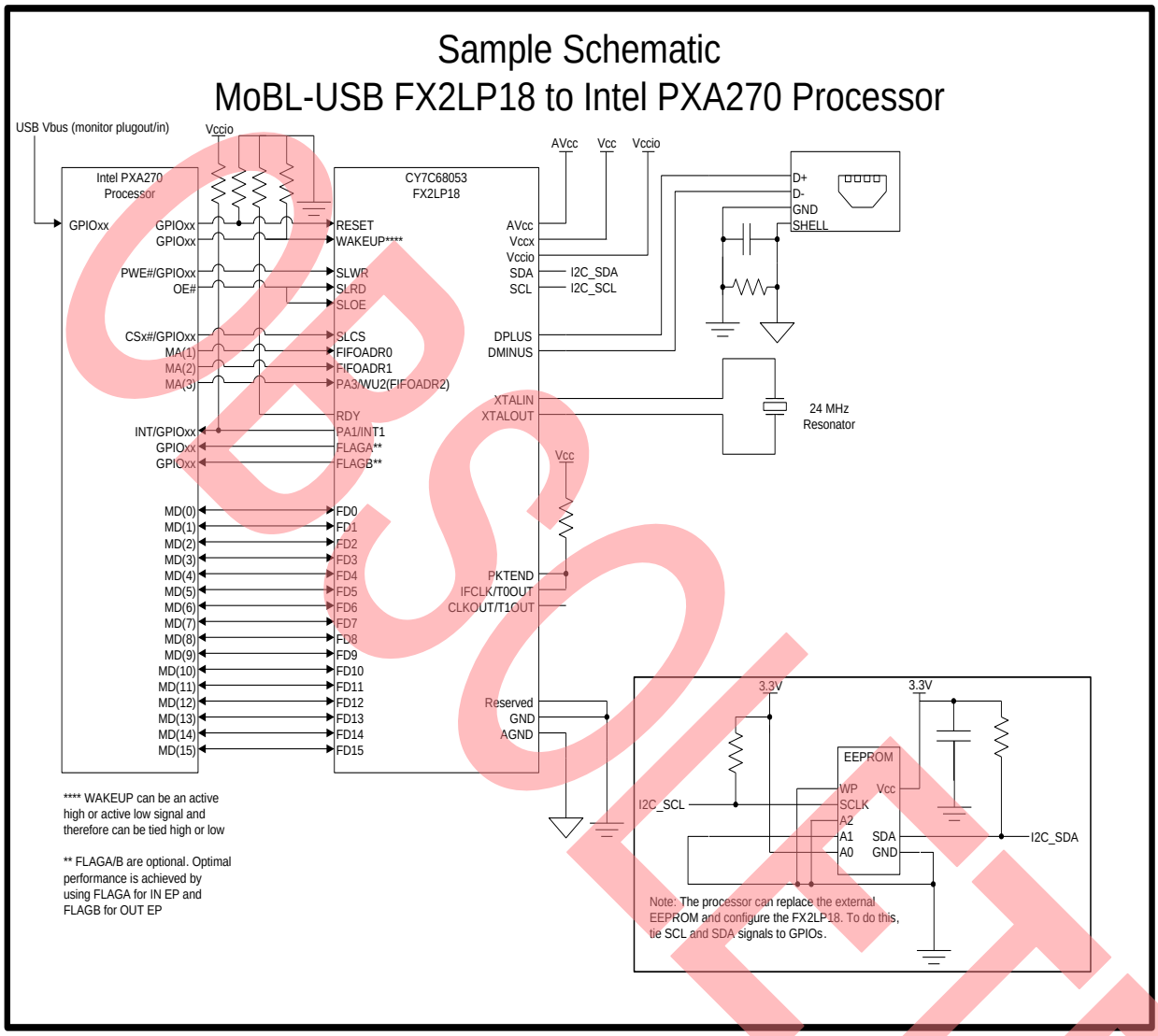
## Appendix A. Sample Schematic

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## Document History

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| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | 1168147 | RSKV | 06/24/2007 | New Application Note. |
| *A | 3121900 | RSKV | 12/28/2010 | Added additional resources and updated template. |
| *B | 3286103 | RSKV | 06/17/2011 | No change. |
| *C | 4455618 | RSKV | 07/24/2014 | Updated template. Sunset Review |
| *D | 5836322 | RAJV | 07/28/2017 | This spec is obsolete. |

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