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Spec No: 001-15330

Spec Title: Interfacing Cypress West Bridge® Antioch™ to Marvell® PXA27x Processor – AN15330

Sunset Owner: RSKV

Replaced By: None

AN15330

Interfacing Cypress West Bridge® Antioch™ to Marvell® PXA27x Processor

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Associated Project: No

Associated Part Family: West Bridge Antioch, CYWB0124AB
Software Version: Antioch SDK 1.0, 1.1
Associated Application Notes: AN13553

Abstract

West Bridge® Antioch™ provides a processor port (P-Port) that interfaces with the system processor to enable high-speed USB connectivity and mass storage access. This application note presents a system configuration example to interface the Antioch to a Marvell PXA27x processor.

Introduction

The rapid growth of mobile and embedded devices demands high-speed USB connectivity and mass storage capabilities. With that in mind, the Cypress West Bridge Antioch device (CYWB0124AB) was designed to easily enable handset designers to add these functionalities in their designs.

When Antioch is integrated into a system, the Processor Interface (P-Port) on Antioch is usually used to connect to the external bus of the principal processor.

Using the Marvell PXA27x processor as an example, this application note presents some important design considerations when interfacing the Antioch to a processor. More information about the Marvell PXA27x can be found at:

http://www.marvell.com/products/processors/applications/pxa_family/.

An example Windows CE 6.0 HAL using the PXA270 processor can be found with this application note. For further information on WinCE 6.0 integration, see **Error! Reference source not found.**.

Interface Signals

Cypress West Bridge Antioch

The P-Port interface of Antioch was designed for a simple connection with typical embedded processors and an SRAM-style interface. The main Antioch P-Port signals that are considered when connecting to a PXA27x processor include:

- Clock input-CLK. Maximum frequency for Antioch input clock is 33 MHz in synchronous mode. This pin is not needed if asynchronous mode is used.
- 16-bit data bus-DQ[15:0].
- 8-bit address bus-A[7:0].
- Active-low chip enable-CE#.
- Active-low address latch enable- ADV#.
- Common active-low read and write signals-OE# and WE#.
- Active-low DMA control channel-DRQ#. This pin is optional if the processor GPIO resource is limited.
- Active-low device interrupt-INT#.

Marvell PXA27x Processor

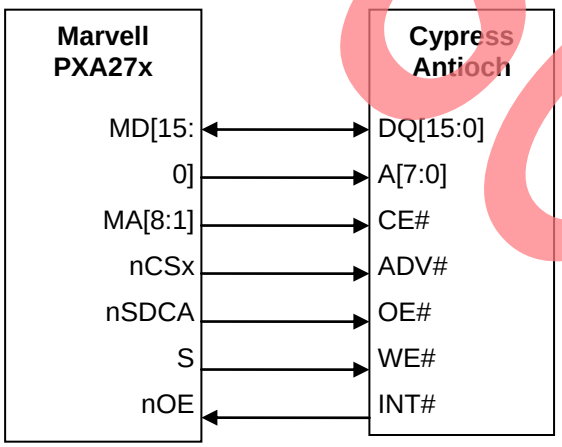
The PXA27x processor includes a memory interface that supports a variety of external memory types. The memory bus signals of the PXA27x that are considered when connecting to Antioch include:

- External memory clock (CLK_MEM)-SDCLK0 or SDCLK3. This pin is not needed if Antioch is used in asynchronous mode. Also, SDCLK3 is only available in the PXA270. For the PXA271 and PXA272, SDCLK3 is dedicated to the integrated synchronous flash device and not intended to use for external memory devices.
- 16-bit data bus- MD[15:0].

- 8-bit word address bus-MA[8:1].
- Active-low chip select-nCSx. Though each of the PXA27x processor's six chip selects (nCS[5:0]) are used, nCS0 is dedicated as a boot chip select. Use any of the other five chip selects (nCS[5:1]).
- Active-low address strobe-nSDCAS.
- Common active-low read and write control signals-nOE and nWE.
- GPIOx for device interrupt and optional DMA control.

Figure 1 shows a connection example between the PXA27x processor and Antioch in asynchronous mode. Timing analysis provided in this application note was also done in asynchronous mode, although synchronous operations between PXA27x and Antioch are possible.

Figure 1. Interconnection Diagram



Voltage Compatibility

The Antioch device operates at voltages of 1.8 V core and 1.8 to 3.3 V IO. The Marvell PXA27x processor supports 0.85 V to 1.55 V variable core, and 1.8 V, 2.5 V, 3.0 V, or 3.3 V memory IO supply voltages. The two devices are compatible when voltages are set at the same levels.

PXA27x Configurations

To properly interface the PXA27x processor to the Antioch device, the MSCx registers of the PXA27x processor must be configured. The register configurations presented in this section assume:

- CLK_MEM of PXA27x is 104 MHz; that is a 9.62 ns time period. The same principle is followed if the CLK_MEM is set at a frequency different than 104 MHz.
- RDN, RDF, and other timing parameters are programmed in terms of CLK_MEM cycles.
- tCES = 2 CLK_MEM cycles and tCEH = 1 CLK_MEM cycle, and cannot be lower than these values.
- tDSOH data setup time for read is less than or equal to two CLK_MEM cycles. This is an internal specification for the PXA27x. If the requirement is more than two CLK_MEM cycles, then read cycles must be increased accordingly.

MSCx registers contain control information for configuring static memories connected to respective chip selects. Table 1 shows the recommended MSCx register settings for Antioch.

Table 1. PXA27x MSCx Register Settings

Field	Value	Description
RTx	0b001	Memory type: SRAM
RBWx	0b1	Data bus width: 16 bits
RDFx	0b0010	Latency for read access: 3 x CLK_MEM
RDNx	0b0001	nWE low time during write: 2 x CLK_MEM
RRRx	0b000	nCS de-assertion between accesses
RBUFFx	0b0	Fast or slow device: Slow

Timing

This section provides a timing analysis summary of read and write operations between the PXA27x processor and Antioch, based on the register configuration.

Table 2 shows the timing parameter values required by the Antioch and the values provided by the PXA27x processor with the register configuration described previously.

Table 2, are maintained as they are in the West Bridge Antioch USB/Mass Storage Peripheral Controller data sheet. The values presented in Table 3 depict the relaxed value of the two timing parameters that are important when operating Antioch in asynchronous mode. This is obtained by connecting the processor's CE# signal to Antioch's CE# and ADV# signals. This allows the processor's CE# signal to be used as an ADV# signal on

All timing parameters, except those described in

Antioch. To take advantage of these relaxed timing parameters, take the following precaution. The accesses to a particular endpoint buffer must be completed before changing the addresses in favor of a different endpoint buffer or register. Limit access cycle time to 60 ns.

To determine throughput and optimization of the interface with a particular processor and further information, contact your local Cypress sales representative.

Table 2. Suggested Values for Timing Parameters

PXA27x Symbol	Description	PXA27x Min	PXA27x Max	Antioch Min (ns)	Antioch Max (ns)	Recommended CLK_MEM Cycles
WRITE CYCLE PARAMETERS						
tsramAS	Address setup to nCS asserted	1 CLK_MEM		-	-	Not Applicable
	Write cycle chip select active	-		30	-	4 cycles (3 cycles for start of nCS active to end of write and 1 cycle of address hold after write end)
tffAS	Address setup to nADV asserted	1 CLK_MEM	4 CLK_MEM	-	-	Not Applicable
tffCES	nCS setup to nADV asserted	1 CLK_MEM	4 CLK_MEM	-	-	Not Applicable
tffADV	nADV low pulswidth	1 CLK_MEM	7 CLK_MEM	5	-	1 cycle
tsramCES	nCS setup to nWE asserted	2 CLK_MEM		-	-	Not Applicable
tsramWL	nWE asserted time	RDN+1 CLK_MEM		22	-	3 cycles (RDN=2)
tsramCEH	nCS hold from new de-asserted	1 CLK_MEM		2	-	1 cycle
	Write cycle address valid	-		40	-	4 cycles
tsramDSWH	DATA setup to nWE de-asserted	RDN+2 CLK_MEMs		18	-	4 cycles (RDN=2)
tsramDH	DATA hold from nWE de-asserted	1 CLK_MEM		0	-	1 cycle
READ CYCLE PARAMETERS						
tromAS	Address setup to nCS asserted	1 CLK_MEM		-	-	Not Applicable

PXA27x Symbol	Description	PXA27x Min	PXA27x Max	Antioch Min (ns)	Antioch Max (ns)	Recommended CLK_MEM Cycles
	Read cycle address valid	RDF+2 CLK_MEM		45	-	5 cycles (includes 19.24 ns read data setup time). RDF=3.
	nOE asserted	48.1 ns		45 (30 for nCE to data valid + 15 for setup)	-	5 cycles
	Read cycle chip select active	48.1		45	-	5 cycles
	Chip select inactive	-		12.5	-	1 cycle
tffAS	Address setup to nADV asserted	1 CLK_MEM	4 CLK_MEM	-	-	Not Applicable

Table 3. Timing Parameters

Parameter	Description	Min or Max	Value	Unit
tVPH	ADV# HIGH Time	Min	12	Ns
tAVH	ADV# HIGH to Address Hold	Min	0	Ns

Figure 2 shows the timing diagram for asynchronous back-to-back read operations. Figure 3 shows the timing diagram for asynchronous back-to-back write operations.

Figure 2. Timing Diagram, Read Operations

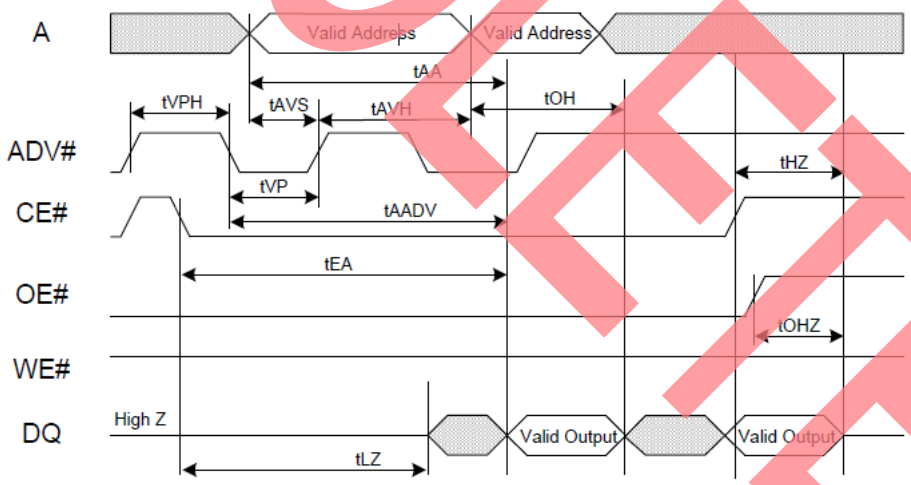
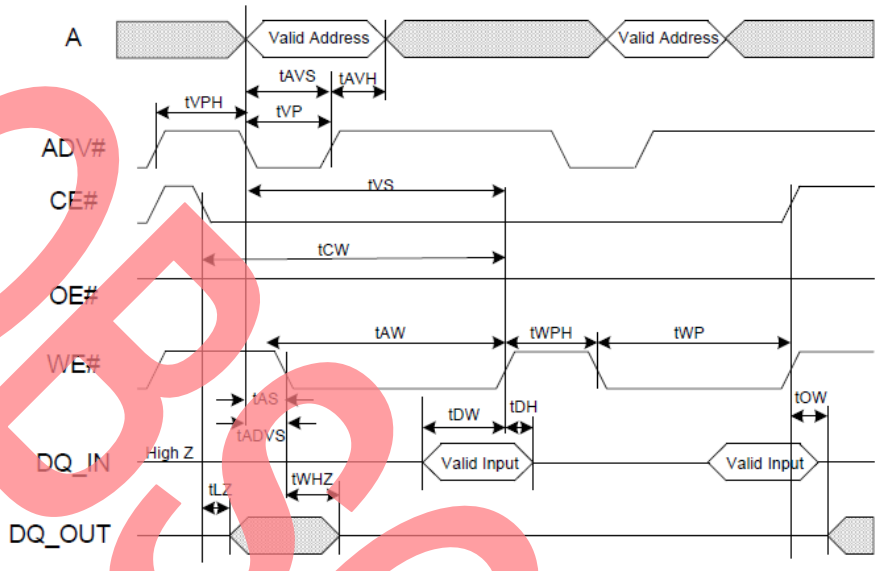


Figure 3. Timing Diagram, Write Operations



Additional Resources

- West Bridge Antioch Advance Data Sheet
- Using Processor Chip Enable as Address Valid Input to Antioch™
- Integrating West Bridge® Astoria™ with Android
- Integrating West Bridge® Astoria™ with Symbian
- Integrating West Bridge® Astoria™ with WinCE 6.0
- Marvell PXA27x Product Page

Summary

Antioch can be effectively interconnected with Marvell PXA27x processors. The timing analysis described in this document affirms that single read and write operations are supported with Antioch. The timing results and recommended timing numbers for the PXA27x asynchronous SRAM interface, for single read and write, are also documented.

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Document History

Document Title: Interfacing Cypress West Bridge® Antioch™ to Marvell® PXA27x Processor – AN15330

Document Number: 001-15330

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1046102	HKH	05/10/2007	New Spec.
*A	1653243	ODC	11/01/2007	Revised timing section and Table 2.
*B	3187216	ANOP	03/03/2011	Update to Antioch SDK Version 1.3.2., added new timing diagrams and resources section.
*C	3346124	ODC	08/16/2011	Removed attached code file.
*D	3376988	RSKV	09/20/2011	No technical changes. Template update.
*E	4538180	RSKV	10/14/2014	Obsolete document. Completing Sunset Review.

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