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# THIS SPEC IS OBSOLETE

Spec No: 001-14569

Spec Title : AN14569 - AT2LP REVISION C: RESET ISSUE AND WORKAROUND

Sunset Owner:  Rama Sai Krishna Vakkantula [rskv]

Replaced by: 001-89895

# AT2LP Revision C: Reset Issue and Workaround

# AN14569

**Author**: Amit Nanda
**Associated Project**: No
**Associated Part Family**: 68300C
**Software Version**: N/A
**Associated Application Notes**: None



## Abstract

AN14569 identifies and offers a solution for an issue seen by customers in the field when using the AT2LP revision C chip.

## Introduction

In response to customer requests, Cypress reduced many delays in the time between reset and startup for the AT2LP chip. The delay reduction occurred when the AT2LP went from revision B to revision C. With this timing change, certain drives (in many cases ATAPI drives) hang the host during the boot up process or during a soft reset [**Ctrl**] [**Alt**] [**Del**].

## Symptoms

This failure is only seen on revision C of the AT2LP chip. Revision B chips do not exhibit this problem. The symptoms most commonly noted by customers are listed below. They only occur when using the AT2LP chip revision C and the default IIC file included in the AT2LP kit. The symptoms are as follows:

1. The host hangs on bootup when the external USB drive is set to be the primary boot device in the BIOS. Most of the time, the BIOS times out and continues to boot up but occasionally some do not.
2. The host hangs when a reset is issued. In this case, most BIOS time out and continue to boot while others just hang.
3. If you probe the ATA bus with an oscilloscope, notice that the RDIOR line is held low while the RDIOW line is held high. This is what causes the host to stop booting. Since RDIOR is active low, being held low indicates it is still active and the bootup sequence cannot continue.

## Workaround

There are two parameters in the EEPROM that can change startup time:

1. Delay after reset. The default value for this parameter (‘0’) creates a delay of 1000 ms between the drive reset and the first access to the drive. If this value is not ‘0’, it can be used to adjust this delay in 20 ms increments. A value of 2 causes a (short) delay of 40 ms, while a value of 0x80 causes a (long) delay of 2560 ms. Please refer to Figure 1.
2. Skip pin reset (address = 0x05, bit 0). Setting this bit to ‘0’ causes a hard reset of the drive on a USB reset. Some drives may require a hard reset to properly configure their interface after the host is powered down. Please refer to Figure 2.

The EEPROM settings should look similar to Figure 1 and Figure 2.

Figure 1. Delay After Reset Increased

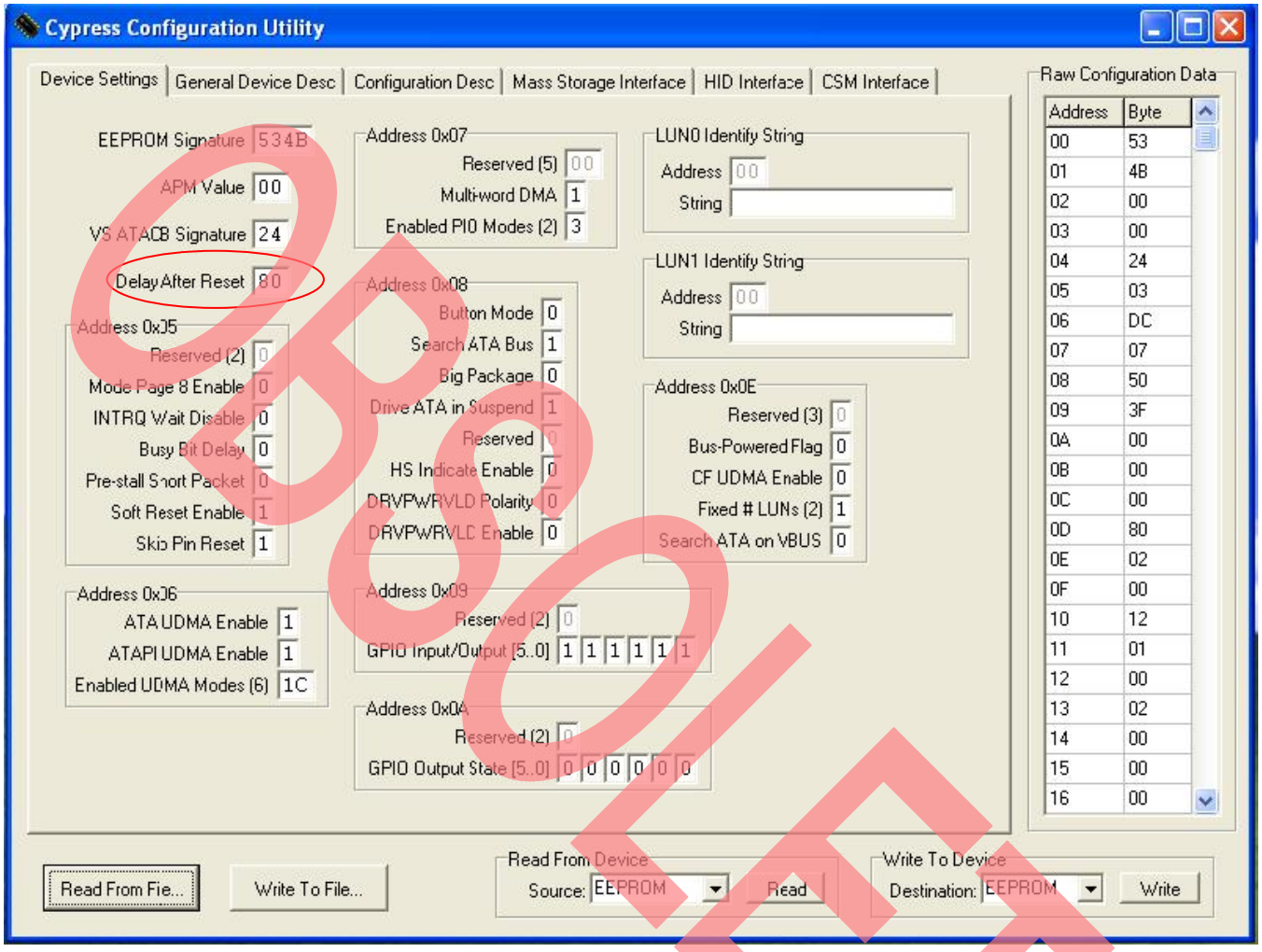
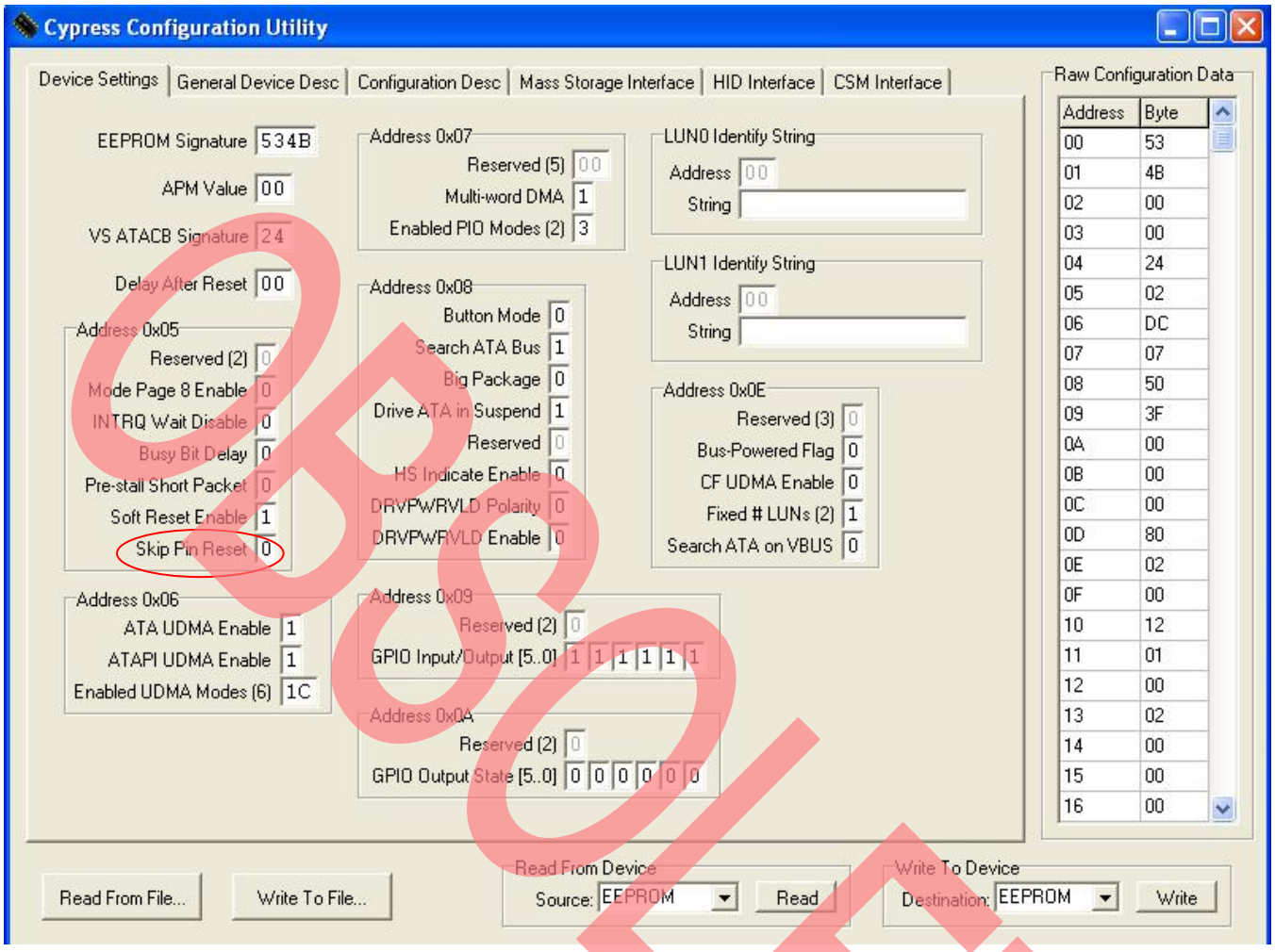


Figure 2. Delay After Reset Increased



# Document History

**Document Title: AN14569 - AT2LP Revision C: Reset Issue and Workaround**

**Document Number: 001-14569**

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | 999843 | GNA | 04/20/2007 | New application note |
| *A | 3177088 | LIP | 02/18/2011 | Template update |
| *B | 3242230 | LIP | 04/27/2011 | Title update |
| *C | 4194260 | RSKV | 11/17/2013 | Obsolete document. |





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