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**THIS SPEC IS OBSOLETE**

Spec No: 001-14569

Spec Title : AN14569 - AT2LP REVISION C: RESET ISSUE AND  
WORKAROUND

Sunset Owner: Rama Sai Krishna Vakkantula [rskv]

Replaced by: 001-89895

### AN14569

Author: Amit Nanda

Associated Project: No

Associated Part Family: 68300C

Software Version: N/A

Associated Application Notes: None

### Abstract

AN14569 identifies and offers a solution for an issue seen by customers in the field when using the AT2LP revision C chip.

### Introduction

In response to customer requests, Cypress reduced many delays in the time between reset and startup for the AT2LP chip. The delay reduction occurred when the AT2LP went from revision B to revision C. With this timing change, certain drives (in many cases ATAPI drives) hang the host during the boot up process or during a soft reset [Ctrl] [Alt] [Del].

### Symptoms

This failure is only seen on revision C of the AT2LP chip. Revision B chips do not exhibit this problem. The symptoms most commonly noted by customers are listed below. They only occur when using the AT2LP chip revision C and the default IIC file included in the AT2LP kit. The symptoms are as follows:

1. The host hangs on bootup when the external USB drive is set to be the primary boot device in the BIOS. Most of the time, the BIOS times out and continues to boot up but occasionally some do not.
2. The host hangs when a reset is issued. In this case, most BIOS time out and continue to boot while others just hang.
3. If you probe the ATA bus with an oscilloscope, notice that the RDIOR line is held low while the RDIOW line is held high. This is what causes the host to stop booting. Since RDIOR is active low, being held low indicates it is still active and the bootup sequence cannot continue.

### Workaround

There are two parameters in the EEPROM that can change startup time:

1. Delay after reset. The default value for this parameter ('0') creates a delay of 1000 ms between the drive reset and the first access to the drive. If this value is not '0', it can be used to adjust this delay in 20 ms increments. A value of 2 causes a (short) delay of 40 ms, while a value of 0x80 causes a (long) delay of 2560 ms. Please refer to Figure 1.
2. Skip pin reset (address = 0x05, bit 0). Setting this bit to '0' causes a hard reset of the drive on a USB reset. Some drives may require a hard reset to properly configure their interface after the host is powered down. Please refer to Figure 2.

The EEPROM settings should look similar to Figure 1 and Figure 2.

Figure 1. Delay After Reset Increased

**Cypress Configuration Utility**

Device Settings | General Device Desc | Configuration Desc | Mass Storage Interface | HID Interface | CSM Interface

EEPROM Signature: 534B  
 APM Value: 00  
 VS ATACB Signature: 24  
**Delay After Reset: 80**

Address 0x05:  
 Reserved (2): 0  
 Mode Page 8 Enable: 0  
 INTRQ Wait Disable: 0  
 Busy Bit Delay: 0  
 Pre-stall Short Packet: 0  
 Soft Reset Enable: 1  
 Skip Pin Reset: 1

Address 0x06:  
 ATA UDMA Enable: 1  
 ATAPI UDMA Enable: 1  
 Enabled UDMA Modes (6): 1C

Address 0x07:  
 Reserved (5): 00  
 Multi-word DMA: 1  
 Enabled PIO Modes (2): 3

Address 0x08:  
 Button Mode: 0  
 Search ATA Bus: 1  
 Big Package: 0  
 Drive ATA in Suspend: 1  
 Reserved: 0  
 HS Indicate Enable: 0  
 DRVWPWVLD Polarity: 0  
 DRVWPWVLD Enable: 0

Address 0x09:  
 Reserved (2): 0  
 GPIO Input/Output (5..0): 1 1 1 1 1 1

Address 0x0A:  
 Reserved (2): 0  
 GPIO Output State (5..0): 0 0 0 0 0 0

LUN0 Identify String:  
 Address: 00  
 String:

LUN1 Identify String:  
 Address: 00  
 String:

Address 0x0E:  
 Reserved (3): 0  
 Bus-Powered Flag: 0  
 CF UDMA Enable: 0  
 Fixed # LUNs (2): 1  
 Search ATA on VBUS: 0

Raw Configuration Data

Address	Byte
00	53
01	4B
02	00
03	00
04	24
05	03
06	DC
07	07
08	50
09	3F
0A	00
0B	00
0C	00
0D	80
0E	02
0F	00
10	12
11	01
12	00
13	02
14	00
15	00
16	00

Read From Device: Source: EEPROM Read Write To Device: Destination: EEPROM Write

Figure 2. Delay After Reset Increased

**Cypress Configuration Utility**

Device Settings | General Device Desc | Configuration Desc | Mass Storage Interface | HID Interface | CSM Interface

EEPROM Signature: 534B  
 APM Value: 00  
 VS ATACB Signature: 24  
 Delay After Reset: 00

Address 0x05:  
 Reserved (2): 0  
 Mode Page 8 Enable: 0  
 INTRQ Wait Disable: 0  
 Busy Bit Delay: 0  
 Pre-stall Short Packet: 0  
 Soft Reset Enable: 1  
 Skip Pin Reset: 0

Address 0x06:  
 ATA UDMA Enable: 1  
 ATAPI UDMA Enable: 1  
 Enabled UDMA Modes (6): 1C

Address 0x07:  
 Reserved (5): 00  
 Multi-word DMA: 1  
 Enabled PIO Modes (2): 3

Address 0x08:  
 Button Mode: 0  
 Search ATA Bus: 1  
 Big Package: 0  
 Drive ATA in Suspend: 1  
 Reserved: 0  
 HS Indicate Enable: 0  
 DRVPRVRLD Polarity: 0  
 DRVPRVRLD Enable: 0

Address 0x09:  
 Reserved (2): 0  
 GPIO Input/Output [5..0]: 1 1 1 1 1 1

Address 0x0A:  
 Reserved (2): 0  
 GPIO Output State [5..0]: 0 0 0 0 0 0

LUN0 Identify String:  
 Address: 00  
 String:

LUN1 Identify String:  
 Address: 00  
 String:

Address 0x0E:  
 Reserved (3): 0  
 Bus-Powered Flag: 0  
 CF UDMA Enable: 0  
 Fixed # LUNs (2): 1  
 Search ATA on VBUS: 0

Raw Configuration Data

Address	Byte
00	53
01	4B
02	00
03	00
04	24
05	02
06	DC
07	07
08	50
09	3F
0A	00
0B	00
0C	00
0D	80
0E	02
0F	00
10	12
11	01
12	00
13	02
14	00
15	00
16	00

Read From Device: Source: EEPROM Read

Write To Device: Destination: EEPROM Write

## Document History

Document Title: AN14569 - AT2LP Revision C: Reset Issue and Workaround

Document Number: 001-14569

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	999843	GNA	04/20/2007	New application note
*A	3177088	LIP	02/18/2011	Template update
*B	3242230	LIP	04/27/2011	Title update
*C	4194260	RSKV	11/17/2013	Obsolete document.

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