AN13553

Using Processor Chip Enable as Address Valid Input to Antioch™

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Related Application Notes: None

West Bridge® Antioch™ requires an Address Valid (ADV#) signal when the Processor Interface (P-Port) operates in asynchronous mode. Processors that do not have an ADV# signal (or any signal that can be programmed to behave like the ADV# signal) on their memory interface can use the information in this application note to interface to Antioch by connecting the processor's Chip Enable signal to both the Chip Enable (CE#) signal and the ADV# signal on Antioch. This approach allows the designer to use Antioch with processors that may not have an ADV# signal whose timing is compatible with Antioch's ADV# signal.

1 Introduction

The West Bridge Antioch device (CYWB0124AB) is a peripheral controller supporting high-speed USB and mass storage access. Antioch provides access from a processor interface and a high-speed USB (HS-USB) interface to peripherals including SD, MMC/MMC+, CE-ATA, and NAND. It supports interleaving accesses between the processor interface, the HS-USB, and the peripherals so that an external processor and an external USB host can transfer data to each other and to the mass storage peripherals simultaneously.

The Processor Interface (P-Port) on Antioch is usually connected to the principal processor in a system (for example, the baseband processor in a cell phone system). The P-Port interface is similar to an SRAM interface, and can operate in both asynchronous and synchronous modes. This Application Note deals with the asynchronous mode of operation of the P-Port in which the ADV# signal is required.

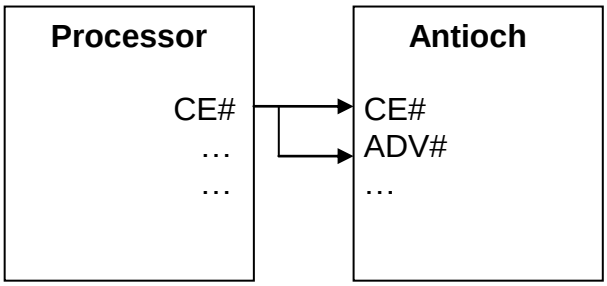
West Bridge Astoria supports SRAM interfaces natively, if the conditions in the errata document provided are followed. For more information, see the West Bridge® Astoria™ Data Sheet and the West Bridge® Astoria™ errata document.

2 ADV# Signal Use

Antioch has several internal endpoint buffers, which are accessed through the SRAM-like interface on the P-Port. These internal endpoint buffers are structured as FIFOs. During a DMA access, the address of the endpoint buffer being accessed is maintained on the address bus of the P-Port with another signal required for advancing the FIFO pointer within Antioch. In synchronous mode operation, the CLK signal is used to advance the endpoint FIFO pointer in Antioch during an endpoint access. In asynchronous mode operation, the CLK is permanently tied LOW. The toggling of the ADV# signal is required to advance the endpoint FIFO pointer within Antioch during an endpoint access. The endpoint address is latched onto the rising edge of the ADV# signal. The latch is transparent when ADV# is LOW. The rising edge of ADV# also increments the FIFO pointer of the internal endpoint buffer being accessed.

Processors that do not have an ADV# signal or any other signal whose timing can be programmed to behave like the ADV# signal can also connect to the P-Port on Antioch in asynchronous mode. In such cases, the processor's Chip Enable (CE#) signal, in addition to being connected to Antioch's CE#, can also be connected to Antioch's ADV# signal. Figure 1 depicts the simple connection of the processor's CE# to Antioch's CE# and ADV# signals.

Figure 1. Interconnection Diagram



3 Timing

When the processor's CE# signal is used as an ADV# signal on Antioch, the CE# must be toggled, that is, a new CE# access cycle must be used for every 16-bit data read or write operation. The "burst" type of access, in which the CE# remains asserted throughout and ADV# is toggled for each access, is not a valid mode of operation in this scenario. Timing parameters specified for an asynchronous single access read or write apply when using Antioch with CE# tied to ADV#. Even though the "burst" type of access is not valid because ADV#, and therefore CE#, has to be toggled every cycle, the DRQ Status Registers and DRQ Mask Registers are still used to indicate which of the endpoints is ready for a transfer.

All timing parameters, except those described in Table 1, are maintained as they are in the West Bridge: Antioch USB/Mass Storage Peripheral Controller data sheet. They are relisted in Table 2 for convenience. The values presented in Table 1 depict the relaxed value of the two parameters that are important when operating Antioch in this mode. To take advantage of these relaxed timing parameters, take the following precaution. The accesses to a particular endpoint buffer must be completed before changing the addresses in favor of a different endpoint buffer or a register. Limit the access cycle time to 60 ns.

To determine throughput and optimization of the interface with a particular processor and further information, please contact your local Cypress sales representative.

Table 1. Timing Parameters

Parameter	Description	Min or Max	Value	Unit
tVPH	ADV# HIGH Time	Min	12	ns
tAVH	ADV# HIGH to Address Hold	Min	0	ns
tVPH	ADV# HIGH Time	Min	12	ns
tAVH Antioch	ADV# HIGH to Address Hold	Min	0	ns
tAVH Astoria*	ADV# HIGH to Address Hold	Min	2	ns

* Unlike Antioch, Astoria does require Hold Time tAVH to be followed.

Table 2. Asynchronous Mode Timing Parameters

Parameter	Description	Min	Max	Unit
Read Timing Parameters				
	Interface bandwidth (MBPS)		66.7	MBps
tAA	Address to data valid	–	30	ns
tOH	Data output hold from address change	3	–	ns
tEA	Chip enable to data valid	–	30	ns
tAADV	ADV# to data valid access time	–	30	ns
tAVS	Address valid to ADV# HIGH	5	–	ns

Parameter	Description	Min	Max	Unit
tAVH	ADV# HIGH to address hold	2	–	ns
tCVS	CE# low setup time to ADV# HIGH	5	–	ns
tVPH	ADV# HIGH time	15	–	ns
tVP	ADV# pulse width LOW	7.5	–	ns
tOE	OE# LOW to data valid	–	22.5	ns
tOLZ	OE# LOW to Low Z	3	–	ns
tOHZ	OE# HIGH to High Z	0	22.5	ns
tLZ	CE# LOW to Low Z	3	–	ns
tHZ	CE# HIGH to High Z	–	22.5	ns
Write Timing Parameters				
tCW	CE# LOW to write end	30	–	ns
tAW	Address Valid to write end	30	–	ns
tAS	Address setup to write start	0	–	ns
tADVS	ADV# setup to write start	0	–	ns
tWP	WE# pulse width	22	–	ns
tWPH	WE# HIGH time	10	–	ns
tCPH	CE# HIGH time	10	–	ns
tAVS	Address valid to ADV# HIGH	5	–	ns
tAVH	ADV# HIGH to address hold	2	–	ns
tCVS	CE# LOW setup time to ADV# HIGH	5	–	ns
tVPH	ADV# HIGH time	15	–	ns
tVP	ADV# pulse width LOW	7.5	–	ns
tVS	ADV# LOW to end of write	30	–	ns
tDW	Data setup to write end	18	–	ns
tDH	Data hold from write end	0	–	ns
tWHZ	Write to DQ High Z output	–	22.5	ns
tOW	End of write to Low Z output	3	–	ns

4 Additional Resources

- West Bridge® Antioch™ Advance Data Sheet
- West Bridge® Astoria™ Advance Data Sheet
- Errata Document for West Bridge® Astoria™

5 Summary

Antioch can be effectively interconnected with processors that do not possess an ADV# signal that complies with the timing required by using the Chip Select or Chip Enable signal from the processor to control both CE# and ADV# signals on Antioch.

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	840500	ODC	03/15/2007	New Spec.
*A	3186489	ANOP	03/02/2011	Update Software Version as “Antioch SDK Version 1.3.2”. Updated Timing: Added new timing table. Added Additional Resources.
*B	4332083	DBIR	04/03/2014	Updated in new template. Completing Sunset Review.
*C	5703967	RAJV	04/20/2017	Updated template

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