AN1268

Overview of Cypress Neuron® Devices

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Software Version: N/A

Related Application Notes: N/A

Abstract

An overview of the CY7C53120E2, CY7C53120E4, and CY7C53150 products is explained in this Application Note. This includes an in-depth analysis of the technical considerations important to the design of Cypress based Neuron nodes. Specific areas covered are memory architecture, clocking structure, reset circuitry, and programming. Migration for Toshiba to Cypress Neuron devices is also covered.

Introduction

The CY7C53150 and CY7C53120 Neuron® Chips are specifically designed to implement low-cost local operating network applications. Through a unique combination of hardware and firmware, Neuron devices provide all the key functions necessary to process inputs from sensors, control devices intelligently, and propagate control information across a variety of network media.

The Neuron device has three separate processor cores. Two processors interact with a communication subsystem to make the transfer of information from node to node in a distributed control system, an automatic process. In the OSI communication model the Neuron device automatically covers the first six layers; the developer need not worry about developing code for these layers. These two processors use the LonTalk® protocol to communicate with other Lon devices over a distributed communication system. The third processor allows the developer to write application code.

The Neuron device has an 11 pin I/O interface with integrated HW and firmware for connecting to motors, valves, display drivers, A/D converters, pressure sensors, thermistors, switches, relay, triacs, tachometers, and other MCUs.

Neuron devices make it possible to rapidly implement many applications. These include: distributed sense and control systems, instrumentation, machine automation, process control, diagnostic equipment, environmental monitoring and control, power distribution and control, production control, lighting control, building automation and control, security systems, data collection/acquisition, robotics, home automation, consumer electronics, and automotive electronics. The Neuron devices communicate with each other over standard communication media such as: Twisted Pair, RF, IR, Fiber, and Coax.

Application Development

Users rely on Echelon development tools, namely the NodeBuilder®, to create application images for the CY7C53120E2, CY7C53120E4, and CY7C53150.

The current versions of the development tool (NodeBuilder 4.01.03) support all of the above-mentioned devices and their features.

For the latest version of the development tools software, visit the Echelon website at

http://www.echelon.com/products/development/nodebuilder/default.htm.

Neuron has its own version of the C programming language. To learn more information about this see

http://www.echelon.com/communities/energycontrol/developers/neuronc/default.htm

Memory Architecture

Earlier generations of Neuron chips had their on-chip non-volatile memory based on electrically erasable programmable read-only memory (EEPROM) technology. To improve performance, Cypress Neuron chips are designed and manufactured in advanced 0.35-µm silicon-oxide-nitride-oxide semiconductor (SONOS) flash process technology.

To maintain software compatibility, the on-chip flash memory is designed to automatically emulate the behavior of an EEPROM; this emulation is completely transparent to the user.

The memory can be written up to 10,000 times, with data retention of at least 10 years. As an additional feature, the flash memory supports both byte and sector based memory writes. The sector write feature is available only in the CY7C53120E4 device. The system firmware aggregates writes to eight successive memory locations into a single write thereby improving the effective endurance of the memory significantly.

To prevent data loss during an unexpected power down the CY7C53120E2, CY7C53120E4, and CY7C53150 employ internal hardware mechanisms. The first is a low-voltage detect (LVD) circuit that resets the chip when the voltage drops below acceptable flash programming voltages. Additionally, internal hardware is employed to ensure that a flash write is completed once it has begun in spite of any voltage drop. In order to ensure the functionality of the flash protection circuitry, a VCC droop time from 4.5 V to 3.5 V of at least 10 ms is required, while 15 ms droop time is strongly recommended.

The CY7C53150 device uses external memory components to store system and application code. As with the I/O models and the timing objects the external memory interface scales with input clock frequency. This means that the read and write times decreases as the clock input frequency increases. Therefore if an existing design is being migrated, and an increase in the input clock rate is desirable, it becomes important to investigate whether the changed timing parameters of the external memory interface supports the memory components in the current design.

Clocking Structure

The input clock to CY7C53120E2 and CY7C53120E4 can be generated either by an external free-running clock source, or by an on-chip oscillator using an external crystal or ceramic resonator. The on-chip oscillator design allows operation over a frequency range from 1.25 MHz to 20 MHz.

Alternatively, an externally generated clock may drive the CMOS input pin CLK1 of the Neuron chip, in which case CLK2 pin must be left unconnected or used to drive no more than one external CMOS load.

The valid input clock frequencies for the CY7C53120E2 and CY7C53150 are 20 MHz, 10 MHz, 5 MHz, 2.5 MHz, 1.25 MHz, and 625 kHz. For the 625 kHz operation, an externally generated clock must be used.

The valid input clock frequencies for the CY7C53120E4 are 40 MHz, 20 MHz, 10 MHz, 5 MHz, 2.5 MHz, 1.25 MHz, and 625 kHz. For 40-MHz and 625-kHz operation, an externally generated clock must be used.

Each channel type has a required minimum and a maximum input clock rate specified. The development tools calculate the correct parameters for the system firmware for a chosen input clock rate and channel type. Not all channel types are supported at 20 MHz and 40 MHz.

To run at 40 MHz the CY7C53150E4 requires an external clock oscillator. It is important to note that external oscillators may typically take on the order of 5ms to stabilize after power-up. The Neuron chip should be held in reset until the CLK1 input is stable. With some oscillators, this may require the use of a reset stretching low-voltage detection chip/circuit. Check the oscillator vendor's specification for more information about startup stabilization times.

Neuron Chip I/O and Timing Models at 20 or 40 MHz

In most cases, doubling or quadrupling the input clock rates doubles or quadruples the Neuron chip's application performance. This is true for most of the I/O models as well. Table 1 compares some of the I/O model timings for 10-, 20-, and 40-MHz input clock rates.

By the same token, some timer objects have different timing specifications at 20 and 40 MHz. This is shown in

Table 2.

Because of these two facts, the user must be careful when upgrading existing designs to 20 MHz or 40 MHz. In applications where timer/counter I/O objects or timer/delay objects are used, it is sometimes necessary to change the timing parameters to accommodate the change in input clock frequency.

Table 1: I/O Model Timing Vs. Input Clock Rate

I/0 Model	10 MHz Timing	20 MHz Timing	40 MHz Timing
Parallel I/O	2.4us per byte	1.2 us per byte	0.6 us per byte
Bithift I/O	1,10,or 15 kbps	2,20, or 30 kbps	4, 40, or 60 kbps
Magcard Input	Up to 8,334 bps	Up to 16,668 bps	Up to 33,336 bps
Magrack 1	Up to 7,246 bps	Up to 14,492 bps	UP to 28,984 bps
Neurowire Master	1,10, or 20 kbps	2,20, or 40 kbps	4,40, or 80 kbps
Neurowire Slave	Up to 18 kbps	Up to 36 kbps	Up to 72 kbps
Serial I/O	0.6, 1.2, 2.4, or 4.8 kbps	1.2, 2.4, 4.8, or 9.6 kbps	2.4, 4.8, 9.6, or 19.2 kpbs
Touch I/O	For 5 and 10 MHz only	Not supported	Not supported
Frequency Output	Resolution: 0.4 to 51.2 use max Range: 26.21 to 3,355 ms	Resolution: 0.2 to 25.6 us max Range 13.10 to 1,678 ms	Resolution: 0.1 to 12.8 us max. Range: 6.55 to 839 mse
Other Timer/Counter I/Os	Resolution: 0.2 to 25.6 us max Range 13.11 to 1,677 ms	Resolution: 0.1 to 12.8 us max. Range: 6.55 to 838.8 mse	Resolution: 0.05 to 6.4 us max. Range: 3.28 to 419.3 mse

Table 2: Timing of Other Timers vs. Input Clock Rate

Timer	10 MHz	20 MHz	40 MHz
Watchdog timer	840 ms	420 ms	210 ms
Millisecond timer	1 to 64,000 ms	1 to 64,000 ms	1 to 64,000 ms
Second timer	1 to 65,535 sec	1 to 65,535 sec	1 to 65,535 sec
delay() function	33,333 counts	16,666 counts	8,333 counts
get_tick_count() function	819.2 us per count	409.6 us per count	204.8 us per count

Interoperability Considerations for 20- and 40-MHz Nodes

20- and 40-MHz nodes based on Cypress Neuron chips will be interoperable with 10-MHz nodes as long as the communications parameters are the same. In other words, interoperable nodes must be on the same channel type, even though they have different input clock rates. For example, a 40-MHz node based on CY7C53120E4 on the 78.13-kbps TP/FT-10 channel communicates with a 10 MHz node on the same channel.

Note that not all existing channel types are supported at 20 and 40 MHz. Each channel type has a required minimum and a maximum input clock rate specified. The development tools calculate the correct parameters for the system firmware for a chosen input clock rate and channel type.

If the user has to work with a channel type that has already been deployed and not supported by 20- and 40-MHz Neuron chips, they can always use the 40-MHz devices with an input clock of 10 MHz or less

Reset

The Neuron chip reset pin is an open-drain active-LOW I/O pin with an internal pull-up. The reset pin can be driven active from an external signal or can be an output driven by internal reset sources. When using an external signal to drive the reset, ensure that the driver is open-drain drives low. An external device should never drive the reset line high. The internal reset sources include power-on reset, low-voltage detect (LVD) reset, watchdog reset and software reset.

For the Cypress Neuron chips, all internally generated resets will have the reset active pulse stretched for 323 input clock periods (about 32.3 µs at 10 MHz). All resets driven by external sources are stretched for 67 input clock periods. The reset pulse is stretched to allow internal initialization before the processors start executing.

When the reset is held LOW, either from an external pull-down or an internal source, the following behavior is observed on the CY7C53120Ex Neuron chip signal pins:

- All I/O pins go to a high-impedance mode
- Service pin goes to an undetermined state
- Communication port pins go to a high-impedance mode.

Programming

In choosing a programming method, different options should be evaluated for flexibility, speed, and cost. The different options to program the Cypress Neuron chips are:

1. Universal device programmers
2. Network programming

Network Programming

Network programming refers to a programming method where the application image is downloaded into the user space through the use of the Neuron's COMM Port. This method of programming takes advantage of the Neuron chip's built-in LonTalk® capability, which allows it to perform field upgrades to the application.

Performing network programming requires a number of items: an NEI programming file; a programmer or tool that generates the required LonTalk commands to load the application image into the user memory of the Neuron chip; finally, it is necessary that the Neuron chip and the programmer be configured to communicate on the same channel. The default configuration of a Cypress Neuron chip is differential mode, running at 10 MHz and 1.25 Mbps. Slower communication bit rates can be accomplished by scaling the clock frequency down accordingly.

Network programming is employed by custom Neuron Programmers. These programmers work by communicating with the Neuron chip over the default channel.

Another way to use the network programming method is through the use of a network manager. Echelon also offers a variety of network managers with varying types of interfaces to the PC. A network manager is also part of the LonBuilder development tool. The network manager's communication channel needs to match that of the Neuron chip. See the user guide for the network manager for more information on how to perform application downloads to a Neuron chip. Contact Echelon for more information on available network managers.

One key disadvantage of this programming option is the requirement for the communication parameters between the device and the programmer to agree. If the parameters on a given device are changed, it can no longer communicate with the programmer. Another disadvantage of this method is the relatively long time needed to program compared to other methods now available.

Universal Device Programmers

The Cypress Neuron chips provide a major advantage over the previous generations of Neuron chips by offering the option to program using universal device programmers (UDPs). UDPs have built-in support for a wide variety of programmable devices such as EPROMs, PLDs, flash memories, and microcontrollers.

To program a Cypress 3120 Neuron using a UDP, an application image in the NFI file format is needed. Also necessary are socket adapters specific to the Neuron chip package being targeted (either a 32-lead SOIC or 44-lead TQFP). These adapters are available from the programmer vendor.

Universal device programmers are ideal in both the engineering and the production environment. In the product development phase using a UDP means that a single programmer can be used for all the devices without having to resort to a dedicated programmer for the Neuron chips. Additionally, UDPs provide generally fast programming times and eliminate the problem of communication parameter compatibility issues associated with older programming methods.

For production purposes universal device programmers are available to meet a wide variety of volume and cost demands. Programmer vendors have a large number of options varying from multi-site programming units to fully automated programming systems. The programming vendor assists in choosing the best production programmer to fit your needs.

Both Hi-Lo and BP Micro create UDPs for the Neuron Device

Migration from Toshiba to Cypress

The CY7C3120E4 represents a new member in the Neuron Chip family with improved performance. It supports a faster 40-MHz operating frequency, a larger 12-KB ROM and a 4-KB EEPROM. Because of its expanded features and memory configuration, new system firmware is required. Echelon has released Version 13 system firmware to support the CY7C53120E4.

Existing Neuron C application code targeted at previous generations of 3120 Neuron Chips needs to be recompiled for the CY7C53120E4

When migrating from a previous 3120 Neuron Device to the Cypress CY7C53120E2 Device, care must be taken with regards to RAM space. The Cypress Neuron Device has 2KB of SRAM while Toshiba Neuron Devices could have up to 4KB of SRAM. Also the E2 Device runs on firmware version 6 and some Toshiba devices run on different firmware versions. Thus it is recommended if using an E2 device to recompile for firmware version 6.

The 0.35 mm-based CY7C53150 is a near drop-in replacement for the previous generation Neuron 3150 Toshiba (TMPN3150B1AF). There are slight package differences between the two parts that need to be considered when migrating. The Toshiba part is a 64-pin QFP and the Cypress part is a 64-pin TQFP. Inspect the PCB land pattern to ensure the Cypress TQFP fits on a QFP pattern.

For more information on the differences between Neuron devices see

http://www.echelon.com/Support/documentation/bulletin/005-0175-01E_NeuronChipMatrixE.pdf

Document History

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*A	3175731	TDU	02/17/2011	Title and template update
*B	3340666	TDU	08/10/2011	Updated Programming and Migration sections
*C	3435014	TDU	11/10/2011	Minor text edits Template update.
*D	4491078	AAE	09/02/2014	Sunset Review – No Change

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