AN1236

CY23FP12 Field Programming Guide

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Related Application Notes: AN1234

AN1236 explains the device architecture, programmable options, programming process, and software configuration tools of the CY23FP12, a high-performance zero-delay buffer (ZDB) makes it a versatile clock distribution solution.

1 Introduction to CY23FP12

CY23FP12 is a field-programmable zero-delay buffer. It is a high-performance clock-distribution device that can be customized for a wide range of applications. CY23FP12, which integrates the functionalities of complete clock distribution solutions, takes advantage of Cypress's proprietary non-volatile memory technology to provide a fully programmable device. For prototypes, programmers are used; else, Cypress distributors take the responsibility of programming in large volumes.

Figure 1 shows the basic block diagram of CY23FP12. It employs a single phase-locked-loop (PLL) architecture to provide 12 output clocks that are aligned in phase. The 12 outputs are derived from either the PLL output or the reference frequency (REF). All outputs are grouped into one of two banks (Bank A and Bank B) with separate power supply pins, which can be connected independently to either a 2.5-V or 3.3-V power supply. Bank A has three pairs (CLKA0/CLKA1, CLKA2/CLKA3, and CLKA4/CLKA5) and Bank B has three pairs (CLKB0/CLKB1, CLKB2/CLKB3, and CLKB4/CLKB5) as well.

There are five post-divider options: /1, /2, /3, /X; where X is a programmable value between 5 and 130. Each pair has its own post dividers so they can be programmed to a custom frequency. There is also an option to have complementary outputs to the inputs. For further reference to zero delay buffers, refer to Application Note AN1234.

The field-programmable zero-delay buffer enables the user to define an application-specific clock distribution device by customizing parameters such as: input and output dividers, feedback topology (internal/external), output inversions, and output drive strengths. For additional flexibility, the user can choose from multiple functions listed in CyberClocks Tool Suite and assign a particular function set to any of the four possible select (S1/S2) control-bit combinations. This feature allows for implementation of four distinct options, selectable with the S1/S2 pins on a single device. Cypress’s field-programmable zero-delay buffers also feature a proprietary auto power-down circuit, which shuts down the device in case of a reference clock source failure.

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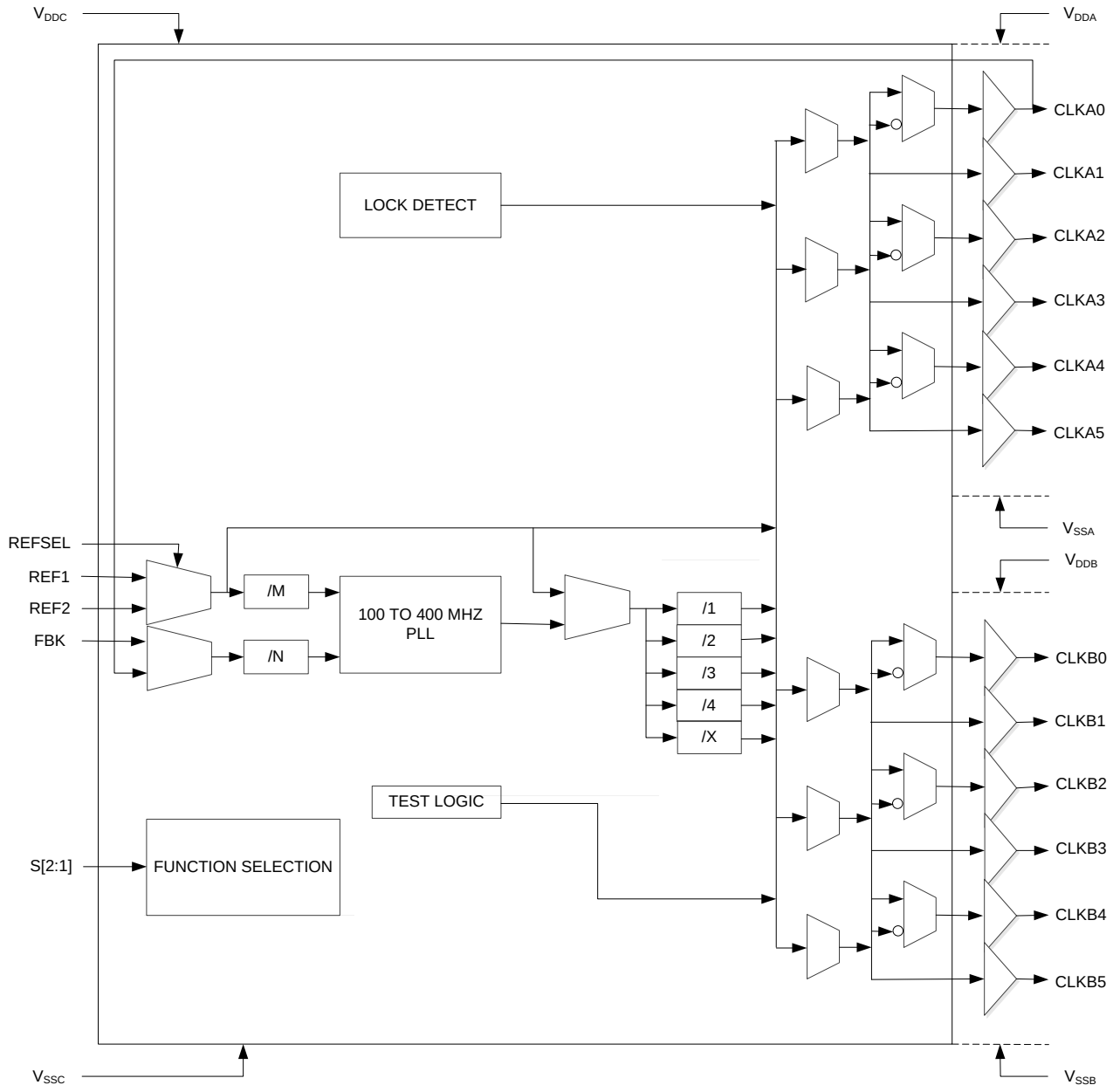
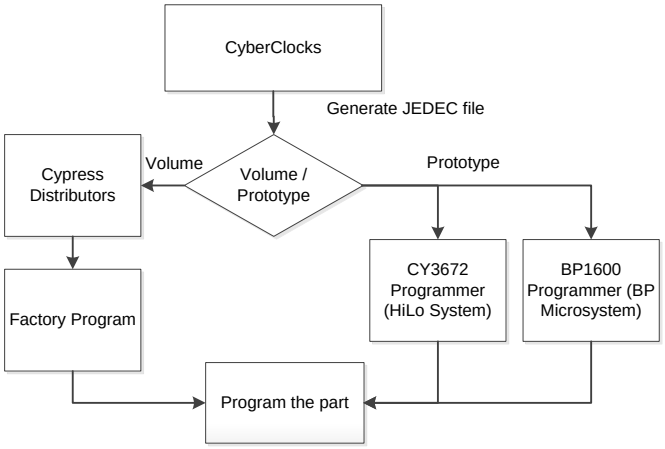
Figure 1. Block Diagram



2 Configuring and Programming the CY23FP12

Figure 2 shows the programming flow chart for CY23FP12. Cypress provides the software “CyberClocks” to configure and program its clocks. CY23FP12 can also be configured using this software. GUI of CyberClocks allows selection and input of specific requirements. A JEDEC file is generated that can be downloaded to the clock device using specific programmers (HiLo System or BP Microsystem).

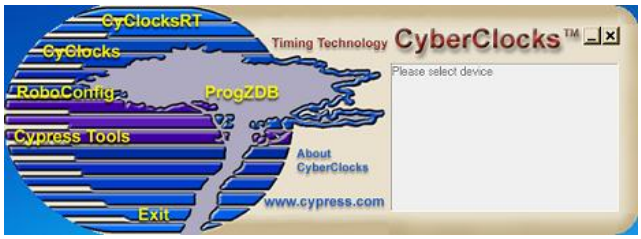
Figure 2. Programming Flowchart



2.1 CyberClocks Tool Suite

CyberClocks (Figure 3) is an integrated tool suite designed to combine CyClocksRT, CyClocks, ProgZDB, and RoboConfig™ into one seamless package. ProgZDB is an easy-to-use software application that allows the user to custom-configure CY23FP12. Users can specify the reference input frequency, PLL enable, output frequencies, and post-divider values along with different functional options. ProgZDB outputs an industry-standard JEDEC file to program CY23FP12. CyberClocks can be downloaded from the Cypress website.

Figure 3. CyberClocks



From the CyberClocks interface shown in Figure 3, choose ProgZDB and then “CY23FP12” as shown in Figure 4. This will initiate the CY23FP12 software configuration GUI as shown in Figure 5.

Figure 4. ProgZDB CY23FP12

The CY23FP12 configuration software has two modes: basic mode (Figure 5) and advanced mode (Figure 6). By default, the software will load the basic mode. Different configuration parameters of these modes are explained in Table 1 and Table 2.

Figure 5. ProgZDB CY23FP12 Basic Mode

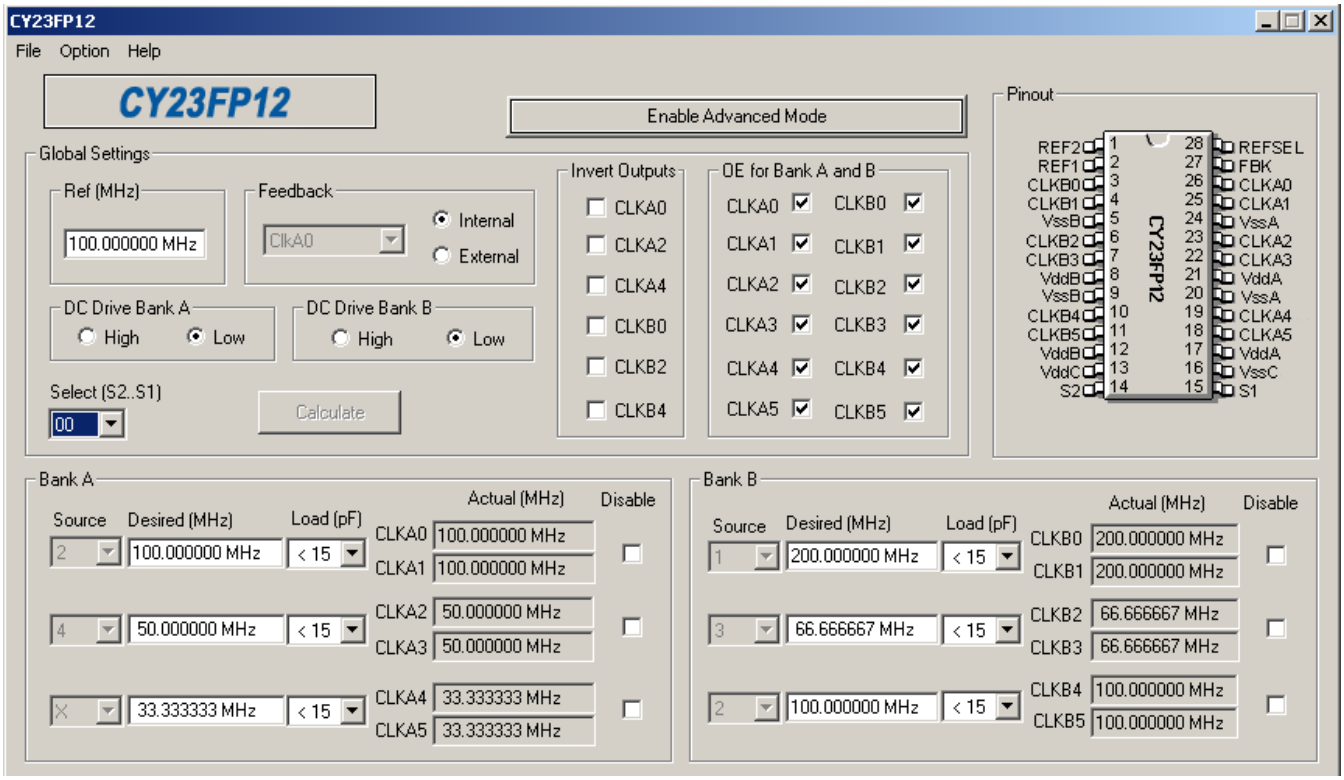


Table 1 is a list of independent functions that can be configured and programmed with either volume or prototype programmer. Some of these options are available only in the advanced mode.

Table 1. Global Setting Options

Configuration	Description	Default
DC Drive Bank A	Programs the drive strength of Bank A outputs. The user can select one out of two possible drive strength settings that produce output DC currents in the range of ±16 mA to ±20 mA.	±16 Ma
DC Drive Bank B	Programs the drive strength of Bank B outputs. The user can select one out of two possible drive strength settings that produce output DC currents in the range of ±16 mA to ±20 mA.	±16 mA
Output Enable for Bank B clocks	Enables/Disables CLKB[5:0] outputs. Each of the six outputs can be disabled individually if not used, to minimize electromagnetic interference (EMI) and switching noise.	Enable
Output Enable for Bank A clocks	Enables/Disables CLKA[5:0] outputs. Each of the six outputs can be disabled individually if not used, to minimize EMI and switching noise.	Enable
Inv CLKA0	Generates an inverted clock on the CLKA0 output. When this option is programmed, CLKA0 and CLKA1 will become a complimentary pair.	Non-invert
Inv CLKA2	Generates an inverted clock on the CLKA2 output. When this option is programmed, CLKA2 and CLKA3 will become a complimentary pair.	Non-invert
Inv CLKA4	Generates an inverted clock on the CLKA4 output. When this option is programmed, CLKA4 and CLKA5 will become a complimentary pair.	Non-invert
Inv CLKB0	Generates an inverted clock on the CLKB0 output. When this option is programmed, CLKB0 and CLKB1 will become a complimentary pair.	Non-invert
Inv CLKB2	Generates an inverted clock on the CLKB2 output. When this option is programmed, CLKB2 and CLKB3 will become a complimentary pair.	Non-invert

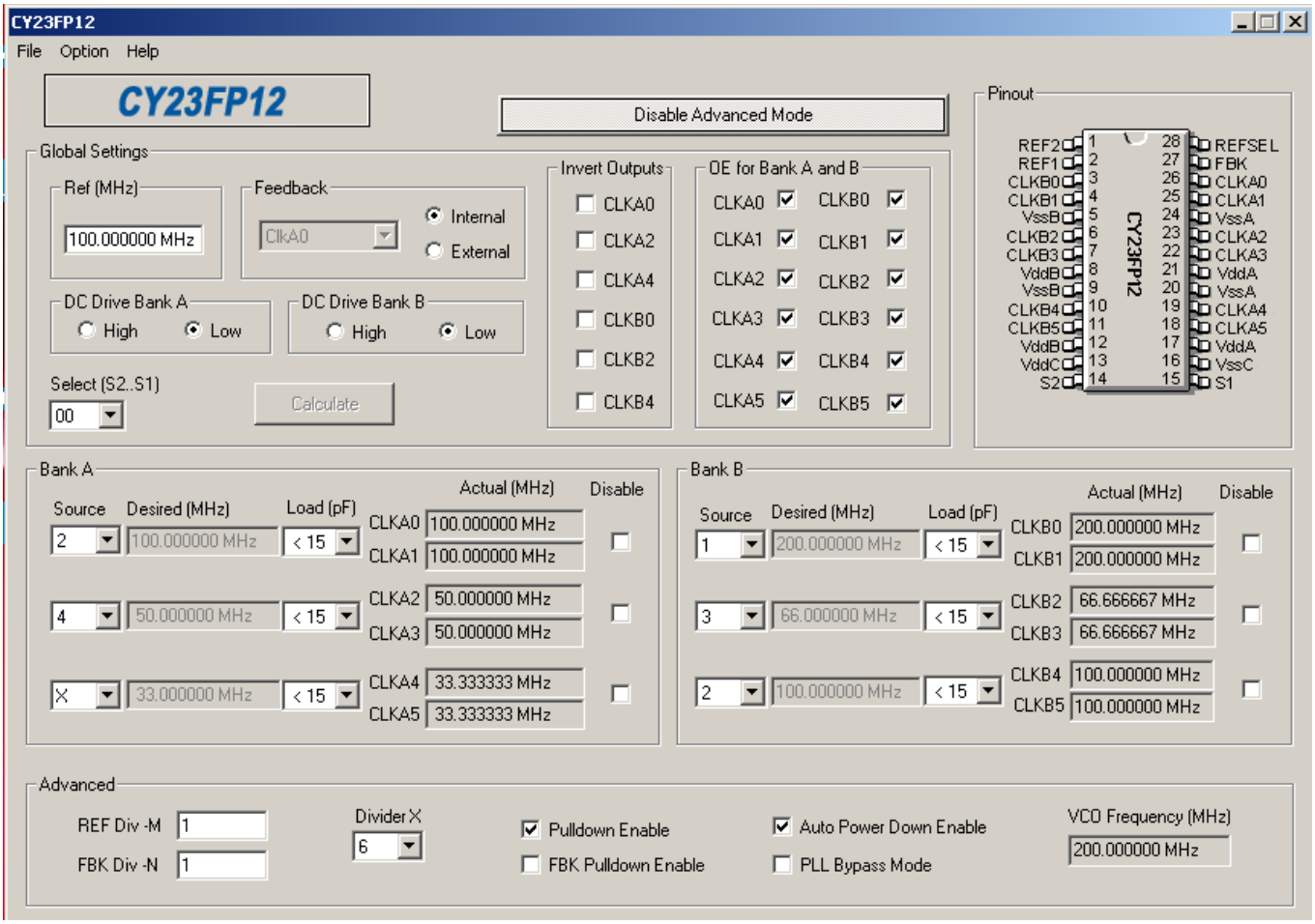
Configuration	Description	Default
Inv CLKB4	Generates an inverted clock on the CLKB4 output. When this option is programmed, CLKB4 and CLKB5 will become a complimentary pair.	Non-invert
Pull-down Enable (advanced mode)	Enables/Disables internal pulldowns on all clock outputs	Enable
Fbk Pull-down Enable (advanced mode)	Enables/Disables internal pulldowns on the feedback path (applicable to both internal and external feedback topologies)	Enable

Table 2 lists the independent functions which can be assigned to each of the four S1/S2 combinations. Basic mode controls some settings (which are available only in the advanced mode) automatically by prompting the user to input their desired output frequency and then calculating the necessary values.

Table 2. S1/S2 Select Input Combination Configuration Options

Function	Description	Default
Output Enable CLKB[5:4]	Enables/Disables CLKB[5:4] output pair	Enable
Output Enable CLKB[3:2]	Enables/Disables CLKB[3:2] output pair	Enable
Output Enable CLKB[1:0]	Enables/Disables CLKB[1:0] output pair	Enable
Output Enable CLKA[5:4]	Enables/Disables CLKA[5:4] output pair	Enable
Output Enable CLKA[3:2]	Enables/Disables CLKA[3:2] output pair	Enable
Output Enable CLKA[1:0]	Enables/Disables CLKA[1:0] output pair	Enable
Auto Power-down Enable	Enables/Disables the auto power down circuit, which monitors the reference clock rising edges and shuts down the device in case of a reference “failure”. This failure is triggered by a drift in reference frequency below a set limit. This auto power down circuit is disabled internally when one or more of the outputs are configured to be driven directly from the reference clock.	Enable
PLL Power-down	Shuts down the PLL when the device is configured as a non-PLL fanout buffer.	PLL Enabled
M[7:0]	Assigns an eight-bit value to reference divider –M. The divider can be any integer value from 1 to 256; however, the PLL input frequency cannot be lower than 10 MHz.	2
N[7:0]	Assigns an eight-bit value to feedback divider –N. The divider can be any integer value from 1 to 256; however, the PLL input frequency cannot be lower than 10 MHz.	2
X[6:0]	Assigns a seven-bit value to output divider –X. The divider can be any integer value from 5 to 130. Divide by 1, 2, 3, and 4 are preprogrammed on the device and can be activated by the appropriate output mux setting.	1
Divider Source	Selects between the PLL output and the reference clock as the source clock for the output dividers.	PLL
CLKA5,4 Source	Independently selects one out of the eight possible output dividers that will connect to the CLKA5 and CLKA4 pair.	Divide by 2
CLKA3,2 Source	Independently selects one out of the eight possible output dividers that will connect to the CLKA3 and CLKA2 pair.	Divide by 2
CLKA1,0 Source	Independently selects one out of the eight possible output dividers that will connect to the CLKA1 and CLKA0 pair.	Divide by 2
CLKB5,4 Source	Independently selects one out of the eight possible output dividers that will connect to the CLKB5 and CLKB4 pair.	Divide by 2
CLKB3,2 Source	Independently selects one out of the eight possible output dividers that will connect to the CLKB3 and CLKB2 pair.	Divide by 2
CLKB1,0 Source	Independently selects one out of the eight possible output dividers that will connect to the CLKB1 and CLKB0 pair.	Divide by 2

Figure 6. PrgZDB CY23FP12 Advanced Mode



Advanced mode, shown in Figure 6, gives the user more flexibility to configure the device exactly as required. Features such as enabling/disabling internal pulldowns on all outputs, enabling/disabling internal pulldowns on the feedback path, selecting the REF input divider M value, FBK input divider N value, and output divider X value are all directly controlled by the user when advanced mode is enabled. Refer to the Help file for CyberClocks for more detailed information on usage of the software.

3 Programmers for CY23FP12[1]

3.1 CY3672 Programmer

The Cypress CY3672 FTG Development Kit cab be used to configure and program CY23FP12 samples in small prototype quantities. It has a small portable programmer that connects to a USB port for on-the-fly programming of custom frequencies. The JEDEC file output of CyberClocksRD™ (Embedded in CyberClock software) or CyberClocks online can be downloaded to the portable programmer. This is for small-volume programming or a production programming system for larger volumes. The datasheet for the CY3672 is available on the Cypress website. The CY3672 programming kit includes three sockets for the CY23FP12: CY3695, CY3698, and CY3699.

[1] To know the latest programming options, contact our Technical Support team at www.cypress.com/support, or mail to clocks@cypress.com . You can also visit www.cypress.com/go/cy3675 to know the latest update on the kit information and software.

3.2 BP1600 Programmer (BP Microsystem)

The BP1600 programmer and socket SM28SSA are used for CY23FP12 programming. The JEDEC file output of CyberClocks can be downloaded to this programmer for larger volumes. You can order the programmer and socket from the BP Micro System website at www.bpmicro.com.

3.3 Factory Programming

Cypress can also program the devices in-house, depending on volume. Contact your Cypress Sales representative or local Cypress Field Applications Engineer for more information.

4 Summary

The rich feature set of the field programmable CY23FP12 zero delay buffer makes it useful for clock distribution in a variety of applications. The ProgZDB configuration software within the CyberClocks software suite, when used in conjunction with a programmer kit, allows the user to quickly and easily custom-configure the CY23FP12 to meet their specific needs.

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	946546	KVM	04/11/2007	New application note.
*A	3254457	CXQ	05/12/2011	Major document revision for content clarity. Updated template to current Cypress standards.
*B	3726269	CINM	09/04/2012	Updated in new template.
*C	4389903	XHT	05/28/2014	Sunset review.
*D	5775663	TAVA	06/20/2017	Updated template The note of contacting Cypress Technical support is included in page 1 The note to visit the CY3675 webpage to know the latest update is included in page 6.

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